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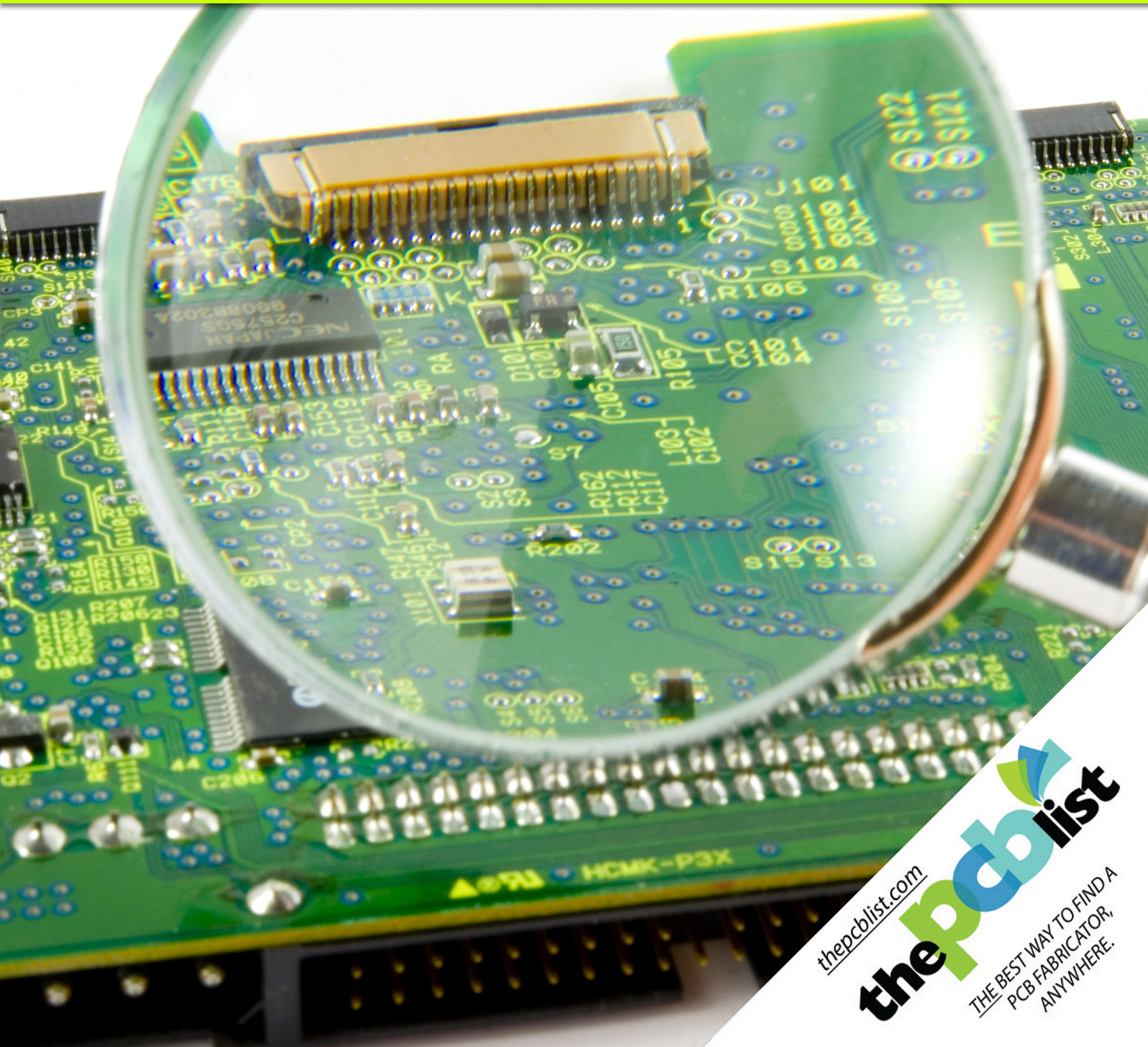
ENGINEERING SOLUTIONS FOR PCB MANUFACTURING

# SMT® MAGAZINE

JULY 2016



## FOCUSING ON TEST AND INSPECTION



# 2016 IWLPC

13th International Wafer-Level Packaging Conference

October 18-20, 2016 San Jose, California

SMTA Surface Mount Technology Association

Chip Scale Review — ChipScaleReview.com — The Future of Semiconductor Packaging

## Event Schedule

### October 18-19, 2016

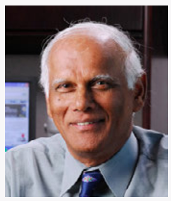
- Exhibition
- Panel Discussions
- Technical Presentations:
  - 3D
  - MEMS
  - WLP
  - Manufacturing Challenges

### October 20, 2016

Four Half-Day Workshops To Be Announced.

## Keynote Presentations

Advanced Technology Platforms for Next Generation of Smart Systems
Klaus-Dieter Lang, Ph.D.
Fraunhofer IZM



The Promise and Future of Wafer Fan-out Technology
Rao R. Tummala, Ph.D.
Georgia Institute of Technology

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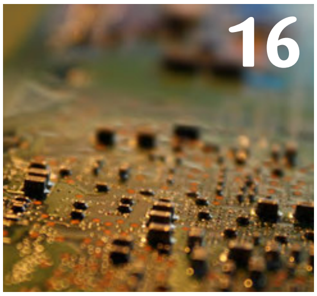



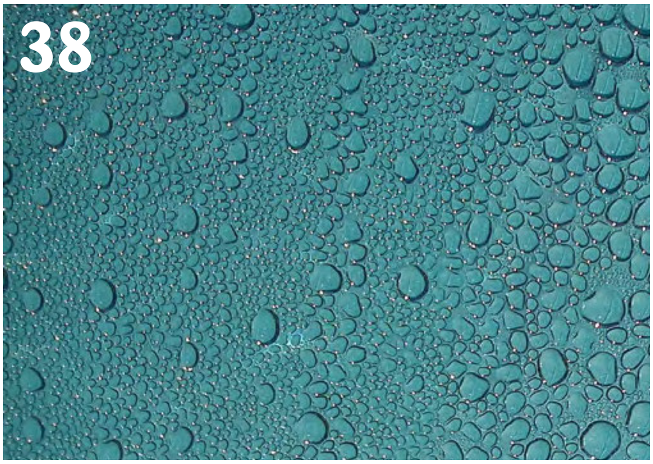




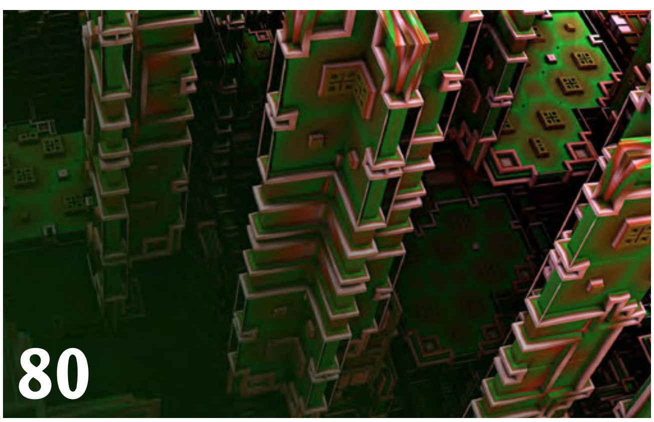


# PCBA Test and Inspection

This month, *SMT Magazine* discusses test and inspection technologies that help identify PCB assembly defects for the improvement of associated manufacturing processes.

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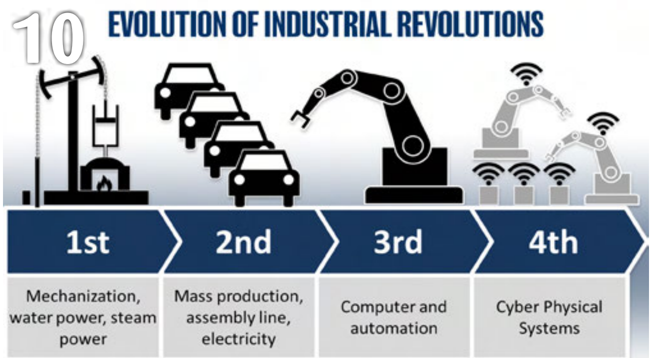


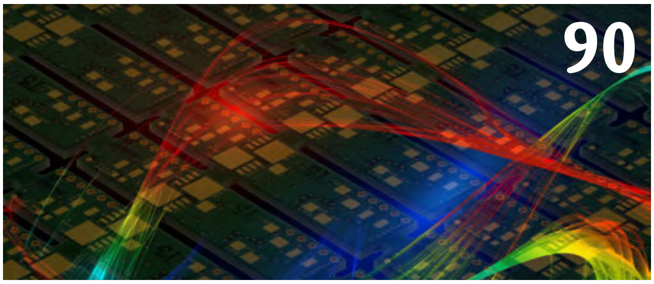



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# Improving Test and Inspection

**by Stephen Las Marias**
I-CONNECT007

Our survey last month on the challenges manufacturers face regarding tighter tolerances, finer lines and features in assemblies provided us two key issues: solder paste printing challenges, which we covered in-depth in the June edition of *SMT Magazine,* and PCBA testing and inspection, the topic for this month's issue.

It is interesting to note that in our recent survey on PCBA test and inspection challenges, most respondents consider these same subjects to be among their main problems. Some of those problems include: probing to narrower traces and pads; testing boards with smaller and finer features and sizes; dry solder; and other solder-related issues that cannot be easily detected during PCBA testing. Other challenges include finding sublayer defects; dealing with flat, no-lead components; and testing cycle time, as more manufacturers grapple with high-mix, low-volume production issues.

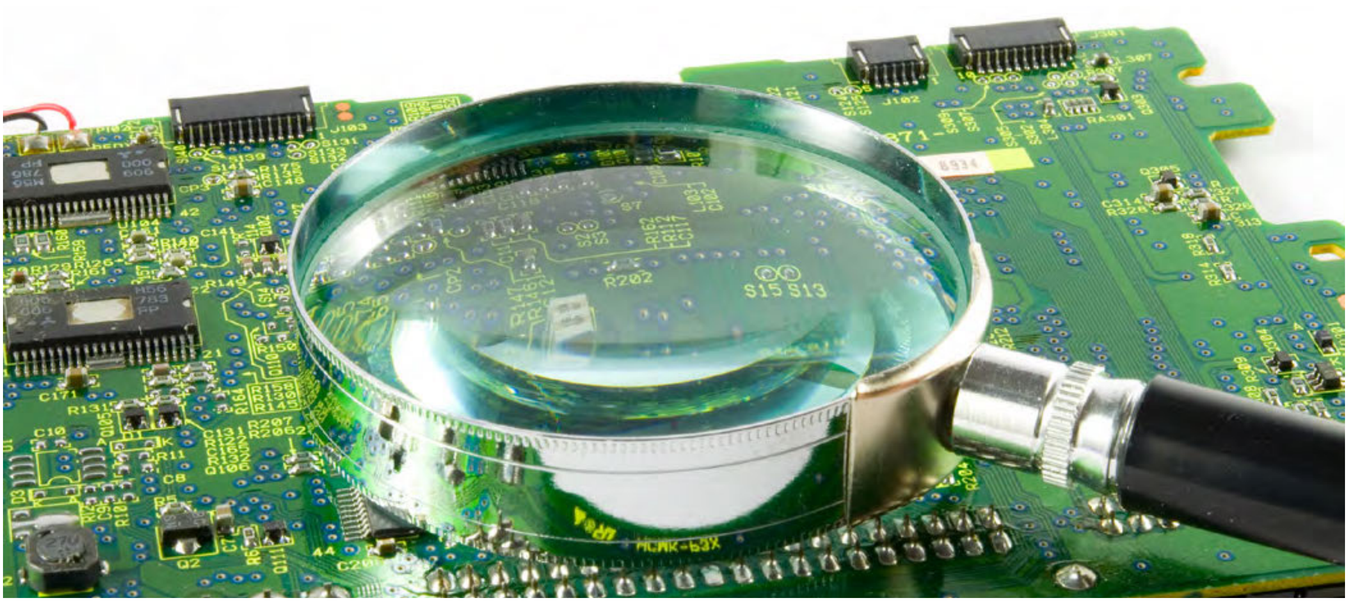
On top of dealing with increasingly complex and higher-density boards, assemblers are also facing tougher requirements such as data traceability, changes in IC packaging structure, embedded substrates and modules, and thermal conductivity, according to our survey.

**Innovation Wish List**

To help address their challenges, respondents are looking for innovations such as better boundary scan capability and better test equipment that find latent defects in electrical testing. From an optical test/inspection, they said innovations such as better lighting and focal plane depth are key. They are also looking for CAD/CAM systems that could suggest the best test implementation, as well as software to economically automate functional test of low-volume production runs.

Meanwhile, the majority of our respondents (64%) say they are planning to purchase new test and inspection equipment this year. Assemblers are looking to acquire equipment such as ICT for high-power device testing, benchtop instruments, SPI, 3D AOI and AXI systems, and RF test systems for their test and inspection process.

This month, we look into different PCBA test and inspection strategies that address some of the key challenges in today's electronics manufacturing and assembly environment. First, we have a study done by Alpha Assembly Solutions' Karen Tellefsen et al., comparing the results from testing two solder pastes using the IPC-J-STD-004B IPC TM-650 2.6.3.7 surface insulation resis-



tance test and IPC TM-650 2.3.25 in an attempt to investigate the correlation of ROSE (resistivity of solvent extract) test methods as predictors of electronic assembly electrical reliability.

Next, I interviewed Keysight Technologies' NK Chari to learn more about the challenges in PCBA testing and inspection, technology and market trends that are driving these issues, and the latest innovations happening in the test and inspection industry to help customers address those challenges. He also discusses best practices that customers should consider to improve their PCBA testing and inspection process.

We also have another technical paper written by Chris Hunt and Ling Zou of the National Physical Laboratory and Phil Kinner of Electrolube. Their article talks about a new, repeatable and controllable approach to condensation testing of electronic assemblies.

Jens Mille and Jens Kokott of Goepel Electronic GmbH, meanwhile, focus on 3D measurement of connectors' swash circumference and embedment depth.

Wei Keat Loh of Intel Malaysia and Haley Fu of the International Electronics Manufacturing Initiative (iNEMI) write about iNEMI's work on establishing package-on-package (PoP) warpage characteristics and understanding the effect of current measurement criteria that potentially address the component board assembly challenges.

In his article, National Instruments' Matej Krajnc explains why electronics manufacturers are shifting from using turnkey ATE solutions to building their own cost-optimized testers based on off-the-shelf instrumentation. He also discusses how modular instrumentation platforms like PXI, which offer the measurement accuracy required for R&D and the speed required for manufacturing test, are helping manufacturers reduce the cost of test.

We also have interesting article from Ahne Oosterhof of Eastwood Consulting, who currently consults for LPKF Laser & Electronics North America, about the challenges of using laser systems for the depanelization of circuit boards. His article provides an in-depth analysis of the various laser system operating parameters to determine the resulting substrate material temperature changes during depanelization.

Carrying forward last month's topic on solder paste printing, Watson Tseng of Shenmao America Inc. and Hsiang-Chuan Chen, Ya-Ching Chuang, Jen-Yio Shiu, and Chang-Meng Wang of Shenmao Technology Inc. spotlights a new solder paste alloy developed for automatic laser soldering processes.

Carl Lincoln of EMS firm Integrated Technologies Ltd has written about overcoming medical electronics manufacturing challenges, and lists the top 10 questions to ask that will help you make comparisons when looking to change your medical PCB manufacturer or are outsourcing for the first time.

In her column SMT Prospects & Perspectives, Dr. Jennie Hwang of H-Technologies Group discusses the fourth industrial revolution—Industry 4.0—and explains its impact on running businesses, producing products, offering services, and living our lives.

Still on the topic of Industry 4.0, Michael Ford of Mentor Graphics takes a look at the most common approaches adopted so far—Industry 4.0, Internet of Manufacturing (IoM), or smart factory projects—and discusses how things are going, what can be learned from the experiences, and how things could be done better.

For his column this month, Tom Borkes of The Jefferson Project dissects the STEM education and presents the real problem that's been going on in the STEM initiative for the past three decades.

Last but not least, Robert Voigt of DDM Novastar continues his series on selecting a selective soldering system, focusing on the programming software needed to optimize production speed.

I hope you enjoy this month's issue of *SMT Magazine*. Next month, we'll feature the "voices of the industry." Stay tuned!

By the way, we are always looking for good, technical content that's relevant to the industry. If you would like to contribute, feel free to drop us a note. **SMT**

**Stephen Las Marias** is managing editor of *SMT Magazine*. He has been a technology editor for more than 12 years covering electronics, components, and industrial automation systems.

# The Fourth Industrial Revolution (Industry 4.0): Intelligent Manufacturing

by Dr. Jennie S. Hwang
H-TECHNOLOGIES GROUP

As the world is pivoting away from the third industrial revolution, what will we face in terms of running business, producing products, offering services, and living our lives?

The last industrial revolution was driven by striking advances in electronics and information technology having achieved enormous economic prosperity and manufacturing automation. So what is the fourth industrial revolution and what does it encompass? Is it gravitational pull?

### The First to Third Industrial Revolutions

The first industrial revolution in the late 18th century used steam engines, which flourished the textile industry and other mechanization systems; the second industrial revolution in the final third of the 19th and beginning of the 20th centuries introduced electrically-powered mass production, creating steel industry, and telegraph and railroad systems. The invention of transistors in 1947 led the dawn of the digital age and information technology, thus the third industrial revolution has offered phenomenal applications of computers and electronic gadgets since the 1970s.

The third industrial revolution propelled the global economic development and the manufacturing advancement by utilizing information and automation technology, making the beginning and the continued progress of the vibrant and fast-paced digital era. As most of us have lived through (and are living in) this era, smart electronics has been proliferating and relentlessly moving toward a higher level of wearability, connectivity and mobility[1].

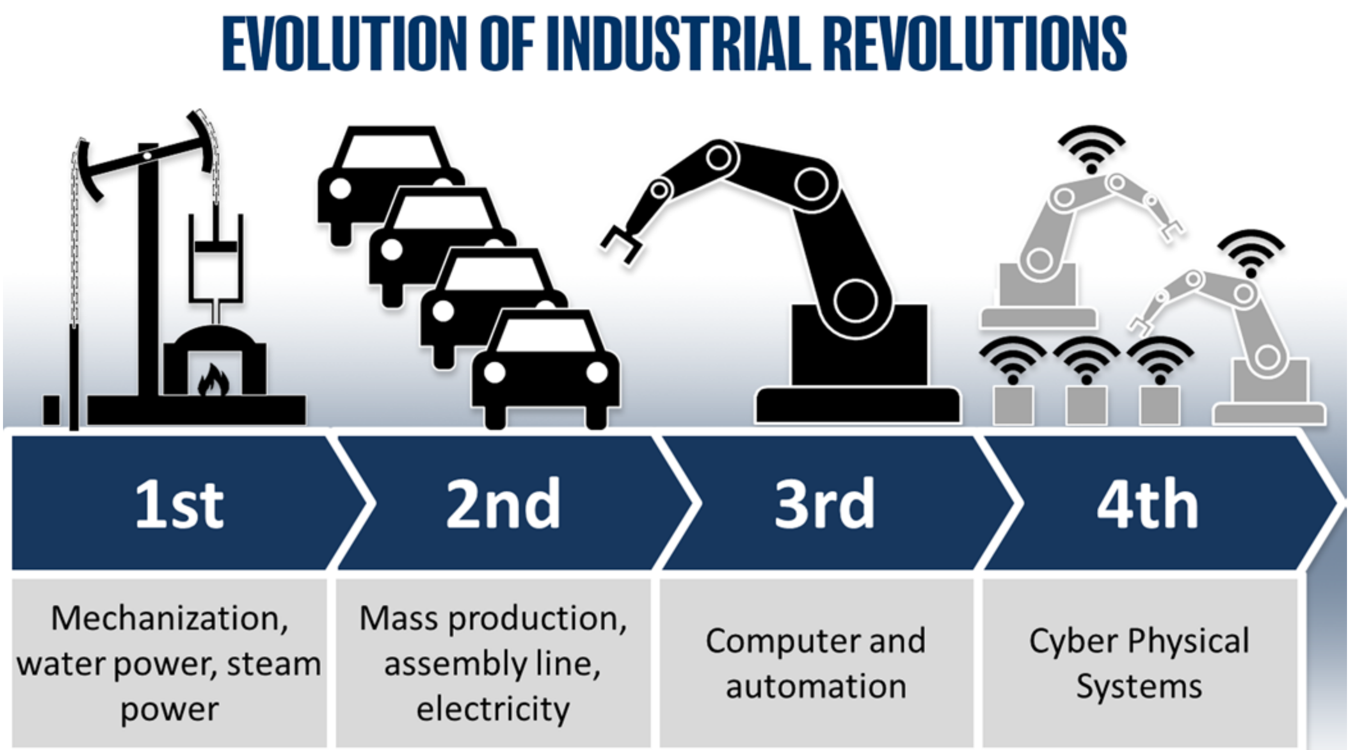


image: Christoph Roser - AllAboutLean.com

Five words speak for the essence of electronics: smart, mobility, connectivity, wearability, and innovation[2]. Innovation has been the name of the game. It spurs an unprecedented growth of exponential technology during the period of the third industrial revolution.

### The Fourth Industrial Revolution

The genesis of the term, fourth industrial revolution, also dubbed Industry 4.0, was rooted in the German federal government's high-tech strategy in 2011. Industry 4.0 will leverage the internet, digital technologies and quantum sciences to drive further into autonomous, intelligent cyber-physical systems.

> "Through the fusion of the physical and the virtual world, interoperability, advanced artificial intelligence and autonomy will be integral parts of the new industrial era."

As Industry 4.0 is evolving, it is fitting to define it as the get-together assembly of cyber-physical systems, cloud technology, internet of things and internet of services, and its integration and interaction with humans in real-time to maximize value creation. Through the fusion of the physical and the virtual world, interoperability, advanced artificial intelligence and autonomy will be integral parts of the new industrial era. In this era, fascinating technological developments are underway or will be pursued in both military and commercial sectors in the U.S. and around the world.

### Commercial Sector—Intelligent Manufacturing

In the commercial sector, rigidity is out, flexibility is in; stiffness is out, agility is in. Sluggishness is out, and swiftness is in. Responding to the evolving new industrial era, delivering customized products with flexible, modular production flow at an optimal economics becomes necessary.

Manufacturing companies need to develop a deep understanding of the technologies, translating business objectives into technology roadmaps targeting at operational efficiency. This will be accomplished by leveraging the machine-to-machine communication, machine-to-human interaction, cloud computing and advanced analytics. For instance, intelligent machines can trigger maintenance processes autonomously and are capable of predicting failures; data analytics aids to detect process inefficiencies, thus reducing production cost.

I cannot emphasize enough that inventory management is imperative to the success of manufacturing operations, and its optimization is paramount to the healthy balance sheet and cash flow, especially for raw-material-intensive businesses. Companies must keep track and control of both days of inventory as well as the actual dollar value of inventory. Doing well in this area mitigates the mishap of production outpacing demand as well as eschews cash flow trap.

Using cyber-physical systems, supply chains will be fully integrated and automated. Cyber physical systems deployed throughout the value chain enable the linkage between data and material flows, creating the complete visibility of the supply chain, in stationary or in transit state. This also facilitates the formulation of reliable inventory forecasts, the avoidance of unscheduled downtimes, and the timely reaction to unexpected changes in production.

Visibility, traceability, predictability and sophisticated simulations, coupled with speed, agility and flexibility are the underlying characteristics of intelligent manufacturing.

### Military Sector

In preparation for the future, the U.S. Department of Defense recently unveiled technology areas that will translate into operational advantages. Deputy Defense Secretary Robert Work recently unveiled five technology areas that will guide future investments in new weapon capabilities as well as drive organizational and operational experimen-

tation as part of the "Third Offset Strategy." The Strategy reflects the Defense Department's new paradigm to strengthen conventional deterrence against potential global threats and adversary nations. The Pentagon will not try to match its adversaries "tank-for-tank, gun-for-gun, missile-for-missile, person-for-person, and instead will offset enemy strengths in other ways...We will reveal for deterrence, and we will conceal for war-fighting advantage," Work said (Inside Defense). It is a dynamic strategy aiming at the dynamic, complex and uncertain environment.

Among the technological "elixirs," the U.S. military will pursue its effort to harness artificial intelligence and autonomy as part of a competition among the world's greatest powers. Secretary Work said, "We have identified what we believe to be the five key technological components of the Third Offset Strategy." The five components are:

- Learning machines that will literally operate at the speed of light; they will change the way we pursue intelligence; they will be utilized for indications and warning; they will be used in cases where human reaction speed is simply not up to the task—specifically in cyber defense, electronic warfare and large-density missile raids.
- Human-machine collaboration, as teaming up human insight with the tactical acuity of human computers, to make the human more effective in the decision space.
- Assisted-human operations, coming online in the commercial sector, such as automotive technology that warns an operator about obstacles when backing up. Such capabilities would evolve to allow decisions to be delegated to a machine. The U.S. military will primarily be interested in wearable electronics—combat apps, new types of different things that the soldier, sailor, airman and Marines will carry and help them fight.
- Advanced manned and unmanned combat teaming, which is happening now and will get more powerful in the future.
- Network-enabled autonomous weapons that are hardened for cyber-attack and electronic-warfare environments.

According to Work, implementing the Third Offset Strategy, which is set to be as part of the fiscal year 2017 budget request, will require "strong, top-down governance," revitalization of war-gaming with more demonstrations and experimentation, and a focus on agility and cost.

**Gravitational Pull**

The fourth industrial revolution epitomizes "gravitational pull" that is set by multiple and complex drivers as well as crosscurrents—expanded globalization, technological explosion,

> "The fourth industrial revolution epitomizes "gravitational pull" that is set by multiple and complex drivers as well as crosscurrents—expanded globalization, technological explosion, digital tools, Internet-centric data flow, global competitiveness, among others."

digital tools, Internet-centric data flow, global competitiveness, among others. As striding toward the fourth industrial revolution, regardless of a particular business strategy, be it a service provider or an agile niche product producer or a low-cost mass merchandise supplier, success in the era of Industry 4.0 hinges on a comprehensive vision coupled with a compelling business model embodied with a decisive strategy and defined core value drivers. To that end, focus areas for future investments can then be identified.

Key efforts are to be made on the collectivity and connectivity of technologies, seamless integration of data, effective use of digital tools, and the vision and continued deployment of new technologies to achieve operational optimization and business excellence. SMT

**References**

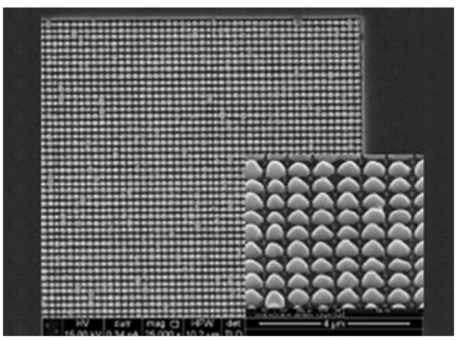
1. Hwang, Jennie. "2013 Year-in-Review," SMT Magazine, December 2013.

2. Hwang, Jennie. "2014 New Year Outlook," SMT Magazine, January 2014".

3. Further readings: "The Fourth Industrial Revolution" by Klaus Schwab, published by World Economic Forum January 11th, 2016.

**Dr. Hwang** is a forward thinker, an international businesswoman, international speaker, and a business and technology advisor. She is a pioneer of and long-standing contributor to SMT manufacturing since its inception, as well as to the lead-free electronics implementation. Among her many awards and honors are induction into the International Hall of Fame—Women in Technology, election to the National Academy of Engineering, YWCA Women Achievement Award, and being named an R&D-Stars-to-Watch (Industry Week). Having held senior executive positions with Lockheed Martin Corp., Sherwin Williams Co., Hanson, plc, IEM Corp., she is currently CEO of H-Technologies Group, providing business, technology and manufacturing solutions. She serves as Chairman of Assessment Board of DoD Army Research Laboratory, National Institute of Standards and Technology (NIST), National Materials and Manufacturing Board, Board of Army Science and Technology, Commerce Department's Export Council, various national panels/committees, international leadership positions, and the board of Fortune 500 NYSE companies and civic and university boards. She is the author of 450+ publications and several textbooks, and a speaker and author on trade, business, education, and social issues. Her formal education includes four academic degrees (Ph.D., M.A., M.S., B.S.) as well as Harvard Business School Executive Program and Columbia University Corporate Governance Programs. For more information, click here.

# New Generation of High-efficiency Solar Thermal Absorbers Developed



Researchers from the Universities of Bristol and Exeter are one step closer to developing a new generation of low-cost, high-efficiency solar cells. The structure is one of the world's first examples of a tri-layer metasurface absorber using a carbon interlayer.

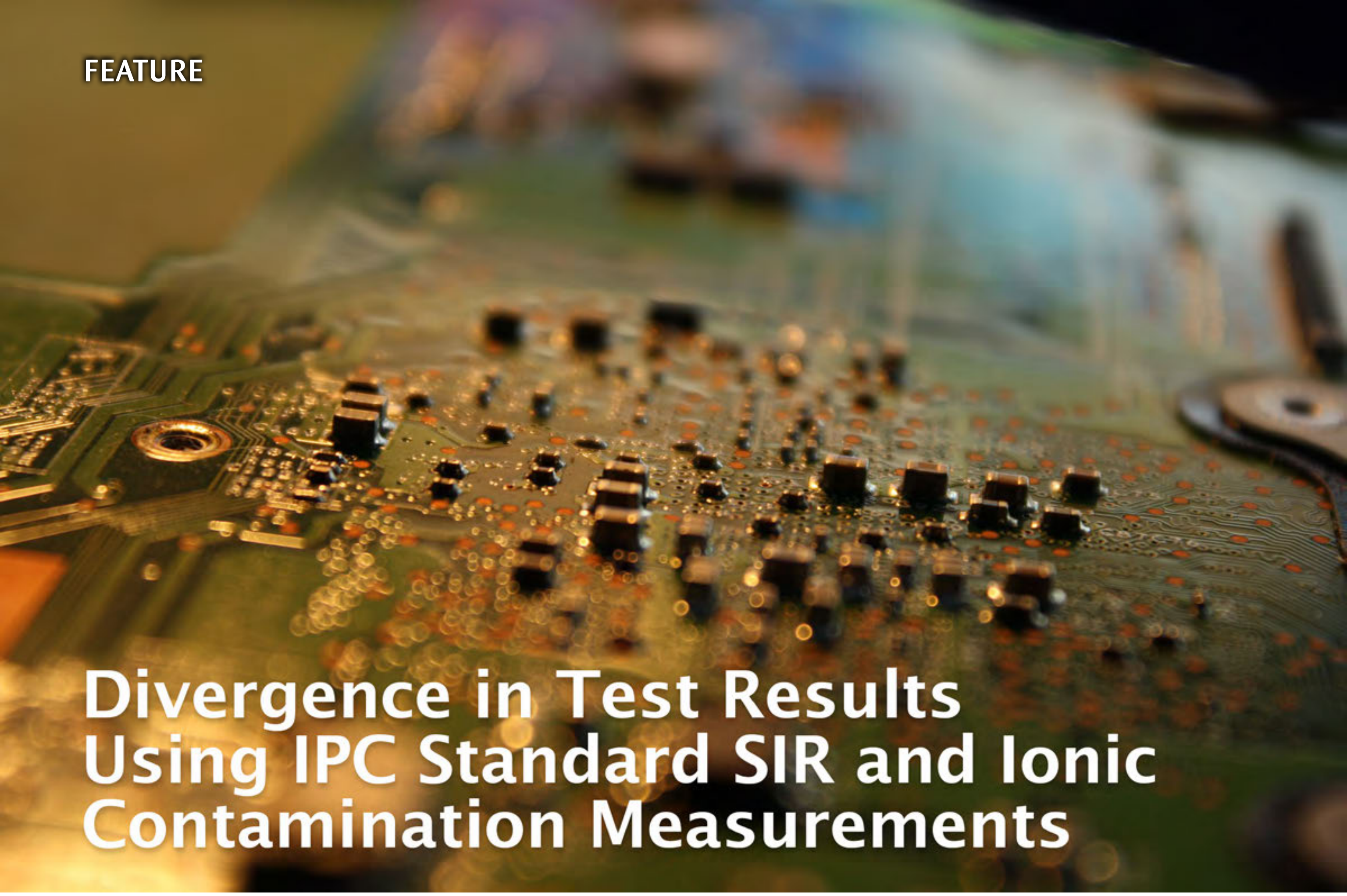
The system, developed by Chenglong Wang, a PhD student in Professor Martin Cryan's research group, uses amorphous carbon as an inter-layer between thin gold films with the upper film patterned with a 2D periodic array using focused ion beam etching. Professor Cryan is the professor of Applied Electromagnetics and Photonics in the Department of Electrical and Electronic Engineering.

The trilayer gold-carbon-gold metasurface strongly absorbs light across the solar spectrum but minimizes emission of thermal radiation from the structure. The use of gold in the research is a first step towards a high temperature metasurface where gold can be replaced by other refractory metals such as tungsten or chrome.

The cell will be used for solar thermal energy applications and has the potential to reach much higher temperatures than simple black surfaces because it can minimise the emission of thermal radiation.

The metasurface has been developed as part of a joint project, led by Dr. Neil Fox, between Bristol's Department of Electrical and Electronic Engineering and Schools of Physics and Chemistry.

The Bristol team have been working with Professor Tapas Mallick from the University of Exeter to develop the low-cost solar concentrator systems.



# Divergence in Test Results Using IPC Standard SIR and Ionic Contamination Measurements

**by K. Tellefsen, et al.***
ALPHA ASSEMBLY SOLUTIONS

Controlled humidity and temperature controlled surface insulation resistance (SIR) measurements of flux covered test vehicles, subject to a direct current (DC) bias voltage, are recognized by a number of global standards organizations as the preferred method to determine if no-clean solder paste and wave soldering flux residues are suitable for reliable electronic assemblies. The Association Connecting Electronics Industries (IPC), Japanese Industry Standard (JIS), Deutsches Institut fur Normung (DIN) and International Electrical Commission (IEC) all have industry reviewed standards using similar variations of this measurement.

Ionic contamination testing is recognized by the IPC as a standard for evaluating the cleanliness of assemblies that have been subjected to a cleaning process. IPC J-STD001F calls for a cleanliness level of $<1.56$ µg/cm$^2$ NaCl equivalent after the cleaning processes. Historically, this threshold originated from the cleanliness specifications of military and aerospace original equipment manufacturers (OEMs). These applications used rosin-based wave soldering fluxes, such as RMAs, and cleaned with now presently banned fluorocarbon solvents. Many of these applications have subsequently implemented water soluble soldering processes. Several automotive and consumer electronic OEMs still use this standard, to qualifying assemblies built with no-clean materials using mixed SMT and PTH assembly technologies.

IPC-TM-650 Method 2.3.25 contains standard test methods for extracting contaminants from circuit boards using heated isopropanol (IPA) / water mixtures. Test method 2.3.25 is commonly referred to as the ROSE (resistivity of solvent extract) test. Previous work[1,2] has shown poor correlation between the presence of extractable, corrosive weak organic acids and results from IPC-TM-650 2.3.25 test results, partially due to the lack of solubility of materials found in no-clean fluxes, and the higher SIR values imparted by rosins and resins in modern no-clean soldering materials.

This study will compare the results from testing two solder pastes using the IPC-J-STD-

004B IPC TM-650 2.6.3.7 surface insulation resistance test and IPC TM-650 2.3.25 in an attempt to investigate the correlation of ROSE methods as predictors of electronic assembly electrical reliability.

**Introduction**

Ionic contamination testing has been traced back to work done at the United States Naval Avionics Center in Indianapolis in the early 1970s by Hobson and DeNoon[3]. This work eventually led to the development of the 1.56 µg/cm$^2$ (10 µg/inch$^2$) NaCl equivalent standard for ionics extracted using an IPA/water mixture. High volume circuit assembly at the time used only wave soldering processes, employing foam fluxers to apply RMA flux followed by a post soldering cleaning process with fluorocarbon solvents.

This ionic contamination limit became part of now defunct Mil Spec P-28809[4] and Mil STD-2000A, but has been carried through versions A through F of ANSI/J-STD-001. This manual procedure has become more automated with the invention of descriptively branded test equipment such as the Contaminometer, Ionograph and Omega Meter. Although these measuring devices improve the efficiency and accuracy of measuring ionic contamination soluble in alcohol/water mixtures, they also increase the amount of ionic material measured[5, 6].

IPC-9202 describes a procedure for qualifying a process for electrical reliability by measuring SIR using IPC TM-650 2.6.3.7 and IPC TM-650 2.3.28 by using the IPC-B-52 test coupon. This coupon is shown in Figure 1. The standard calls for a minimum SIR value of 100MΩ, but only calls for a measure and report of the ionic contamination. The reported ionic contamination then becomes a benchmark for "future trouble shooting or process improvement efforts."

The experiments carried out in this work were designed to use methodology derived from IPC-9202 to determine if it is possible to have a solder paste that passes SIR standard of >100 MΩ, but fails the ionic contamination level of ANSI/J-STD-001f, and determine if a second solder paste fail the SIR test and pass the ROSE test standard.

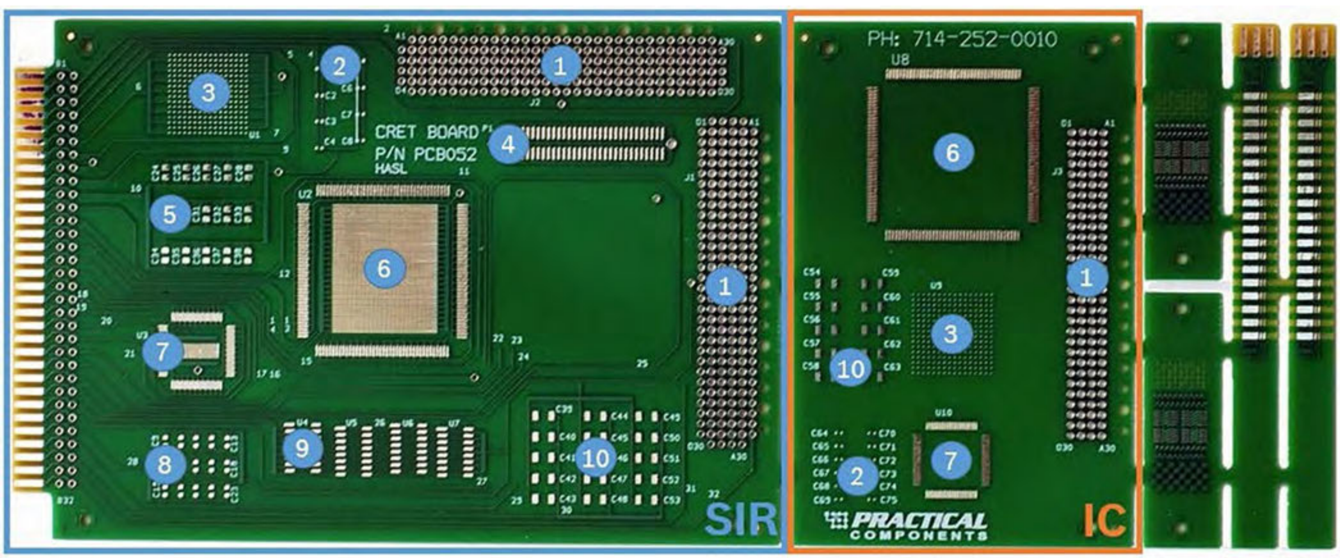



Figure 1: IPC B-52 test coupon comprising a SIR test coupon (SIR) and a section for ionic contamination measurements (SIR). Component ID: 1 – TH connector 4 x 24 pins; 2 – Capacitor, 10 pF, 0402 package; 3 – BGA, 256 IO, 1 mm pitch, isolated; 4 – SM connector IEEE 1386, 2 x 16 pins; 5 – Capacitor, 10 pF, 0805 package; 6 – QFP160, 0.65 mm pitch, isolated; 7 – QFP80, 0.5 mm pitch, isolated; 8 – Capacitor, 10 pF, 0603 package; 9 – SOIC16, 1.27 mm pitch, isolated; 10 – Capacitor, 10 pF, 1206 package.

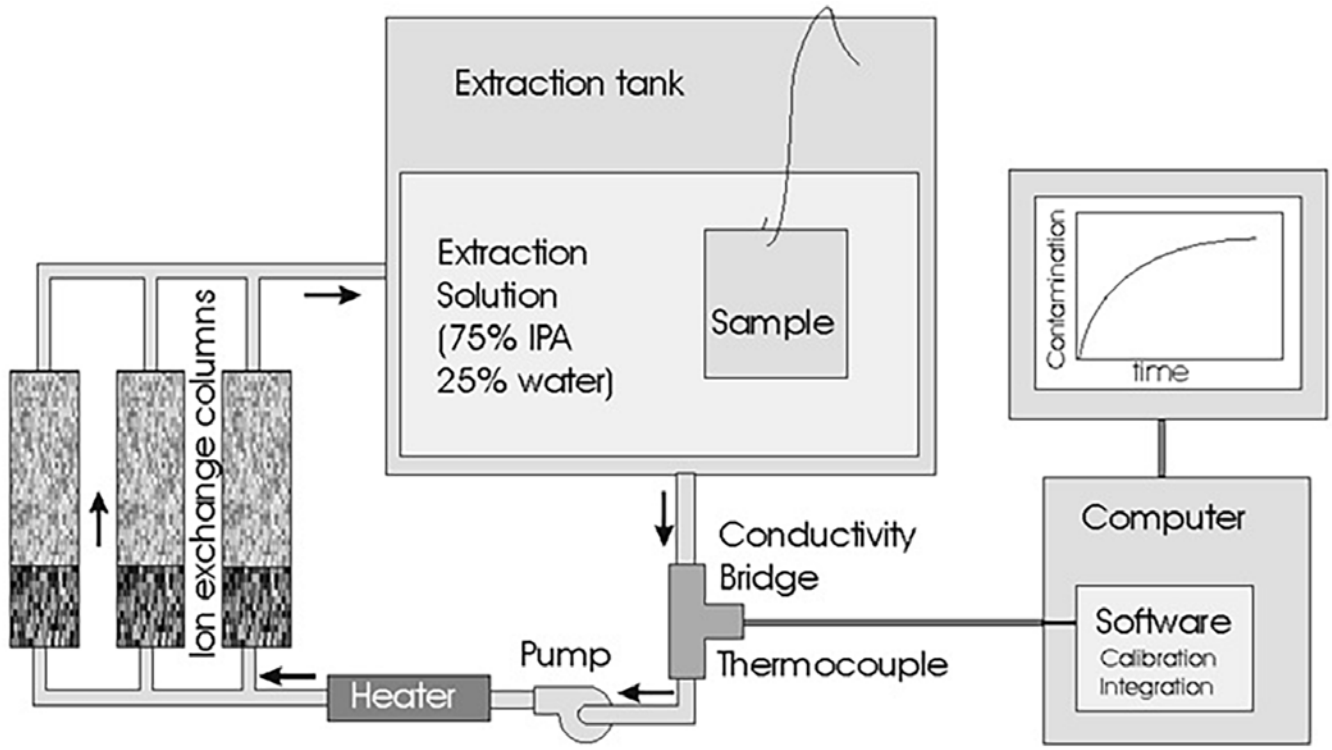



Figure 2: Schematic diagram of the "Ionograph."

## Methodology

Two different SAC305 solder pastes were printed and reflowed on IPC B-52 test coupons (Figure 1). The assembled coupons were broken into two separate test vehicles after the solder pastes were printed, populated and reflowed. The section of the board on the center right was used to measure ionic contamination. The left portion of the test vehicle was used to measure SIR. The four smaller panels on the far right were discarded. A schematic diagram of the Ionograph that was used is depicted in Figure 2. The Ionograph is considered a "dynamic" ROSE measurement in which the extraction solution is continuously passed through ion exchange columns that remove the ionic material in the solution. A conductivity bridge detects ions in solution, and a flow meter measures the volume of solution passing by the conductivity bridge, allowing ionic contamination to be integrated with extraction solution volume.

A second measurement using three IPC-B-24 coupons (usually used for single material SIR measurements) for each of the two pastes was made.

## Experimental Procedure

### *1. IPC-B-52 Coupon Preparation*

Ten IPC-B-52 coupons were processed for each of the two selected solder pastes. These coupons were used as delivered from the board fabricator; no further cleaning was done. The pastes were printed using a 0.125 mm (5 mil) stencil. Positions 2, 3, 5, 7, 8 and 10, as shown in Figure 1, were populated with dummy components. The coupons were then reflowed using an OmniFlo 7 oven with a 1.1 °C/s straight ramp to a peak temperature of 243°C with a time above liquidus of 53 s using a nitrogen atmosphere (600–800ppm $O_2$), as shown in Figure 3.

### *2. SIR Measurements*

The SIR portion of twenty coupons and two unprocessed control coupons were mounted in a temperature-humidity chamber. Teflon-insulated leads were hand soldered to the coupons. The chamber was programmed to run at 40°C +-1°C and 90–93% RH, and a GEN3 AutoSIR was programmed to apply 12V bias and to measure

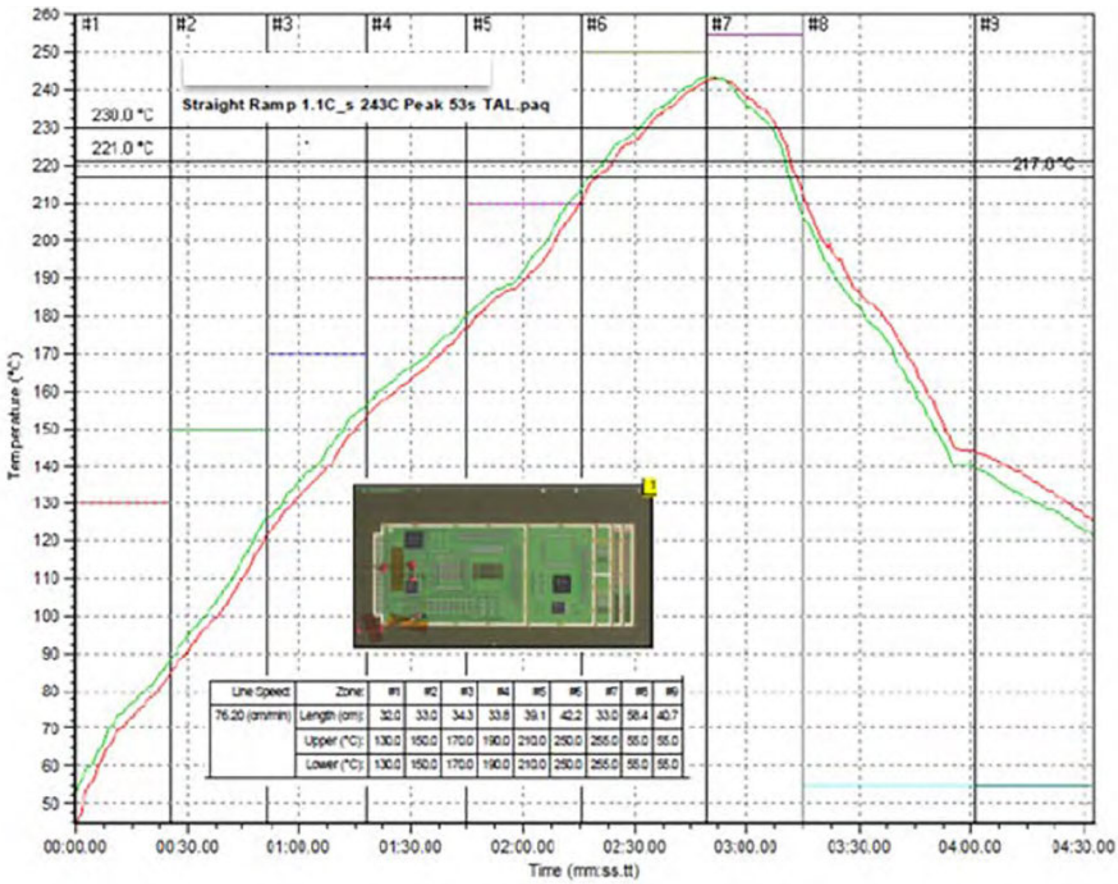



Figure 3: Applied reflow profile comprising a straight ramp to 243°C under nitrogen (1.1 °C/s, 53 s TAL).

SIR at bias voltage every 20 minutes for seven days.

SIR data were recorded for pattern No. 5, 6, 7 and 8 (Figure 1). The boards were mounted in the temperature/humidity chamber and connected to a "Gen3 AutoSIR" instrument for measuring the SIR. The chamber was programmed to record SIR readings at 12 V every 20 minutes. No edge card connectors were used. Teflon-insulated wires, were soldered with ROL0 solder cored wire.

### 3. Ionic Contamination Measurements of IPC-B52-Coupons

Ten IPC B 52 ionics break away with three populated patterns were measured for each of the two pastes. An Ionograph 500M SMD II was used to measure the ionic contamination of each sub coupon. A 75% isopropanol 25% water extraction solution heated to 45°C was used. A dwell time of 15 minutes in the ionograph was used. This time was a balance between complete removal of ionic contamination, versus CO2 absorption increasing the apparent conductivity of the solution from a source other than the test vehicle. A PCB surface area of 65 $cm^2$ was used in the calculations.

### 4. IPC-B-24 Coupon Preparation

#### A. Pre-cleaning

Modified IPC-B-24 test coupons, with bare copper FR4 were immersed in a 75% isopropanol/25% water solution in an Ionograph 500M SMD II. The solution was heated and circulated. The boards remained in the solution until a solution resistivity of >300 ohm-cm was achieved. The boards were then baked at 50°C for one hour.

#### B. Coupon Assembly

The solder paste was printed on three test coupons per paste using a 150 µm (6 mil) sten-

cil. The coupons were then exposed the temperature profile similar to that shown in Figure 3 below using a OmniFlo 7 oven in N2 (600-800ppm O2).

**Results and Discussion**

Log SIR results for solder paste A and solder paste B measured on the leads around the small QFP on the IPC-B-52 coupons are depicted in Figures 4 and 5 respectively. Figure 6 shows the mean Log SIR values for all six patterns measured for both solder pastes. As can be seen from the 7-day test, paste A has a consistent SIR reading of three orders of magnitude greater than paste B. Paste B is a marginal fail if 100MΩ is used as the pass/fail standard.

Figure 7 compares the results for ionic contamination measured on the IC part of the B-52 test vehicles with solder paste A and B. Contrary to the SIR readings, the test coupons processed with solder paste A exhibit an ionic contamination level that were three times larger than solder paste B. The discrepancy is a result of the easy extraction of benign ionics in the alcohol/water mixture from solder paste A, and insoluble contributors to reduced surface insulation in solder paste B. A detailed analysis of the chemical nature of the ionic residues was not

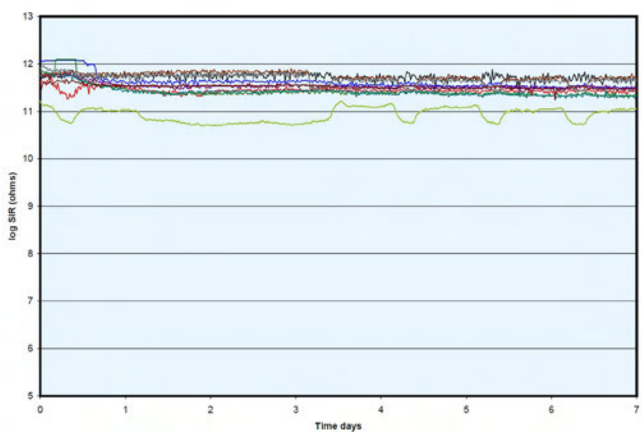



Figure 4: IPC-B-52 SIR test results of paste A at small QFP leads.

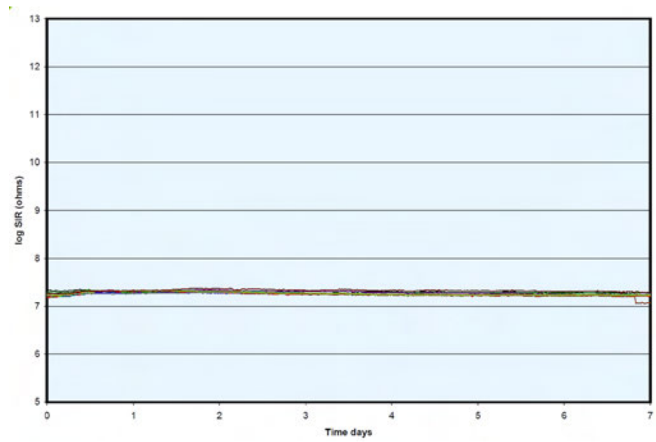



Figure 5: IPC-B-52 SIR test results of paste B at small QFP leads.

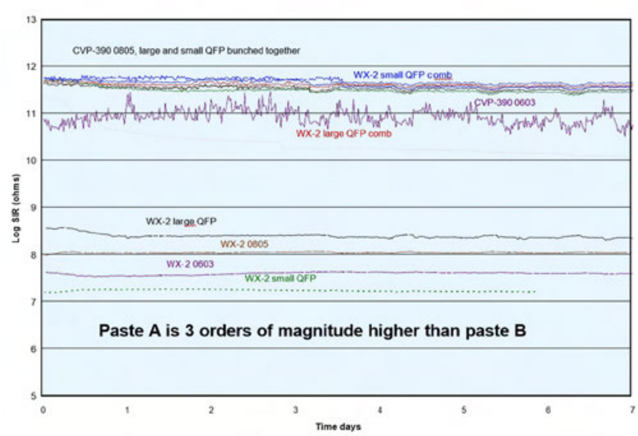



Figure 6: Mean B52-SIR all patterns paste A and paste B.

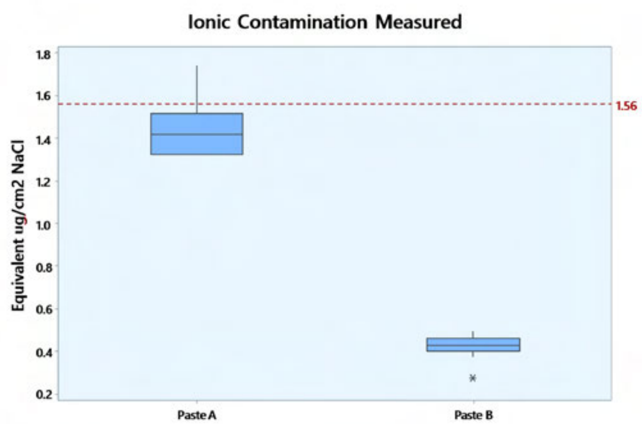



Figure 7: Box plots of ionic contamination measurements of the IC part of B-52 test vehicles processed with solder pastes A and B.

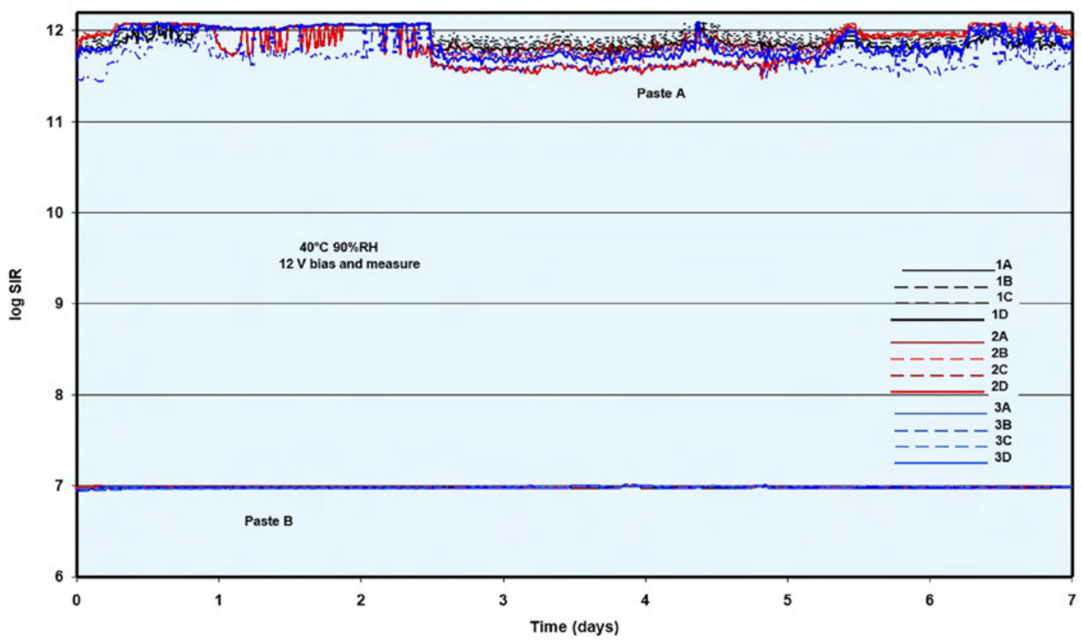



Figure 8: Paste A and Paste B SIR per J-STD-004B/IPC-TM-650 Method 2.6.3.7.

performed. The results are a borderline pass for solder paste A with high SIR values and a pass with a wide margin for the samples that used solder paste that failed to consistently maintain a SIR above 100 MΩ during the constant climate test.

Log SIR per J-STD-004C is shown for pastes A and B in Figure 8. In this case, SIR values are 4.5 orders of magnitude higher for paste A than paste B.

## Conclusions

These divergent test results emphasize why a ROSE test should be used as a relative test to qualify a process, and to use the baseline SIR/Ionic contamination measured using the dual purpose test as a benchmark for "future trouble shooting or process improvement efforts." Test coupons with ionic equivalent measurements just below the 1.56 $\mu g/cm^2$ NaCl equivalent limit used in ANSI/J-STD-001f were shown to have three orders of magnitude greater surface insulation resistance, but still have 3X measured ionic contamination. Thus, the ionic contamination of a PCBA does not predict any reliability of the electronic control unit under high temperature and high humidity conditions. It is highly recommended that the 5-22A task group review and amend ANSI/IPC-J-STD-001f to account for the known divergence in SIR and Ionic contamination results on the electrical reliability if SMT assemblies. **SMT**

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*Note: This article was presented at the technical proceedings of the IPC APEX EXPO 2016.*

## References


1. Seelig, K. "VOC-Free Flux Study-Not All Weak Organic Acids are the Same," APEX 2012 Proceedings.
2. Chan, A.S.L., Shankoff, T.A. "A Correlation between Surface Insulation Resistance and Solvent Extract Conductivity Cleanliness Tests," Circuit World, Vol. 14 Iss: 4, pp.23–26 (1988).
3. Mittal, K.L. "Treatise on Clean Surface Technology," Vol. 1, p.81, (1987).
4. Hymes, L. "Cleaning Printed Wiring Assemblies in Today's Environment" (1991).
5. Tegehall, P-E., "Cleanliness and Reliability," IVF Research Publication 96846 (1996).
6. Crawford, T., "An In-Depth Look at Ionic Cleanliness Testing," IPC-TR-583 (1993).

# Supply Lines Highlights

## China, Trump, and the Future

At NEPCON China, Hamed El-Abd of WKK and I-Connect007's Barry Matties discussed China's fluctuating economy, the impact of the U.S. presidential election, the current state of electronics manufacturing in the region, and the overall craziness of doing business in modern day China.

## Indium's Andy Mackie Named to IMAPS Global Business Council Steering Committee

Indium Corp.'s Andy C. Mackie, PhD, MSc, has been named to the International Microelectronics Assembly and Packaging Society (IMAPS) Global Business Council Steering Committee.

## ALPHA Argomax 9000 Silver Sintering Preforms Wins Prestigious Award at JPCA Show

Alpha Assembly Solutions' ALPHA Argomax 9000 Silver Sintering Preforms won the award under the materials category of Sangyo Times.

## Goepel Free Webinar on Flexible Integration of AOI Systems into the THT Process is Available on Demand

The new GOEPEL webinar, "Individuality Desired? Flexible Integration of AOI Systems into the THT Process," is now available on demand.

## Universal Instruments to Distribute Mentor Graphics Production Plan Tool for Fuzion SMT Platforms

Universal Instruments will offer Mentor Graphics' Valor Production Plan tool to users of Universal Instruments' Fuzion surface mount technology (SMT) placement platform.

## Electrolube's FPC Gains UL94V-0 Approval

Electrolube's new Conformal Coating product (FPC) was specially developed to resolve a number of longstanding problems relating to coverage and connectivity experienced by a specific user of surface modifier materials.

## BTU Continues Advanced Research in Electronics Assembly

BTU International Inc. has renewed its membership in the Advanced Research in Electronics Assembly (AREA) Consortium, established by Universal Instruments' Advanced Process Laboratory (APL).

## Rehm Expands Sales and Services Network

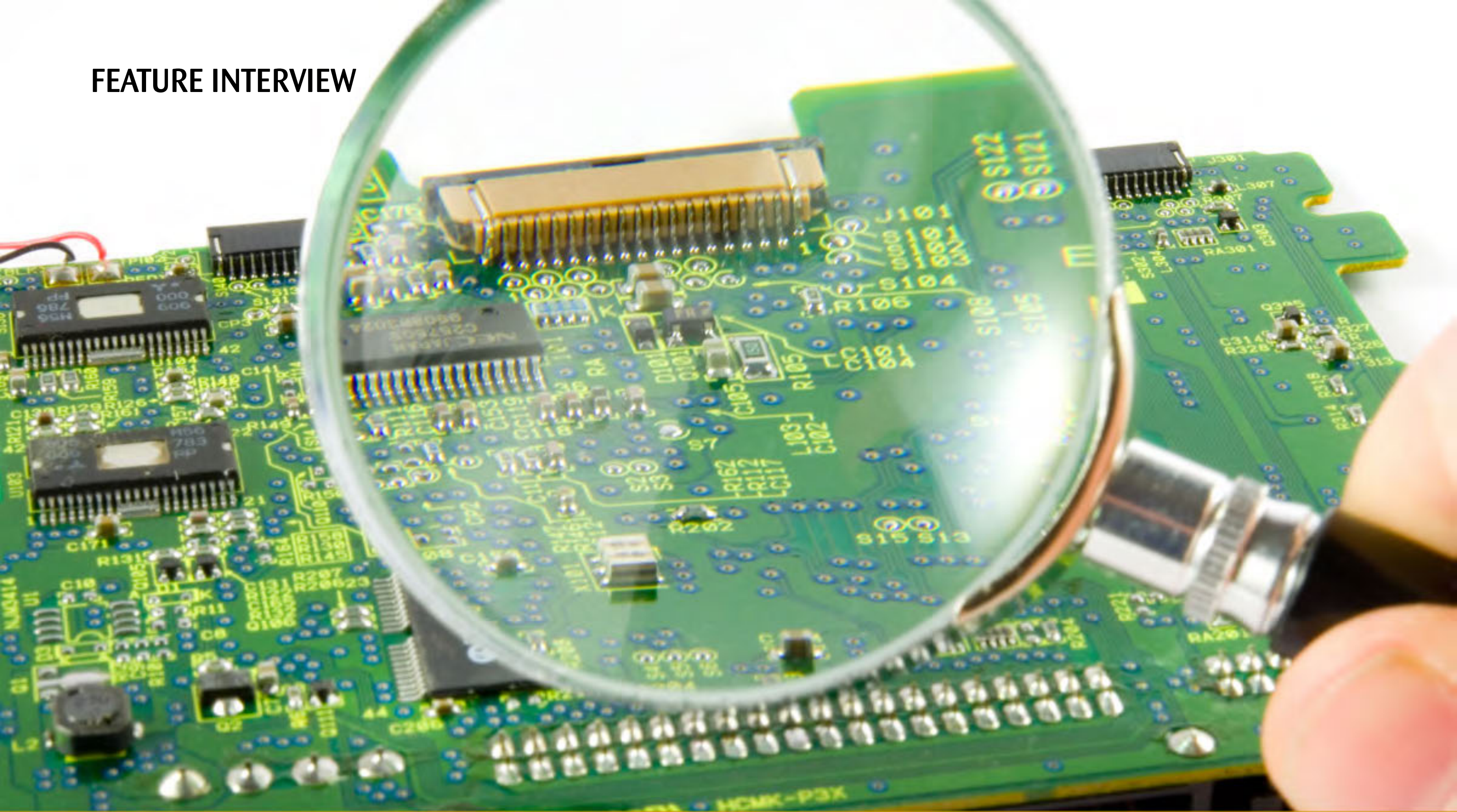
Rehm Thermal Systems has added two new representatives for Sales Germany South East and Sales Central Eastern Europe, expanding its worldwide network for sales and service.

## Dymax Introduces Multi-Cure 9451 Conformal Coating

Dymax's newest conformal coating, the Multi-Cure 9451, is designed to enhance security on PCBs.

## Speedprint Moves to Direct Sales and Customer Support in Germany

Speedprint Technology is investing in new infrastructure, resources and personnel in Germany. Starting this month, the company will deliver direct sales and support to its customers in the country, and across other German-speaking regions.



# Addressing New Testing & Inspection Challenges

**by Stephen Las Marias**
I-CONNECT007

In an interview with *SMT Magazine,* NK Chari, marketing director for manufacturing technologies at the Electronic Industrial Solutions Group of Keysight Technologies, talked about the challenges in PCBA testing and inspection, tougher requirements for testing, and the need for functional testing.

He also mentioned some best practices to consider to improve the PCBA testing and inspection process.

***Stephen Las Marias: What are the greatest challenges that your customers face when it comes to PCB assembly testing and inspection?***

***NK Chari:*** Electronics manufacturers continue to face challenges for PCBA test (i.e., they want to test as many components and processes as effectively as possible at the lowest cost). Their challenges are compounded by the type of technologies and products they are working on. For instance, we are seeing more RF integration or high-speed component into products. These are shielded components, thus, making it very difficult to do board-level testing.

***Las Marias: Are there new or tougher demands and requirements from your customers for testing? If yes, what are they?***

*NK Chari*

***Chari:*** With the advent of the Internet of Things, these PBCAs have become even smaller, and manufacturing volumes are not necessarily very high. Hence, customers have to optimize their test strategy for a mix of medium volume, high-mix, high-complexity production environment. At the same time, new test access challenges continue to surface, with developments like USB 3.0 and integration of higher-speed signals, so the boards can no longer host test pads. Customers have to think of new methods of testing, such as embedded test.

***Las Marias: What technology or market trends are driving these issues?***

***Chari:*** Concurrently, increasing labor costs are driving manufacturers to really think about, and start adopting automation for smart factories to be in place so that they can maximize their resource utilization and improve their yields and performance. The drive towards Industry 4.0 will mean looking at integrating the entire manufacturing process, from design for test to automation. With costs going up considerably, we can see the trend of our customers manufacturing closer to their end markets. For instance, Mexico manufacturing for the American markets and Europe for the European markets. These will put new demands and requirements on manufacturers as they will need common global test processes that can be used across different sites worldwide and more automation.

***Las Marias: What innovations in test and inspection technologies are happening to help customers address these challenges?***

***Chari:*** From a board test stand point, apart from driving automation in board test, Keysight's new Mini In-Circuit Tester is compacting test capabilities into a compact, powerful form factor, and it can be enabled for parallel testing to offer excellent test coverage and increase throughput for handling smaller boards used in IoT products. We are trying to enable more embedded tests with our boundary scan technologies and are continuing to improve our vectorless test performances to help manufacturers detect faults on much smaller devices. We are also working on innovations using XML technology to help our customers connect better as they gear towards Industry 4.0.

These innovations are highly appropriate for various markets, such as the automotive sector, where we see customers testing multiple panels simultaneously, especially for sensor boards. These are small form factor boards similar to IoT boards where you can run multiple parallel tests. Keysight is continuing our investments to push test coverage for new IoT and wireless products such as 5G Analysis Reference Solutions, EXM IoT Reference Solutions.

Another area of Keysight's focus is modular test technologies, which will help manufacturers standardize their test strategies while providing flexibility of reusable modules instead of expensive customized systems.

***Las Marias: With all the common test stations built into a typical SMT line—bareboard testing, solder paste inspection, AOI, X-ray inspection, and ICT/flying probe—why is there still a need for functional testing?***

***Chari:*** OEMs and contract manufacturers continue to see the addition of test stations as one way to improve their test coverage. However, we believe new technologies provided by in-circuit test, embedded tests with boundary scan are providing very high value where it's common to see extremely high functional test yields of over 99 % with the test coverage provided by in-circuit test. This enables customers to reduce the functional test needs, especially at the board level. However, functional test is still needed at the assembled product level because it's the only way to validate and verify the performance of a finished product in an "in-situ" environment to make sure it still operates as it was designed to when operating alongside other functions in a system. Board level functional test is very useful in areas where coverage is weaker with in-circuit or inspection. Keysight continues to offer functional test solutions in a number of industries which continue to see that need for performance validation.

***Las Marias:** It is now an accepted fact that ATE can be integrated into an automated electronic assembly line. However, testing in an automated environment provides new challenges, or opportunities, for both the ATE vendor as well as the end user. Having said that, what are the factors to consider before selecting a test/inspection vendor and implementing a functional test strategy?*

***Chari:*** This is an interesting question. There are multiple factors to be considered when selecting an appropriate test vendor to implement a functional test strategy. Firstly, the measurement science is a very critical base component which have to meet the needs of the products to be tested. Secondly, you need to look at the reliability of the solution, because in manufacturing, you don't want failures, you want your test solutions to be running effectively for long periods of time, with the ability to identify product faults more effectively. Thirdly, you need a good strategy for fixturing and connecting the tester to the devices under test. For that, you have to be aware if your test vendor has considered this, and has the ecosystem to support your test needs during implementation.

***Las Marias:** What best practices should customers consider to improve their PCBA testing and inspection process?*

***Chari:*** One of the best practices for improving PCBA testing starts with DfT—design for test. You need to plan for the test and enable the test. Keysight has recently introduced some very good DfT tools for boundary scan, which customers can deploy. This is very critical in order to have the most effective PCBA testing processes. The second best practice is to try and standardize your test strategy, especially for functional tests. Many customers like to develop custom solutions for every product, and this does not allow reuse. Innovative customers have created standard test platforms which can be reused for different applications. This also allows customers to plan their test assets more effectively. For instance, Keysight has a functional test solution for automotive based on PXI. We have helped leading automotive customers implement such standardized functional test platforms for their long term success.

***Las Marias:** What are some of the mistakes you've seen others in your industry make that you're determined to avoid?*

***Chari:*** In their desire to save costs, sometimes industry participants may compromise on their test strategy, which becomes a costly mistake. Cost of test is a small component compared to cost of customer dissatisfaction upon finding defective products. Thus, it is very important for the industry to avoid using strategies which compromise test in their pursuit to reduce cost. We can reduce cost of test via various other techniques such as automation, improving test coverage, integrating more testers into a single test environment. For instance, you could test a product with a manufacturing defects analyzer which provides basic testing, but it may not catch most of the defects found in the industry today. You could use an in-circuit tester and combine it with some functional test capabilities and multiple test stations, thereby reducing your cost of test, and enabling better quality.

In the very cost-competitive consumer products sector, we have seen some customers relying on inspection and functional tests, only to experience defects escaping which lead to costly warranty issues. They have since re-introduced in-circuit test, which is a very viable and cost-effective quality assurance tool. Compromising on test is a mistake—the cost of escapes as well as the loss of customer faith and satisfaction will always outweigh the cost of test.

***Las Marias:** Where is the test and inspection industry headed? What is your outlook for the industry?*

***Chari:*** The test and inspection industry is a mature industry with a few strong players. The industry will continue to be challenged by new technologies such as the Internet of Things, Industry 4.0, connected cars and 5G. With our strong focus on R&D and immense real-time experience in working alongside our customers, Keysight is gearing up to address these technology challenges. **SMT**

# Industry 4.0: Making the First Move

**by Michael Ford**
MENTOR GRAPHICS

After two or three years of hearing about Industry 4.0, many companies now have active Industry 4.0, Internet of Manufacturing (IoM), or smart factory projects. In each case, different approaches were taken that appeared to best fit the project requirements and that would deliver the intended benefits versus the cost and effort investment needed. Like a game of chess, the first move can be the most important. Let's take a look at the most common approaches adopted so far, and check in to see how things are going, what can be learned from the experiences, and how things could be done better.

The earliest adopters of any new idea are often motivated by more than simply a provable return on investment. The search is on for the proof of concept, to show industry leadership, and to move toward a technology that in the future should bring future competitiveness. The company size, allocation of IT resources, the systems and machines currently in use, whether OEM or EMS, and the sector in which the company is doing business determine the approach to be taken. These approaches can be more or less summarized into the following categories:

1) In-house development
2) Application of an existing generic standard
3) The machine vendor environment
4) Middleware
5) An established MES solution
6) The application of OML (Open Manufacturing Language).

However, there is no best solution. Each of these are valid solutions in certain conditions, and we have to remember that each represents a pioneering attitude that only the most progressive of companies have been able to consider. Looking at what might be the average experience today within each of these categories of solutions has flagged some interesting issues and potential solutions.

**In-House Development**

The headline stories for smart factory internal development projects come from Foxconn and Flex, who each presented their achievement of a model smart factory at the recent IoM event in San Jose and at the IPC APEX EXPO in Las Vegas, respectively. The largest EMS companies in the world are among the first adopters to attract new business and reduce operational costs. In both presentations, their results were compelling. The achievement of linking equipment their internal systems and the use of the resultant information seems perfectly in line with their expectations. Even for companies of this magnitude, one of the key challenges was acquiring data from all of the different processes on the shop-floor. Having considerable purchasing power at their disposal, they were able to work with machine vendors to mutually

work out the communication on a specifically agreed basis, which appeared to be unique for each vendor

Significant development resource is needed in this instance, which perhaps is acceptable for companies of this size. But what about the reliability and the degree of on-going maintenance, as older machines are phased out and newer automation introduced? The IT resources have to be maintained indefinitely, as do the close tie-ins to the machine vendors who cooperate. This is perhaps the most expensive way to achieve shop-floor communication, through "brute force," with the underlying expectation that costs will reduce as communication capabilities and standards improve. Both Flex and Foxconn are to be commended in their achievement, which to the rest of the industry may seem like a fairy tale, but is in fact real, with real associated benefits. What is less clear so far is how these benefits compare to the initial and continued investment of the projects.

"Significant development resource is needed in this instance, which perhaps is acceptable for companies of this size. But what about the reliability and the degree of on-going maintenance, as older machines are phased out and newer automation introduced?"

**Application of an Existing Generic Standard**

Standards such as CAM-X and SECS-GEM were introduced about 15 or 20 years ago, a time when SMT operations were a lot simpler and more rigid than they are today. In particular, the IPC-sponsored CAM-X was the first real standard that featured an infrastructure, a protocol, and, to some extent, a definition of standard machine events. The attraction of CAM-X to some companies was enough of a trigger to start them looking at the standardization of shop-floor communication. All seemed to go well for a short time, until CAM-X had some critical weaknesses in the network bandwidth required to support a wasteful infrastructure and protocol and in the ability to support anything beyond the simplest of commonly defined event attributes.

Rather than continue to work to refine the standard, the IPC seemed to let it go as commercial entities sprung up, offering hardware and software solutions based on CAM-X and customizations, which meant that CAM-X was no longer the standard it was meant to be. Instead of every process getting connected as standard, significant amounts of customization were needed on top of the purchase of what were becoming proprietary solutions. This situation seems to have "poisoned" the market away from believing that a real, complete, and open standard could ever exist.

If the IPC could not do it, then who could? Key companies who invested heavily in these broken standards now find themselves with momentum but going nowhere. Once again, commercial entities have come in to take advantage of the situation, offering upgrades to better and more modern protocols, such as XMPP, which although superior in many ways, is seen to be somewhat unreliable in their definition, already with a multitude of variations. The result is an endless pattern of returning to square one; as new equipment comes in, communication capability needs development, with endless maintenance, a real and substantial revenue stream for the commercial providers of solutions based on older standards.

However, the choice to implement the standard is still smart, with benefits achieved before the Internet of Manufacturing was ever conceived. These companies are the true pioneers of the industry, and are the ones likely to get arrows in their backs as history shows. Respect is due to the many people and companies who made it happen; but they must now be thinking that they are like aircraft, endlessly circling the airport, unable to find a way to land.

### The Machine Vendor Environment

The issues around the so-called standards of the industry seem like an investment too large to justify for many other companies, perhaps suited to those larger companies who could afford to pioneer. As events unfolded, machine vendors realized that customer demand for machine-communications-based functionality was growing, without a clear solution. This initially brought unwelcome pressure on the machine vendors to supply data to customers in a myriad of different formats. The larger machine vendors have been able to turn this into a revenue opportunity. The proposal of their proprietary standard by the machine vendors to their customer sounds attractive, with so much information and control available, including now many Industry 4.0 and smart factory functions. The benefits from such things as closed-loop process adjustment, adaptive test, predictive maintenance, and material management, all based on live machine events is compelling, with real demonstrable benefits. The cost of the solution is simple to understand and maintain.

However, the downsides are that the adoption of the solution establishes a dependent relationship between the customer and the machine vendor and that the solution is unlikely to ever be expandable beyond the machine domain. Material management, for example, may only apply to the kitting or preparation area of materials for the SMT machines, rather than complete materials for the factory, and exclude materials for mounting or assembly operations, as well as repair, of which need to be managed preferably with just one site-wide standard operation. Extending the machine-vendor-driven solution to cover or integrate into other factory operations and systems is difficult and may never be addressed.

### Middleware

Rather than working directly with one or more machine vendors' proprietary standards, the use of "middleware" may help to fill the gap between higher level manufacturing systems and machines on the shop-floor. The middleware package is likely to be a productized piece of an established piece of software from a solution provider so that a reasonable range of machines are supported. Extending the support of machines to those not currently supported may be an issue. The degree of data standardization and completeness also would be an issue because the structure would be orientated and limited to the original intention for the use of the data, making it difficult in many scenarios for full system integration. With the dependency on a single provider for all machine interfaces and support, the established manufacturing execution systems (MES) solution might be more practical.

### An Established MES Solution

For those companies who look for a complete factory solution, ironically they have to compromise on specific machine connectivity. Few, if any, generic MES solutions are able to directly acquire machine data and interpret events into meaningful information. The real cost of MES, the addition of many manual operations for data collection, is a bottleneck to smart factory solutions. Several companies now provide better linkage to machines such as the most popular SMT placers, but they are still an extension of a generic interface that is not sufficient to capture the true nature of events or be able to piece together the detail of the events that occur. For simple use, this is not too much of a problem, but far from the goal of providing the kind of functionality that a true Industry 4.0 or smart factory is really about. The generic MES solution is weak where the majority of materials are assembled.

“Few, if any, generic MES solutions are able to directly acquire machine data and interpret events into meaningful information. The real cost of MES, the addition of many manual operations for data collection, is a bottleneck to smart factory solutions.”

Some MES solutions that have originated from the SMT environment are available with built-in sophisticated machine interfaces. They have been somewhat successful at gaining true visibility of the SMT and related processes. However, because of the vast variation in the types of post-SMT processes, the same level of detail

> Some MES solutions that have originated from the SMT environment are available with built-in sophisticated machine interfaces.

for data collection from back-end processes has not been possible, beyond the simpler data capture, which has left these processes neglected. Companies adopting the generic MES approach have found themselves stuck with an expensive system performing at a general level and little opportunity for advanced projects such as smart factory operation.

**The Application of OML (Open Manufacturing Language)**

The new OML standard was announced in February 2016, intended to create the communication backbone for the Industry of Manufacturing and be the enabler of Industry 4.0 and smart factory operations. Strictly speaking, because OML is new, not a category of existing approaches. OML can be applied to all other categories of solutions discussed so far, providing easier and cost-effective ways of achieving the desired goals in the ways that make most business sense. Let's consider how this works in each case.

**In-house Development and OML**

We heard from the largest companies that, even for them, the key difficulty that they had in their smart factory projects was machine communication. If they had OML, the IT teams would have been able to work with only one format of communication, no matter which machine, robot, manual process, or other operational event was being captured. Cooperating machine vendors would have been able to develop just one interface within each of the machines needing communication, which then would be available for all other customer projects. This works out then to be much more cost-effective for the larger EMS companies as well as for the machine vendors. The time-scale to complete the project would also have been reduced by an estimated 50%. Follow-on sites after the initial smart factory showcase could then go-live for a fraction of the cost and lead-time.

Fortunately, it is not too late. Starting a project today to retro-fit the smart factory showcase with OML represents a small amount of additional work for the EMS companies and the machine vendors compared to the cost of repeating the exercise of smart factory conversion for other sites using the previous method.

**Replacement of an Existing Generic Standard with OML**

The design of OML is intended to be an upgrade to existing standards such as CAM-X or SECS-GEM, etc. The process and architecture of exchanging data using the older standards can easily be rewritten and replaced using OML. Although this requires some time and effort, OML brings many upsides. The level of detail and the breadth of scope for data collection using OML can be greatly enhanced compared to the old standards. As new machines and robots come into the market and are introduced into manufacturing, where machine vendors have chosen OML as their IoM language, they simply plug into the existing smart factory structure. In so doing, the values and opportunities of the system are greatly enhanced, while the cost of ownership and support is greatly reduced.

Now is the time to make the switch. OML was created specifically for manufacturing, with internal definitions to provide normalization of information to the level of detail that can describe the complete factory operation, especially the intricate and difficult to understand workings of SMT placement machines. Today, these machines have multiple dimensions of operation, for example, multi-heads, multi-modules, multi-lanes, multi-robot, etc., all of which make

them the most sophisticated machines to understand, which is nearly impossible without the use of OML.

### The Machine Vendor Environment and OML

The limitations of machine-vendor-driven solutions are frustrating. As detailed and potentially valuable as they are, without the ability to expand the solutions beyond the machine environment means that factory-wide benefits, such as true Lean materials, visibility and control of shop-floor product WIP, routing and schedule, etc., are generally automatically excluded. With an OML connector to the machine vendor environment, all of the benefits obtained from the use of the machine-vendor solution can continue to be used, while providing the opportunity to connect all other processes and operational events from the whole factory. Where existing single machine-vendor-based solutions are in place, a truly connected factory can be created without losing value from an existing investment. Expanding machine-vendor-provided solutions with OML will become much easier as machine vendors produce the OML connector as a standard. As many such machine vendors come on-board with OML is a good time to make the request.

“Expanding machine-vendor-provided solutions with OML will become much easier as machine vendors produce the OML connector as a standard.”

### Middleware with OML

The middleware solution provides multiple ways to collect data from machines and other processes, including a requirement to integrate the middleware into existing factory applications. OML represents a great opportunity for middleware providers to expand their limited offerings to more machines, especially as they offer native OML interfaces. The middleware should then be able to offer OML as an output, providing a standard link for higher level systems and thus reducing the cost and work needed. In this way, site-based software solutions can easily gain access to data from machines, processes, and operations through the middleware where value may be added or directly. Perhaps this progression makes the middleware redundant as value is realized in the early stages of the smart factory.

### An Established MES Solution with OML

Investment in MES solutions, as well as ERP and other site-based software solutions, represents a costly capital investment. In addition, the momentum of the operation of the factory based on the system can mean that changing from one EMS or ERP solution to another has significant costs, greater than the cost of the software. Rather than executing a change in these systems to realize improved solutions, OML can provide information to enhance the operation of legacy systems through one single, simple interface. The availability of accurate and timely information can bring a step-change increase in performance and value from existing systems, which currently are compromised by lack of visibility of what is happening across the shop-floor. OML is ready today to bring the key information to existing systems, reducing cost of ownership while increasing value.Overall, OML is a unique and critical enabler, not only for today’s anticipated Internet of Manufacturing-based Industry 4.0 or smart factory systems, but the specification can equally be applied to all cases of existing systems on the shop-floor to drive expansion, improvement, and cost-effectiveness. **SMT**

*Become a “fast follower,” as a member of the OML community. Registration and downloading the OML specification is free, so becoming an OML development partner today is easy.*

**Michael Ford** is senior marketing development manager with Mentor Graphics Corporation Valor division. To read past columns, or to contact the author, click here.

# Condensation Testing: a new approach

**by Chris Hunt and Ling Zou,**
NATIONAL PHYSICAL LABORATORY, AND
**Phil Kinner,** ELECTROLUBE LTD

Conformal coatings are applied to protect electronic assemblies from adventitious environmental factors, which include, corrosive gases and fluids and high humidity. Whenever there is a significant level of humidity, there is always the opportunity for parts of the assembly to drop beneath the dew point, thus resulting in the formation of condensed water on the surface of the assembly, which can significantly reduce the insulation resistance of the boards surface, resulting in malfunctioning electronics.

While the characterization of coating performance under high humidity conditions is detailed, in well accepted IPC and IEC standards, the performance and testing under condensing conditions is not so well developed.

This situation largely reflects the hardware challenge. Most humidity chambers are designed to achieve stable, well controlled humidity and temperature conditions, but none of these offer condensing options. Therefore, the user has to improvise. A common approach to attempt to achieve condensing conditions is to ramp at a fast enough rate to cause condensation, a feature the humidity chamber designers have by and large, successfully managed to remove. Alternatively chambers run very close to 100% relative humidity and hence at this condition condensation will occur in various parts of the chamber. An immediate drawback of these approaches is that chambers of different designs will perform differently, and will be sensitive to small drops in cooling performance.

There are many alternative approaches to achieving condensation, and these are described in ISO, IEC, ASTM and others, and commonly attempt to drive a chamber into producing condensation, against the anticipated use condition, and hence sensors in the chamber detect the additional moisture and will work to reduce the humidity level to the required setpoint. Thus, the level of experimental control will be very dependent on the chamber perfor-

mance, and variability across chamber manufacturers can be expected.

A new approach has been developed where the test board is mounted on a substrate whose temperature can be independently controlled without changing the ambient condition. Thus, the temperature of the test board can be depressed below ambient to any desired point and hence, produce condensation at different levels. It is then, therefore, straightforward to cycle between condensing and non-condensing conditions on the test board in a constant ambient environment. The technique has been demonstrated to be repeatable and controllable, with the user able to select a temperature differential that matches their worst in-use conditions, or to understand the performance of their system under a range of condensing conditions.

The data for a range of conformal coatings are presented, and correlated back to the conformal coating material type, and coverage and thickness by cross-sectioning.

**Introduction**

Condensation is the change of physical state of matter from the gas phase to the liquid phase. It is most often caused when gaseous matter is in contact with a substrate that is at a lower temperature. The temperature at which condensation will form is known as the dew point. The dew point is the temperature at which the water vapor in a sample of air at constant barometric pressure condenses into liquid water at the same rate at which it evaporates. At temperatures below the dew point, water will leave the air. The condensed water is commonly called dew when it forms on a solid surface.

All things being equal, as the temperature falls, the relative humidity rises, reaching 100% at the dew point, at least at substrate level. The dew point temperature is never greater than the ambient temperature, since the relative humidity cannot exceed 100%.

The dew point then, is the saturation temperature for water in air, and the dew point will be dependent on the relative humidity. A high relative humidity implies that the dew point is closer to the current air temperature. Relative humidity of 100% indicates the dew point is equal to the current temperature and that the air is maximally saturated with water. When the moisture content remains constant and temperature increases, relative humidity decreases.

Conformal coatings are thin, polymeric coatings, intended to preserve the condition of a printed circuit board (PCB) under a wide range of operating environments, including high humidity, corrosive gases, dust and other contaminants.

Conformal coatings are often evaluated in high humidity environments, typically 40°C/93% RH, 65°C/ 95% RH or 85°C and 85% RH. Until recently, little attention has been paid to the characteristics of conformal coatings under condensing environments. Table 1 shows the dew point at several conditions, including those of the common evaluation test methods.

The results in Figure 12 show that the two polyurethane coatings behave in a very similar mode as shown in Figure 10. The nano coat-

| Ambient Temperature °C | Humidity % RH | Dew Point / °C in () °C below ambient |
|---|---|---|
| 25 | 75 | 21 (-4) |
| 30 | 90 | 28 (-2) |
| 40 | 85 | 37 (-3) |
| 40 | 95 | 39 (-1) |
| 65 | 95 | 64 (-1) |
| 85 | 85 | 81 (-5) |

Table 1.

ing results are not shown here as they also performed similarly to before. However, now the two acrylic results are different, with the single coated acrylic showing a large drop in SIR, indicating that the corners of the tracks are not covered. Supporting this conclusion, the image in Figure 13 shows corrosion at the track edge, and with corrosion products forming across the top of the coating between the anode and cathode. The acrylic-1 results show the SIR dropping to 106Ω from the first condensation event, with the behavior remaining broadly consistent through the following condensation cycles. With the double coated acrylic, the SIR results are not as bad, but SIR values are dropping below 108Ω, and with a trend of decreasing SIR with each condensation cycle. The 1oz copper SIR pattern boards the results in Figure 9 do not show any difference between the single and double coated boards, but with the 3oz copper SIR pattern boards the results do show a clear difference, and furthermore the acrylic coating can be seen to failing in either single or double coated condition. Hence the geometry challenge of the 3oz copper tracks for the acrylic-1 coating has been shown by it failing the condensation test. From above this coating passed the humidity test at 40°C/93%RH, and the same coating with the 1oz copper tracks also passed. Thus the incremental geometry challenge and the fine control of the condensing condition in this experimental arrangement allows detailed and robust characterization of coating performance.

As can be seen, the dewpoint is within a few degrees of the ambient conditions at all of these conditions. At 30°C and 90% RH, a common enough condition in South East Asia, and North East America for example, the dewpoint is only 28°C (i.e., if the substrate is just 2°C cooler than the ambient air, condensation can begin to form).

As condensation proceeds from the formation of droplets and then coalescence to the formation of a continuous water layer, with the surface then saturated, it is essentially the same as if it were submerged in water, although there will not be the same dilution effect of ionic contamination. Conformal coatings are known to protect poorly in such immersion conditions.

The reasons for this are easy enough to understand. Conformal coatings are typically applied in the liquid state and dry by a variety of mechanisms. During the drying process, the materials are subject to gravity and capillary forces, making it difficult to ensure uniform and even thickness of the applied coating. When the surface is covered by a continuous water layer, any uncoated, partially coated or defectively coated areas will immediately be exposed to liquid water. Whilst liquid water is not a very good conductor of electricity (5.5 x 10-8 S/m), the presence of ionic species greatly increases the conductivity of water. In today's no-clean chemistry dominated production process, the presence of ionic species is impossible to avoid.

The combination of lack of coating coverage (or sufficient thickness), the presence of ionic species and the presence of even nano-layers of moisture can have a devastating effect on electronics, resulting in short-circuits or even permanent corrosion.

Given the proximity of the dew point to ambient conditions in a variety of common working environments, the impact of condensation on the reliable operation of conformal coated PCBs requires more thorough examination.

There are existing methods for generating condensing conditions within humidity chambers, utilizing differing approaches. The biggest challenge to creating condensation in humidity chambers is related to the chamber hardware itself. It is designed to produce a stable, condensation free environment. The most simplistic method, and one that will struggle to generate condensation, is to ramp the temperature and humidity condition as quickly as possible causing a condensation event. However, chamber design is continually improving, and striving to avoid any such condensation event. A second approach is to introduce moisture by a secondary moisture source. This can be either by an independent heated water tray (as in test K15 from GS 95024-3-1)[1] or direct jetting of atomized water droplets. A third approach uses a multi-chamber approach where the working area climatic environment is rapidly changed by injecting an alternative environment from a reservoir chamber.

There are a number of standards that are based around the above approaches and some of these are given here:

- IEC 60068-2-30, Environmental testing - Part 2-30: Tests - Test Db: Damp heat, cyclic (12 h + 12 h cycle)
- IEC 60068-2-38, Environmental testing - Part 2-38: Tests - Test Z/AD: Composite temperature/humidity cyclic test
- ISO 6270-2, Paints and varnishes—Determination of resistance to humidity—Part 2: Procedure for exposing test specimens in condensation-water atmospheres
- ISO 16750-4, Road vehicles—Environmental conditions and testing for electrical and electronic equipment—Part 4: Climatic load.
- ASTM D1735, Standard Practice for Testing Water Resistance of Coatings Using Water Fog Apparatus
- ASTM D2247, Standard Practice for Testing Water Resistance of Coatings in 100 % Relative Humidity
- ASTM D4585 – Standard Practice for Testing Water Resistance of Coatings Using Controlled Condensation
- JIS 5600-7-2—moisture resistance (continuous condensation method) utilizing aerosol water injection
- JASO D 001-94 (Japanese Automobile Standard): General rules of environmental testing methods for automotive electronic equipment

While these methods can demonstrate controlled condensation the control and ease by which they generate condensation remains challenging. Almost all of these approaches generate condensation in humidity chambers, and this leads to a challenge, since the chamber systems are developed to minimize condensation. In these cases, chambers are run very close to 100%RH, inducing condensation. However, the uniformity of this condensation within the chamber is unknown. Hence, reproducibility of the given approaches will be variable between different chambers from different manufacturers, and furthermore with time developments in chambers will make them less prone to suffering from condensation events. The approach developed overcomes many of these difficulties.

None of these approaches control the sample temperature condition, and hence the uniformity of the condensed water layer is unknown and the stability of the condensed water film with time may not be constant, as the chamber control system attempt to compensate for the variance in the nominal conditions set for the chamber.

The approach adopted for achieving condensation in this study is one that can be realized in any humidity chamber and shows good correlation with the calculated dew point.

**Experimental Setup**

In this approach the temperature of the circuit board under test is lowered, and hence within a high humidity environment condensation will occur. To achieve this condition, the test boards are mounted on a platen whose temperature can be independently controlled. Hence by lowering the platen temperature below the chamber ambient, condensation will occur on the platen, and by the thermal coupling of the test board to the platen, condensation will occur on that as well. There is an assumption that the circuit board under test has a flat unimpeded under side so that it can make good contact with the platen. In Figure 1, we show four PCBs mounted on the platen.

The mounting technique is very simple: the boards are held in position on the platen surface which is at 45° by magnets. The PCBs

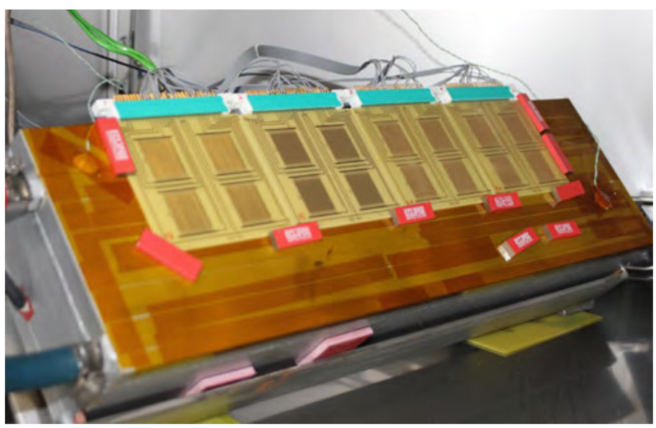


Figure 1: Test boards on platen.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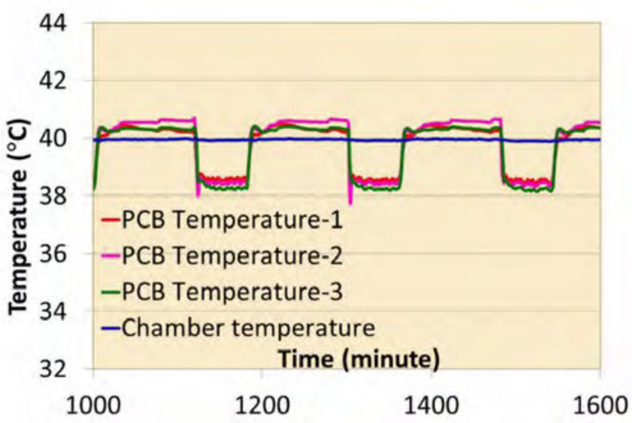



Figure 2: PCB temperature profile during platen thermal cycling.

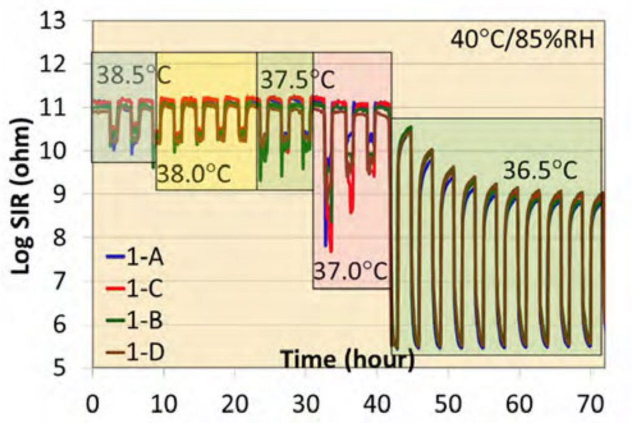



Figure 3: SIR response as the platen was cycled to cooler temperatures.

under test can be connected by the common technique of using connectors, since these are off the platen. In future PCB designs the tabs to the connectors will be extended away from the PCB area in contact with the platen to minimize further any tendency to cause condensation on the connectors themselves. In Figure 2 the ability of the system to control the test board temperature is shown.

The temperature profiles in Figure 2 include the chamber temperature, and it can be clearly seen that this does not change as the platen and PCBs cycle up and down by 2°C, with a nominal chamber temperature of 40°C. This is an important advantage of this approach in that there is no attempt to use transitioning in the humidity chamber condition to create temporary condensing conditions. Furthermore, it can be seen that the transition is rapid in the cooling and heating phase of the cycle, and additionally the low temperature part of the cycle can be sustained indefinitely, or as long as set in the program cycle.

The effect on surface insulation resistance (SIR) on a test PCB with 4 SIR patterns with a 400 µm track and 200µm gap in an ambient condition of 40°C/85% relative humidity (RH) is now explored. This PCB is not conformally coated, the ENIG finished copper is fully exposed. In Figure 3, the effect of cycling to increasingly lower temperatures is presented.

Five sets of data are shown, in which the minimum temperature diminishes by 0.5°C from set to set. In each set the temperature returns to the ambient 40°C. These results show that it is not until the bottom temperature of the cycle reaches 37°C does the reduction in SIR become particularly significant. For the 1.5 to 2.5°C depression of the PCB temperature the level of condensation is only having a minimal effect, but for 3.0 and 3.5°C the condensation is clearly having a significant impact. From this it is clear that the 0.5°C steps provide a fine level of control and that a range of condensing conditions can be readily controlled. The interaction between the ambient condition and the platen temperature can be seen in the comparative results given in Figure 4. At the ambient condition of 40°C/93%RH a platen temperature of 38.5°C now causes significant condensation,

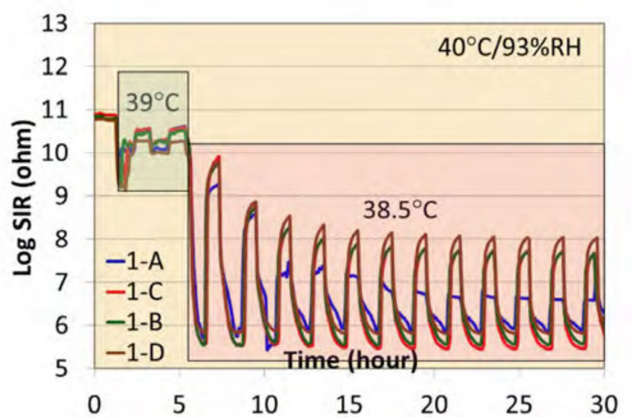



Figure 4: SIR response at 40oC/93%RH under condensing conditions.

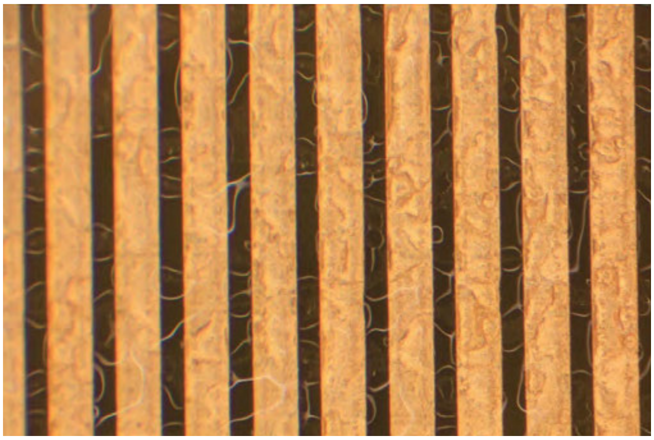


Figure 5: Uniform condensation across the SIR pattern.

which at 85%RH took a platen temperature of 36.5°C. Hence with this experimental arrangement the ambient temperature and humidity and the platen temperature are all independently controlled, and the impact of these factors can be assessed independently. It is also pertinent to note that the platen temperature at which condensation occurs closely agrees with the dew points given in Table 1.

An indication that an even level of condensation is achieved is shown in Figure 5. Here features of the water film can be seen across the entire surface and crossing the track and gap without hindrance.

**Assessing Conformal Coating Performance**

In this study the same test vehicle was used as described above, but manufactured with 1 and 3-oz copper, corresponding to track heights of approximately 35 and 105µm. The test vehicle is shown in Figure 6. The applied coatings included one of the new super hydrophobic nano coatings, two types of acrylic, and two types of polyurethane. The first acrylic was also tested after a double spray process, and both polyurethanes were tested in a thick form. Cross sections of the coatings are shown in Figure 7, the copper thickness is approximately 35 µm, from which the coating thickness can be gauged. Both polyurethanes can be seen to amply cover the track, whereas the acrylic coatings are just managing to do this, and it is not clear whether the nano coating has covered the track.

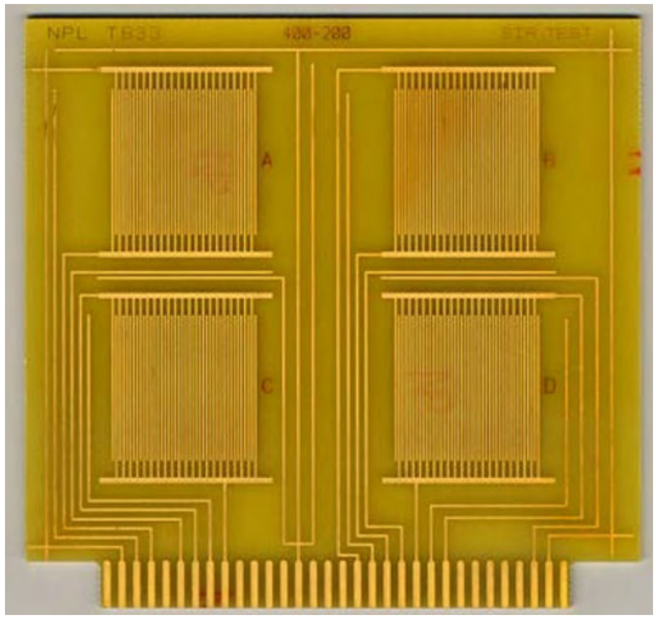


Figure 6: SIR test coupon used for coating studies.

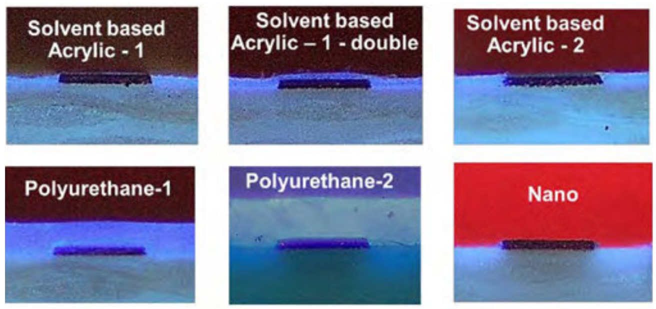



Figure 7: Coating coverage on the 1oz copper tracks of the SIR patterns.

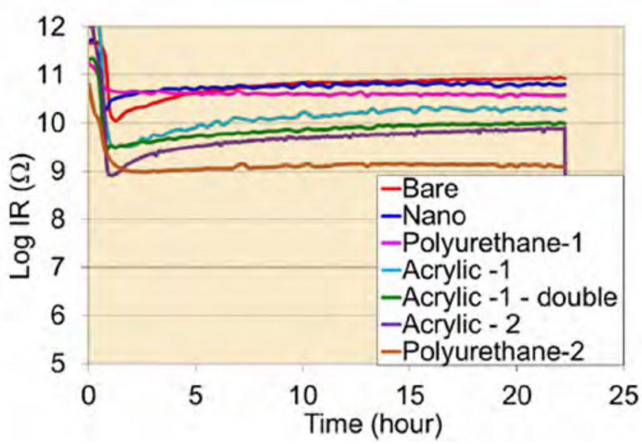



Figure 8: SIR testing of conformal coated boards.

The impact of the double spray process is clear for acrylic-2, where there is clearly a thicker coating on the track. The results of a SIR test, 40°C/93%RH and 5V bias, for the coated boards are shown in Figure 8. These results clearly show that the uncoated board, along with the nano coated board and one of the polyurethane materials have the highest SIR, and one of the thick polyurethanes has the lowest SIR. It is well known that polyurethane coatings can have lower SIR, due to the less hydrophobic backbone, since the absorbed moisture provides an additional conduction path lowering the SIR.

The effect of using the condensing condition is now explored, using a platen temperature of 38.5°C and a 3-hour cycle time with the same environmental condition of 40°C/93%RH and 5V bias. The results of this test are shown in Figure 9 and Figure 10 for all the coatings, and include an uncoated test board. The nanocoating now performs very poorly with little difference between the results and the bare board. All three acrylic results follow the condensation cycle but have less than a two decade drop in SIR, with the values always above $10^8\Omega$. The polyurethanes are far less susceptible to the condensation cycle, particularly polyurethane-1. For all coating results the response from the four SIR patterns on each test coupon are very similar. Clearly, all the coatings, except the nano coating, are working to prevent a large drop in SIR as seen with the bare test board. This is contrary to the SIR results seen in Figure 8.

The coating coverage on the 3-oz copper test boards are shown in Figure 11. Again the polyurethanes are easily covering the copper tracks, and with the nano coating again there is no evidence of coating. However, with the acrylic, acrylic-2 was not used on the 3-oz copper SIR boards, it is difficult to determine from these images if the acrylic coating has covered

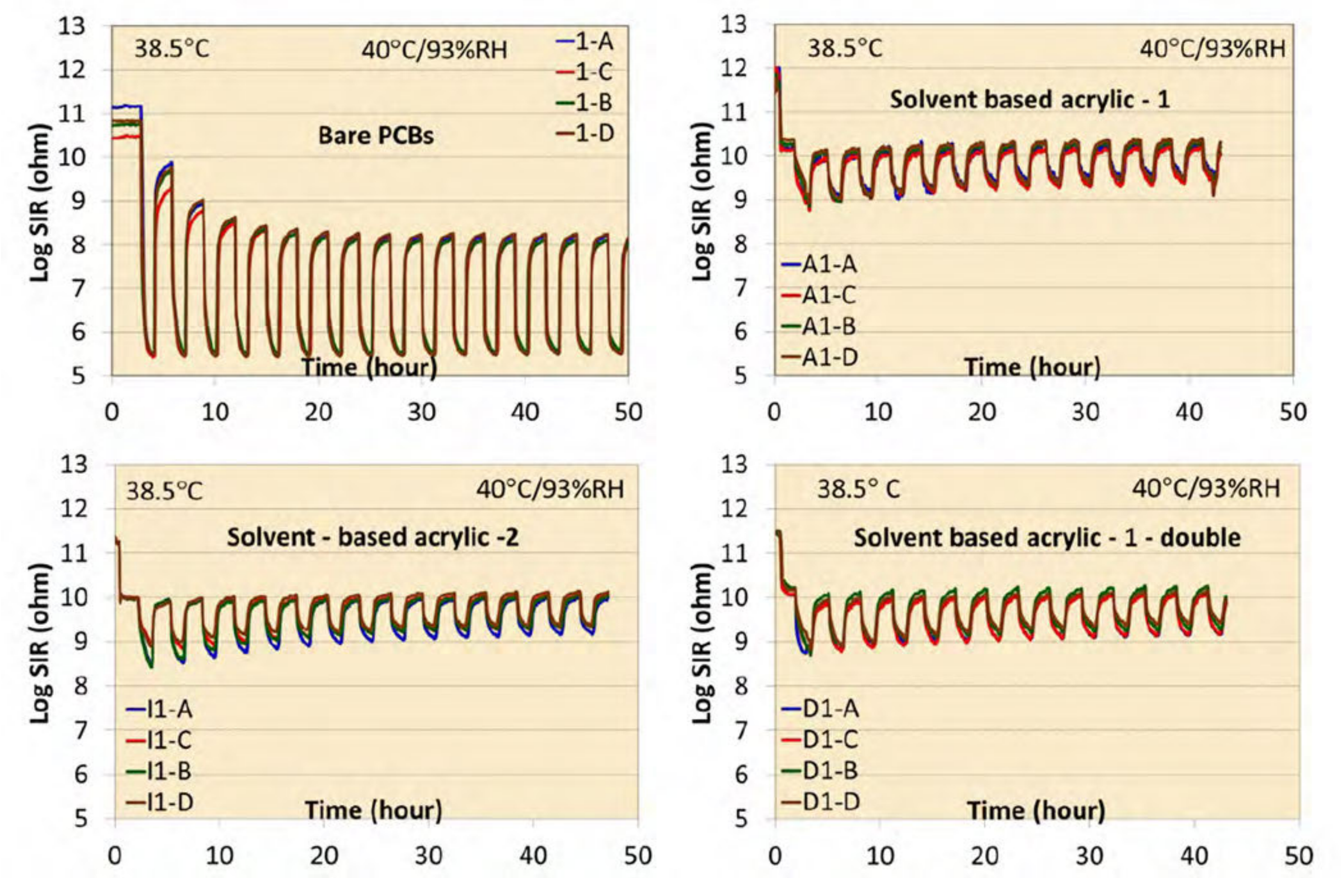



Figure 9: Condensing conditions with the 1oz copper tracks and the acrylic coatings.

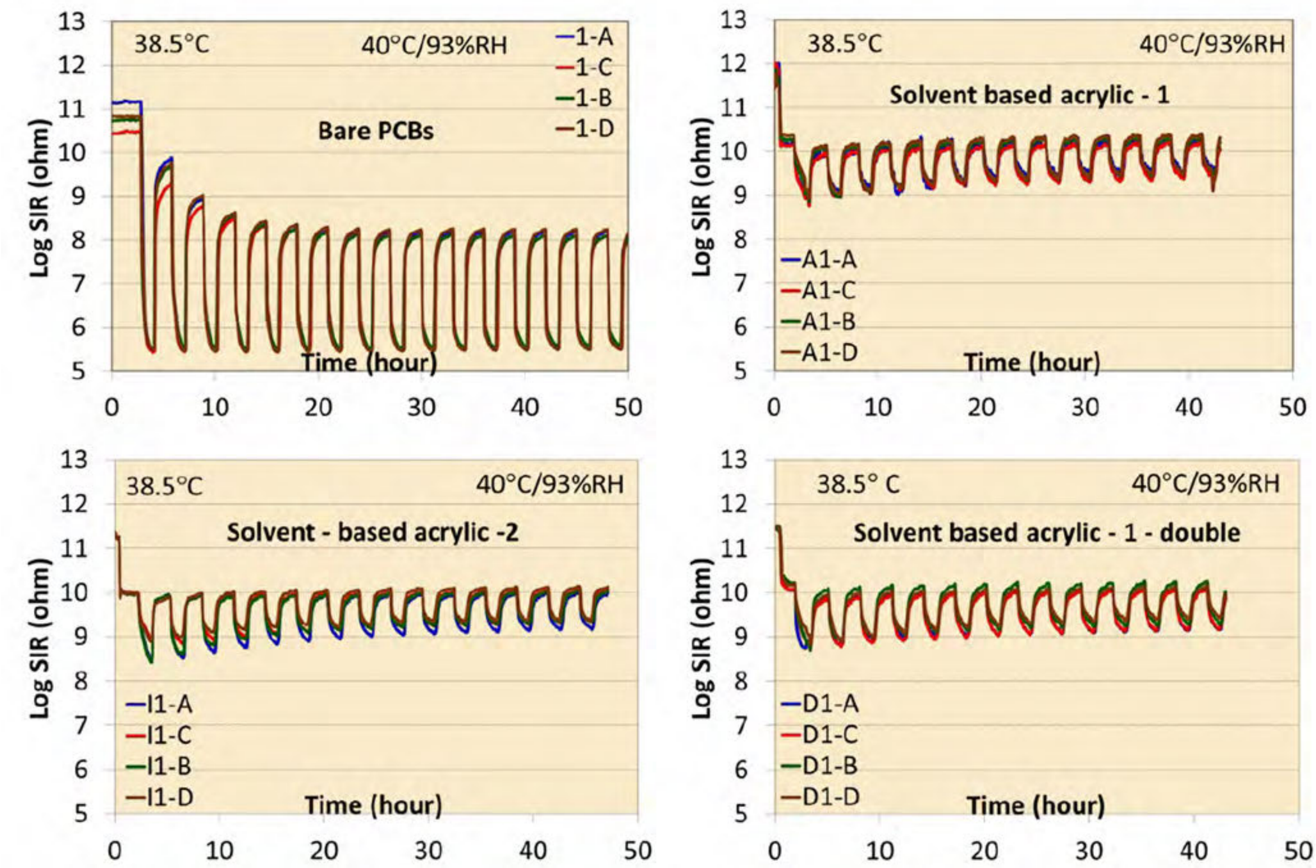



Figure 10: Condensing conditions with the 1oz copper tracks with the nano and polyurethane coatings.

the copper track and in particular, whether the corners are coated. The results from the condensation testing of these coated boards are presented in Figure 12.

The results in Figure 12 show that the two polyurethane coatings behave in a very similar mode as shown in Figure 10. The nano coating results are not shown here as they also performed similarly to before. However, now the two acrylic results are different, with the single coated acrylic showing a large drop in SIR, indicating that the corners of the tracks are not covered. Supporting this conclusion, the image in Figure 13 shows corrosion at the track edge, and with corrosion products forming across the top of the coating between the anode and cathode. The acrylic-1 results show the SIR dropping to 106Ω from the first condensation event, with the behavior remaining broadly consistent through the following condensation cycles. With the double coated acrylic the SIR results

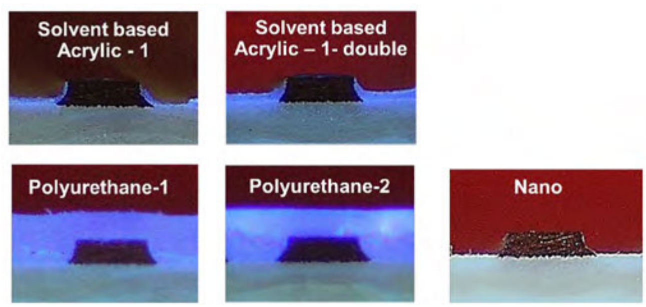



Figure 11: Coating coverage on the 3oz copper tracks of the SIR patterns.

are not as bad, but SIR values are dropping below 108Ω, and with a trend of decreasing SIR with each condensation cycle. The 1oz copper SIR pattern boards the results in Figure 9 do not show any difference between the single and double coated boards, but with the 3-oz copper SIR pattern boards the results do show a clear difference, and furthermore the acrylic coating

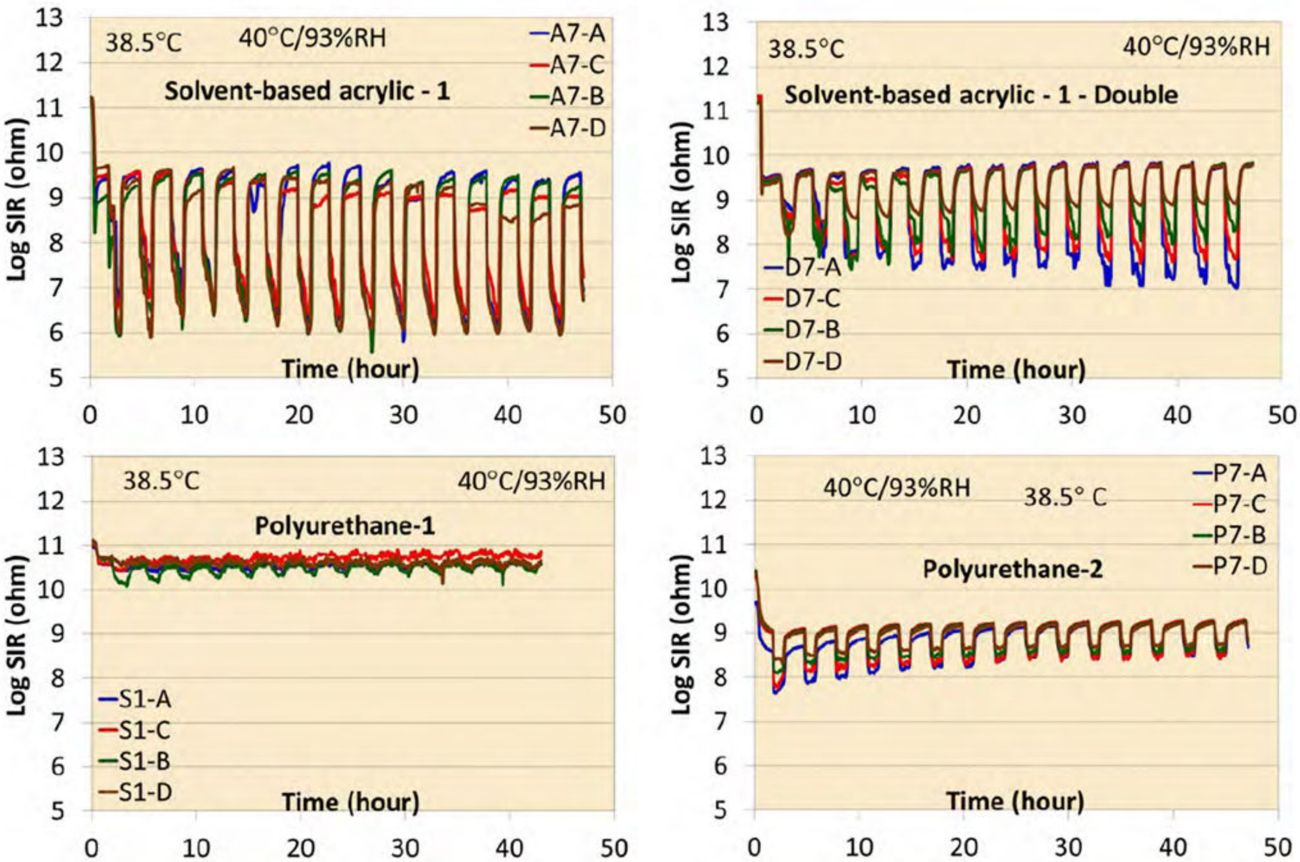



Figure 12: Condensing conditions with the 3oz copper tracks with the acrylic-1 and polyurethane coatings.

can be seen to failing in either single or double coated condition. Hence the geometry challenge of the 3-oz copper tracks for the acrylic-1 coating has been shown by it failing the condensation test. From above this coating passed the humidity test at 40°C/93%RH, and the same coating with the 1oz copper tracks also passed. Thus the incremental geometry challenge and the fine control of the condensing condition in this experimental arrangement allows detailed and robust characterization of coating performance.

## Discussion

It is well known that water films will lead to anodic corrosion on powered circuitry and that conformal coatings are a suitable mitigator. However, this requires complete coverage of all the parts so that the water film has no access to the energized parts of the boards. Hence there is an issue with achieving complete perfect conformal coating coverage.

The technique described here that has just been developed and offers a wide range of flexibility in the test conditions. In the current setup controlled levels of condensation can be achieved above 30°C and a range of humidities. A crucial aspect of any condensation technique is the ability to achieve a number of aims: repeatability, controllable and stable conditions, and maintain those conditions over any desired time period. Within the many existing testing methods that were mentioned above there is a great challenge to achieve a fully controlled condensing condition across the wide range of equipment manufacturers, and hence there is a struggle to achieve all four aims in the wider context of standards testing. However, the approach described here has this ability, and furthermore these four aims are easily met.

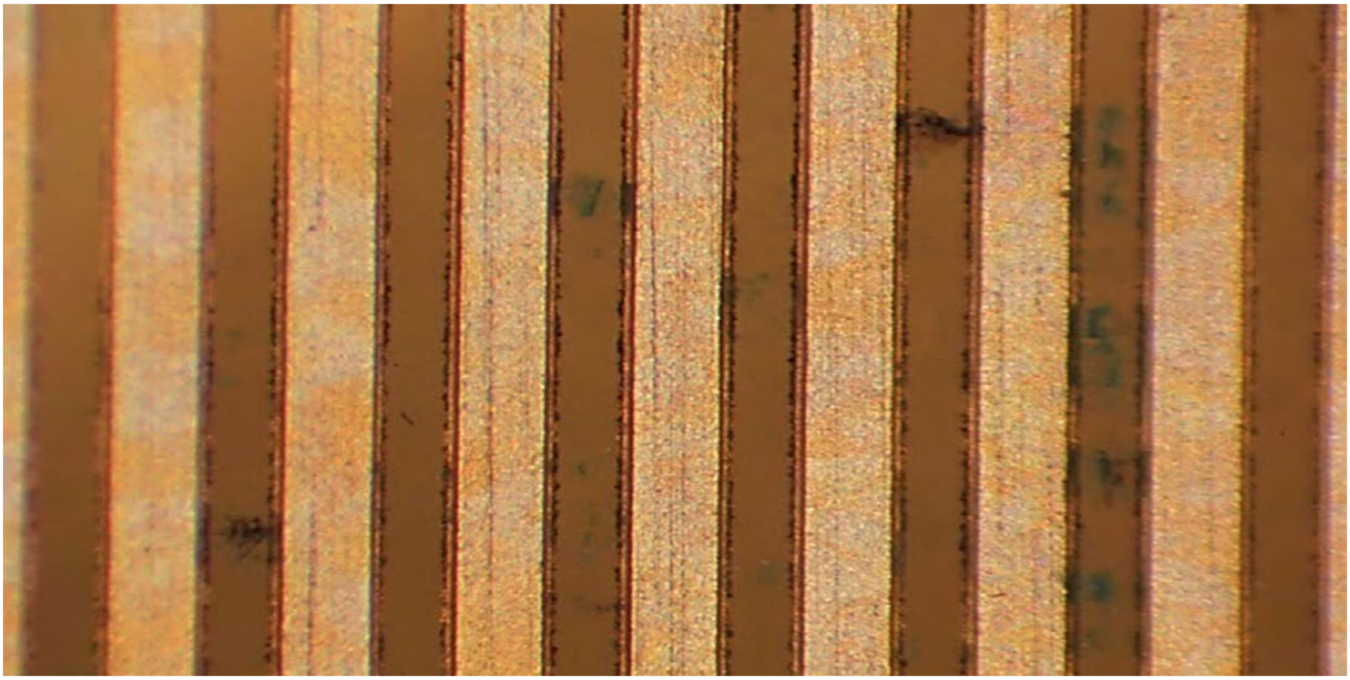


Figure 13: The 3-oz SIR pattern coated with acrylic-1 with evidence of corrosion from the track edges.

The challenge of achieving stable and controlled condensing conditions over large areas is understood by a consideration of the dew point and the onset of condensation. This work shows that the SIR of the uncoated coupons, begins to drop noticeably when the temperature of the platen was dropped below the dewpoint. At 40°C and 85% RH the dewpoint is 37°C, and the onset of degradation was noticeable at 36.5°C. At 40°C/93% the dewpoint is 39°C and the SIR drop was noticeable at 38.5°C. These results are important in showing that there is good agreement between the platen and dew point temperature, and confirms that the platen arrangement is performing as expected.

The experiments described here show clearly that while test boards may pass simple humidity testing, as the geometry of the surface becomes more challenging test boards will fail under condensing conditions if complete coverage is not achieved, as was observed with the acrylic-1 results. In Figure 8 the SIR results for acrylic-1 are very good, for the 1-oz copper tracks in Figure 9, there is some susceptibility to condensation cycles but the SIR values are still high and above 109Ω. However, in Figure 12 with the 3-oz copper track the SIR values are now at the 106Ω level, which is classed as an SIR failure. Hence, the difficulty in achieving good coverage with these acrylic materials became apparent as the copper track thickness increased, and even with the application of two separate coating layers the performance was problematic.

These results clearly demonstrate the need for condensation type testing for finding the weaknesses in coating coverage, and furthermore the control that can be achieved with this experimental setup allows this to be readily achieved than has hitherto been possible. However, while specific condensing conditions can be achieved the desired test parameters still need to be developed, and this will be the scope of further work.

## Conclusions

A review of condensation testing reveals that there are many approaches to achieving the required condition. These approaches struggle to achieve a known and uniform steady state across the test vehicle, and typically attempt to achieve condensation while fighting the inherent control system of the humidity chamber.

This paper presents a new technique for achieving condensing conditions on circuit boards, and utilizes an approach of using a platen as an independent means of controlling the substrate temperature to induce condensation, which has been shown to be uniform. Hence complete control of the condensing conditions can be achieved in a wide range of temperature and relative humidity climatic conditions, and the level of condensation can be easily adjusted and maintained over long periods of time and readily cycled through those conditions. Since the whole test board is cooled on a platen the condensation film that forms will be uniform across the surface.

This paper has shown that as the test becomes more severe the condensing conditions will find weaknesses in the coating quickly. While humidity SIR and a low profile condensing test, the test vehicle passed, as the geometry became more challenging weaknesses and failures were observed. The results confirmed the susceptibility of exposed edges under condensing conditions, and that complete coating coverage is crucial.

The thicker polyurethane materials demonstrated much greater resistance to condensing environments, with polyurethane-1 in particular showing little change in SIR during the condensation events.

It was surprising how quickly the insulation resistance of the acrylic materials and polyurethane-2 dropped with the onset of condensation—the drop in SIR being almost instantaneous. Condensation conditions will find weaknesses in the coating quickly.

Of particular surprise was the poor performance of the nano-coating. It showed no resistance to the condensing environments whatsoever, and corrosion was evident on the traces at both 1oz and 3oz copper track thickness. Although the coating contained a fluorescent trace it was impossible to determine coverage by cross-section.

Therefore, it is clear from both the SIR results, the cross-sections and the visual inspection that conformal coating coverage is crucial in providing protection under condensing environments. There was a clear correlation between coating thickness and coverage and SIR under condensing environments. **SMT**

## References

1. BMW GS 95024-3-1 (Test K15).

*Note: This article was presented at the technical proceedings of the IPC APEX EXPO 2016.*

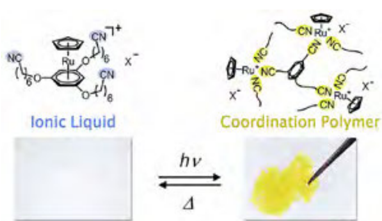
**Chris Hunt** leads the Electronics Interconnection team at the National Physical Laboratory (NPL).

**Ling Zou** is the head of the Measurement Service for Industry in the area of Electronics Interconnection at NPL.

**Phil Kinner** is the technical director of Electrolube's Coatings Division.

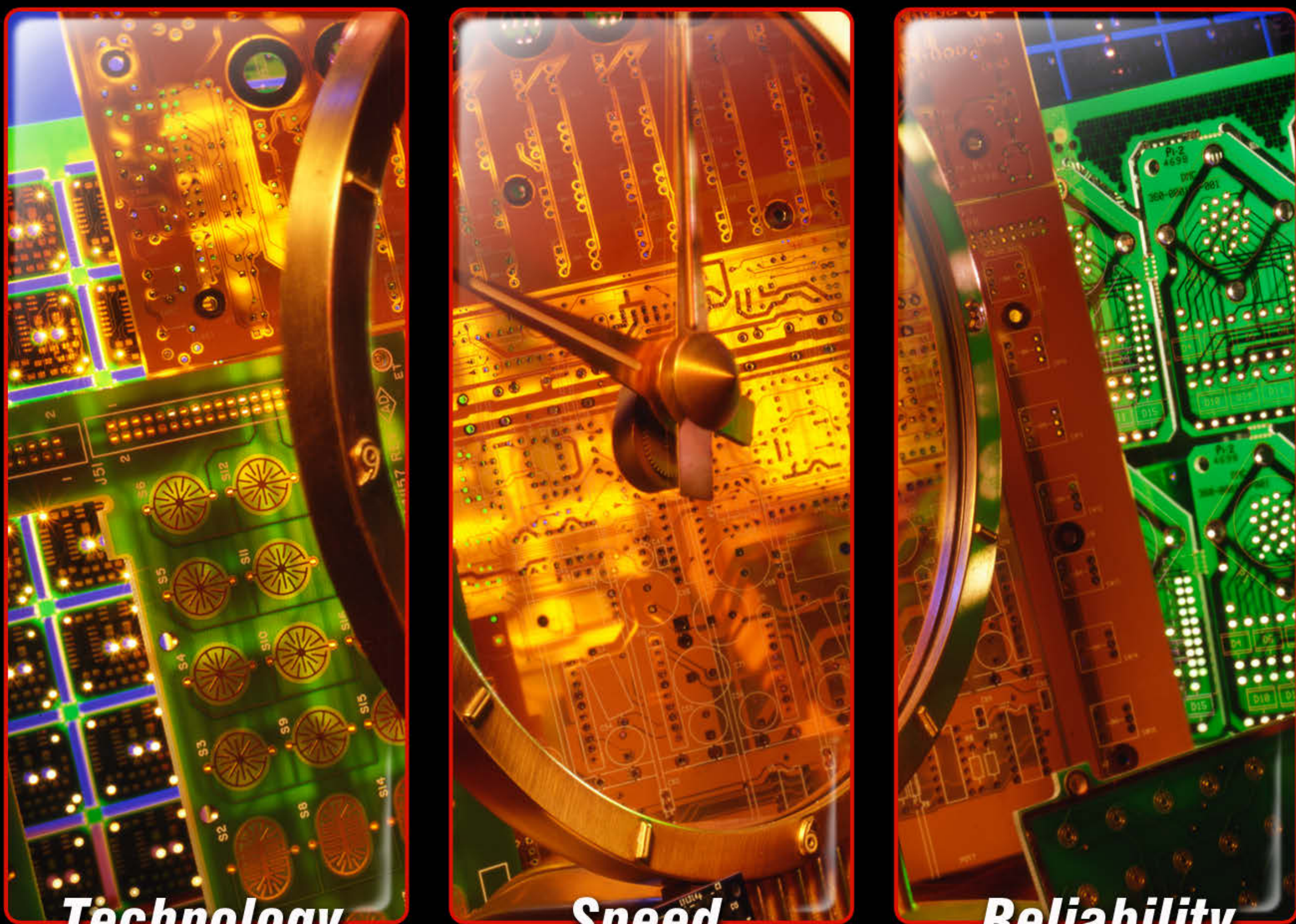
# New Compound Switches Between Liquid and Solid States when Exposed to Light or Heat

A research group led by Professor Mochida Tomoyuki of the Kobe University Graduate School of Science and Dr. Funasako Yusuke of the Tokyo University of Science has become the first in the world to develop an ionic liquid from a ruthenium complex with cyano groups that transforms into a solid when exposed to light and returns to liquid form when heated.




If you apply ultraviolet light to the liquid for a few hours, it changes into an amorphous coordination polymer, and if you heat this solid for one minute at 130°, it returns to its original ionic liquid form.

This research has led to the successful creation of a reusable photocurable liquid that can potentially be applied to printed circuit boards, 3D printing, and adhesives.



# MilAero007 Highlights

## Acromag to Offer ECM Services

Acromag's strategy to automate its processes resulted in increased available capacity for growth—and thus providing the company the capacity to manufacture not only its own products but also offer its manufacturing expertise to customers who need to bring their products to market.

## Plexus to Relocate Design Center

Plexus will be relocating its Neenah Design Center, located at 55 Jewelers Park Drive, to Downtown Neenah.

## Vexos's Markham Facility Approved for Registration to Canadian CGP

Vexos' manufacturing facility in Markham, Ontario, Canada has been approved for registration to the Canadian Controlled Goods Program, a Canadian Federal Government Program administered by Public Works and Government Services Canada and is legislated by the Defense Production Act and the Controlled Goods Regulations.

## Orbit International's Electronics Group Lands Orders Over $1M in May

Orbit International's bookings for its Electronics Group exceeded $1 million for the month of May 2016, highlighted by several follow-on production awards including a contract for a product supporting a gun weapon system as well as other awards for displays and switch panels.

## Jabil Wins Gartner's Manufacturing Supply Chain Innovation Award

Gartner has named the Jabil InControl supply chain visualization and analytics platform a winner in its "Supply Chainnovator" awards during the Annual Gartner Supply Chain Executive Conference.

## Computrol Triples Its Medium Volume Inspection Capability with Three Koh Young SPI Systems

Computrol Inc. has purchased three KY-8030-3 in-line, fully automated SPI systems from Koh Young Technology.

## Dynamic EMS Expands Management Team

EMS firm Dynamic EMS recently strengthened its management team with the arrival of Gordon Macdonald and Sharon Fry.

## PNC Improves Manufacturing Capabilities with Ersa Selective Wave Solder

PNC has improved its manufacturing capabilities with the recent purchase of Ersa's ECOSELECT 2 selective wave solder machine.

## Stadium Appoints New MD to Head Up Global Power Business

Stadium Group has appointed Martin Brabham as managing director for its global power business, comprising the Stadium Power and Stontronics brands.

## SMTC Completes ITAR Registration

EMS firm SMTC Corp.'s San Jose manufacturing facility has completed International Traffic in Arms Regulations (ITAR) registration and is now in compliance with ITAR.

# PERFECT PLACEMENT OF CONNECTORS AND PINS:

## 3D Measurement of Swash Circumference and Embedment Depth

**by Jens Mille and Jens Kokott**
GOEPEL ELECTRONIC GMBH

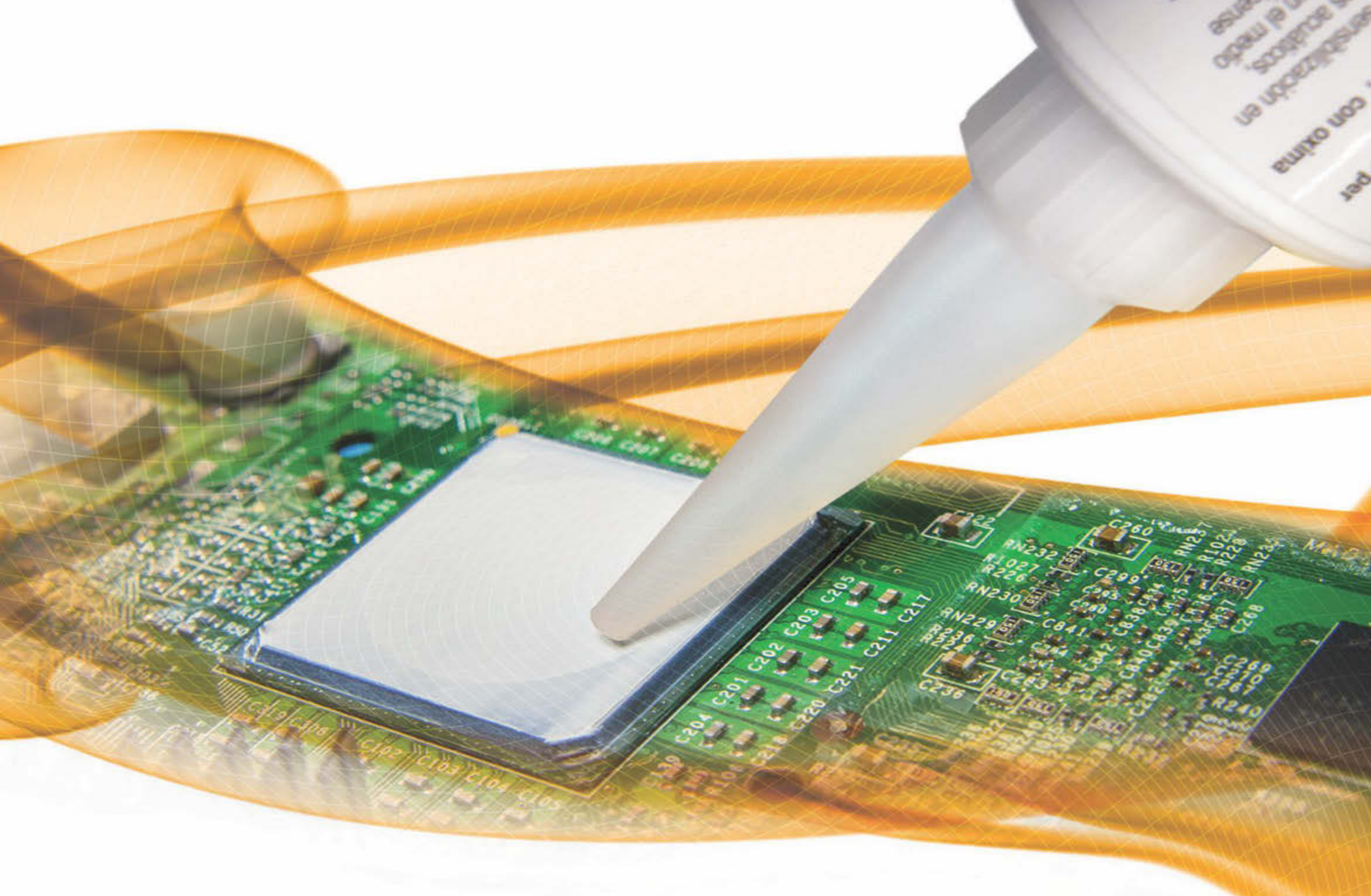
Where the production of electrical PCBs is concerned, manufacturers are faced with steadily increasing miniaturization and higher packing density. Coupled with this, increased requirements are placed on production and testing technologies. The same applies to the manufacturers of connection technology such as connectors and individual pins. Here, too, an increasing number of contacts have to be accommodated in ever smaller areas.

Packing densities in particular repeatedly create challenges in terms of testability, especially when high components such as connectors are fitted in close proximity to other components.

Connectors are also included in the scope of testing, and their design means that they have completely different handling and testing requirements. In addition to the traditional solder joint inspection, the mechanical integrity of the pins must also be checked. Two parameters are of interest in this context: On the one hand, the lateral location of the pin tip, and on the other hand, its height.

The horizontal as well as the vertical position of each individual pin must be tested if these connectors are to be used to establish an electrical connection to other assemblies in a subsequent automated process, or they are precisely fitted into a housing. Automated installation is no longer possible if the pins were deformed through mechanical influences during the preliminary stages.

The examination of the pin displacement on a lateral plane is called swash circumference testing. Swash circumference testing can be carried out using orthogonal inspection. This can generally already be ensured through standard 2D AOI systems. However, it must be considered that the pins, whose diameter is often smaller than one millimetre, have a tip that is only a few tenths of a millimetre in size. The illumination of the test object is therefore



of key importance for the reliable detection of the characteristic. The AOI systems of GÖPEL of electronic GmbH have been successfully used for this testing task for many years, due to their multi-spectral and multidirectional lighting.

**Measurement of Embedment Depth: a Particular Challenge**

There is, however, a sharp increase in requirements when the height of the pin tip has to be determined. This test task is known as embedment depth or press-in depth. As the name of the test task indicates, it is not possible to meet these requirements using the usual two-dimensional measurement and testing technology, as orthogonal inspection cannot provide information on height. This problem cannot even be resolved by using suitable cameras for testing, because the deformation of the pins and PCB is unknown prior to the test, and it is often difficult to detect the pin tip. The reverse conclusion is: An additional testing dimension is required!

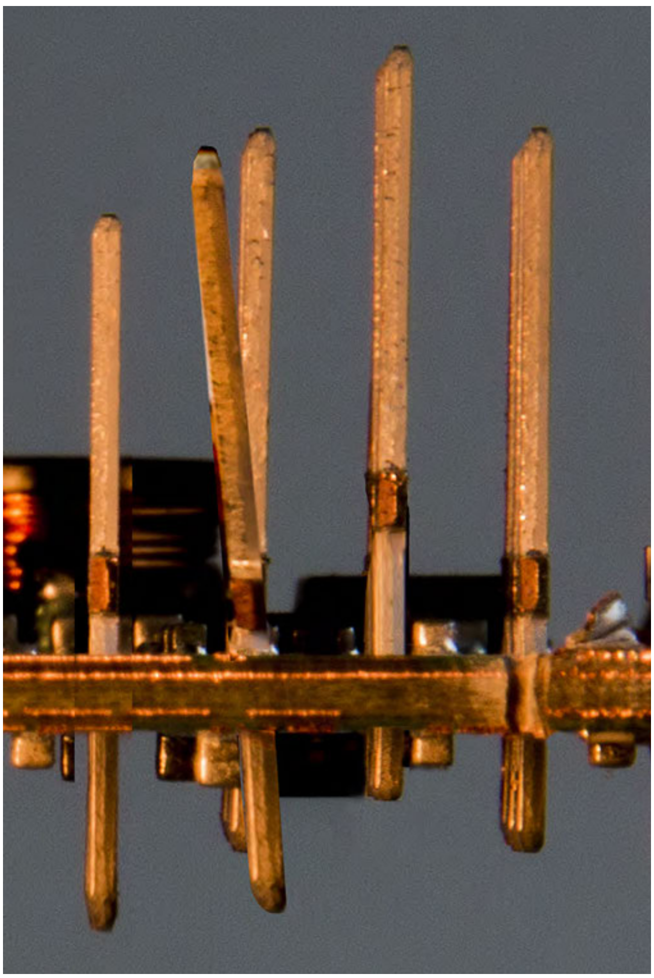


Figure 1: Possible errors on a connector pin.

Attempts to solve this problem using fringe projection often failed because of uncooperative surfaces, which do not provide reliable measuring signals as they are strongly reflective. Neither is it possible to use a triangulation process to carry out measurements into connector housings, as the walls of the housing literally put the interior parts into the shade. This can be partly compensated for through the use of several projectors or cameras, but, if not before, it becomes apparent that it cannot be used for measurements into holes when determining the press-in depth of a pin into a PCB (e.g., pressfit technology) or into other objects (e.g., connector housings).

**3D Measurements Based on TMSA Technology**

One such technology that makes it possible to carry out 3D measurements even into deep holes with very small diameters (<0.5 mm) is telecentric multi spot array (TMSA).

TMSA features a white light source coupled into a telecentric measuring lens developed specially for this purpose. As a result, there is no angle between the light source and the sensors (in contrast to the triangulation process), which means that the lighting and signal beam path are identical. This configuration has the advantage that no shadows are created on high components, making it possible to carry out reliable measurements into deep gaps between components or into holes.

With this arrangement, the lens now differentiates the individual light wavelengths, so that only a small wavelength range is focused and reflected back, depending on the distance between the measuring lens and the surface to be measured. The reflected light or measuring signal is associated with a height value based on the evaluation of the respective intensity. Since this lens projects individual measurement points onto the PCB, the spot array must be moved for a wide-area recording of measurement values. Depending on the increment, this makes it possible to implement different lateral

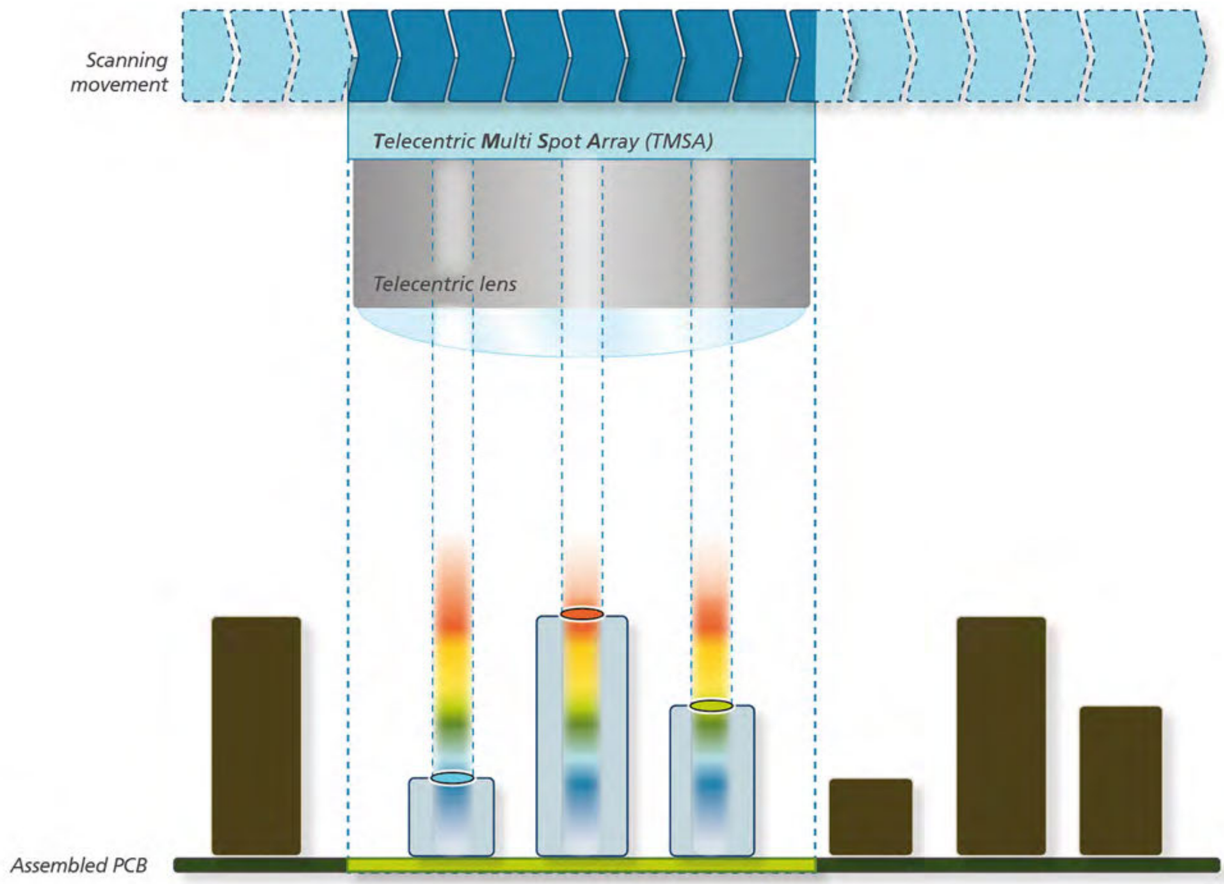



Figure 2: TMSA technology.

resolutions during scanning, so that they are freely configurable based on the requirements of the measuring task.

The technology also enables measurement values to be generated regardless of the reflection characteristics of the respective surfaces, making it possible to check features independently of the layout.

Where connectors or individual pins are concerned, errors such as bent connection contacts, too deep pin insertion into the housing, or portruding pins can occur. These may cause missed insertion of counterparts in subsequent processes. In a worst-case scenario, the assembly is unusable as a result.

The 3D measuring algorithms provided in the AOI Software PILOT 6 enable the user to measure the swash circumference—the deviation in x and y direction—as well the height and embedment depth of the pins, and assess them based on defined tolerances.

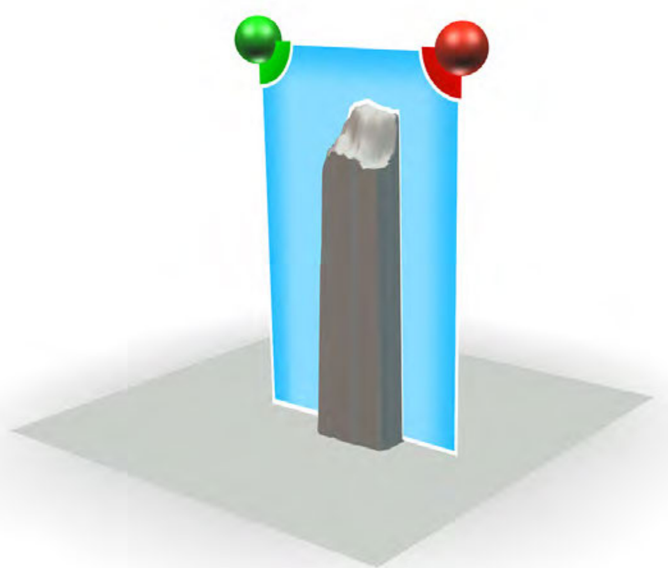


Figure 3: Pin with measurement level for embedment depth testing.

The TMSA technology described above is integrated into Goepel's 3D·EyeZ measuring module, which is available in the stand-alone BasicLine AOI system and the new VarioLine system. The adjustable lateral resolution makes it possible to project a sufficient number of measuring points onto pins or into holes, and to record measurement values.

**Summary**

Swash circumference testing and embedment depth measurements of connectors or individual pins place high demands on the measurement technology used. The sole use of orthogonal or angled view inspection is not suitable for this three-dimensional measuring task.

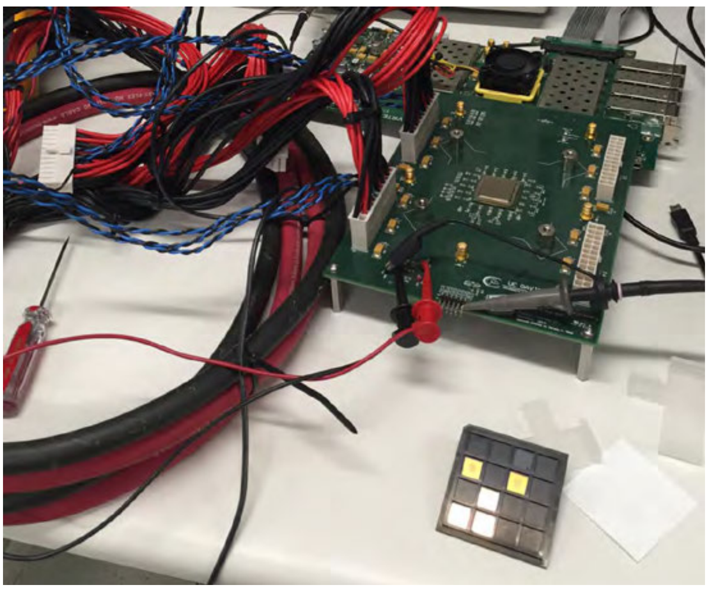
Fringe projection based on triangulation also reaches its limits in this context, as shading occurs on the one hand, and the detection of the pin tips can no longer be ensured on the other hand. It is also completely impossible to carry out depth measurements in holes using this method.

The TMSA technology can eliminate the disadvantages described above. Integrated with the 3D·EyeZ measuring module, the system is available inline or for stand-alone AOI systems. **SMT**


**Jens Kokott** is product manager, AOI, at GOEPEL Electronic GmbH.

**Jens Mille** is the project manager for systems development, AOI, at GOEPEL Electronic GmbH.


# World's First 1,000-processor Chip



A microchip containing 1,000 independent programmable processors has been designed by a team at the University of California, Davis, Department of Electrical and Computer Engineering. The energy-efficient "KiloCore" chip has a maximum computation rate of 1.78 trillion instructions per second and contains 621 million transistors.

KiloCore is said to be the world's first 1,000-processor chip and is the highest clock-rate processor ever designed in a university, according to Bevan Baas, professor of electrical and computer engineering, who led the team that designed the chip architecture. While other multiple-processor chips have been created, none exceed about 300 processors, according to an analysis by Baas' team. Most were created for research purposes and few are sold commercially. The KiloCore chip was fabricated by IBM using their 32 nm CMOS technology.

The chip is the most energy-efficient "many-core" processor ever reported, Baas said. For example, the 1,000 processors can execute 115 billion instructions per second while dissipating only 0.7W.

Applications already developed for the chip include wireless coding/decoding, video processing, encryption, and others involving large amounts of parallel data such as scientific data applications and datacenter record processing.

# The STEM Trap

**by Tom Borkes**
THE JEFFERSON PROJECT

There is something very wrong here. A detached and segregated educational system has caused a lack of proper academic preparation for some of our current, technically based industries. For example, the high-tech product assembly industry has gone through a transformation from labor-intensive to high-tech automated assembly processes. The people who inhabit the ivory tower have largely ignored this evolution. The exodus of jobs in the U.S. from these production operations that are staffed with ill-educated personnel has produced a flurry of anger and activity—a public drum beat to identify the cause and fix it. Previous *Jumping off the Bandwagon* columns have identified some popular misconceptions about what got us here that are currently en vogue—red herrings that distract from the core issue.

While these factors may contribute to the issue at hand, the root cause is our traditional educational system and production organizational structure. Post-secondary schools have not been responsive to the changing landscape of the modern electronic product assembly operation—they really can't, considering the lack of real-world experience of most of the faculty. Regardless, we have tasked the perpetrator with solving the problems they have largely created! *Learning for learning,* which the perpetrator is best at, has totally dominated the educational system and *learning for earning* has been ignored for the most part.

Last month, we discussed the high-tech educational business. But instead of using the traditional caste system model with the faculty and administration considered in the upper stratum and the students as subservient, we turned things upside down. We posited a model that held the student as the customer, with the faculty and administration in a service provider role to their student-customers.

What makes the post-secondary school/student relationship even more unique is how uneducated the *customer* is—in more ways than

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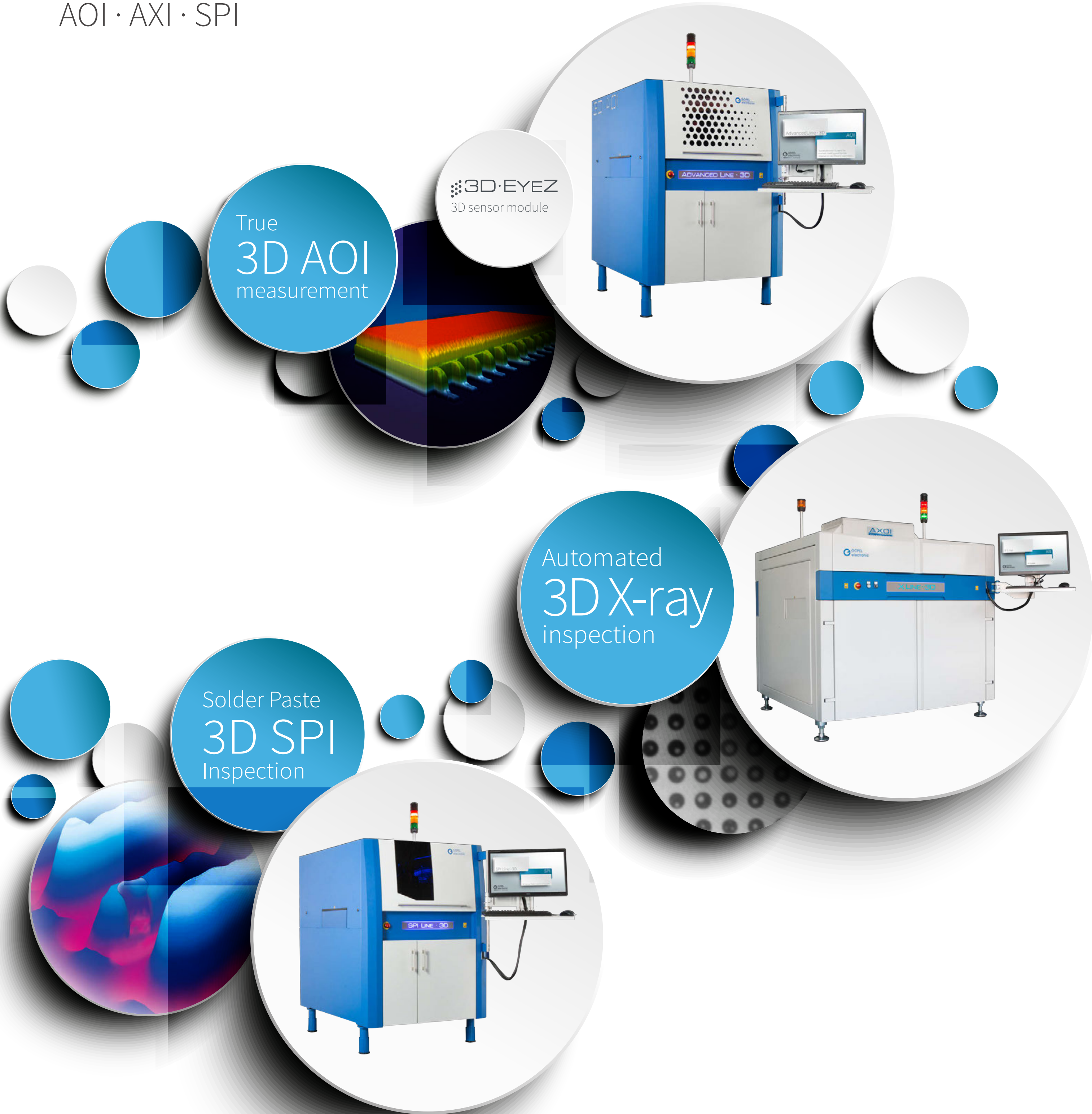


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one. This is a customer that unlike the car-buying or restaurant-going customer, hasn't a clue as to the *value* of the *product* they are paying for—an easy mark, easily taken advantage of without the proper checks and balances. In a free market economy with students subject to a system with the same basic educational objectives throughout, the *value* of that education is partially a matter of the competition that the student population will face in the real world. Within the confines of the U.S., for example, if all the competition resides within its borders

> "A college was to develop the student's mind, creating an open and analytic template for thinking for themselves."

and *learning for earning* is not a component of the university system, does it matter? Not much. But, how about on a global competing field that has different ideas about what a student's education *product* should be? Where, perhaps, in other countries *learning for earning* takes on a greater importance in the post-secondary education world.

So, in our global economy it becomes important and appropriate that a college as a *supplier* establishes what the *product* is that they are selling to their naïve, dependent, uneducated customers. Is it solely a liberal education? This has been the primary objective since the Age of the Enlightenment. A college was to develop the student's mind, creating an open and analytic template for thinking for themselves. Said another way the school was to foster an open mind not tied to the dogma of their parents, their church, their country, or for that matter, their school—developing critical thinking skills that permit problem solving and decision making in an objective way. Even in the most unbiased environment, isn't this a difficult goal to achieve in the antiseptic *Ivory Tower?*

Based on the academic landscape that is on display today, do you think our university system in the U.S. even meets this objective? And, even if it does, is that enough? Is it time to reexamine the role school plays in grooming the youth to be valuable contributors for the society they will be entering? What about the *learning for earning* part? Does the education *product* produce a piece of paper that will get the student a good job upon graduation? Surely education for professions such as medicine, law, and yes, engineering, attempts to overlay biological, legal and physical sciences on top of a liberal education. However, do we continue to leave the specific technical skill set development part of a student's education to industry, or "trade" schools? This historic aspect of a traditional engineering education becomes a convenient truth for college administrators when we realize that most engineering faculties don't have a staff with these skills—whether it is running a milling machine or a pick and place machine. Should any engineering faculty consist of even one member that does not have real world experience to complement the skill to teach, and the analytic aptitude to grasp, the *physics?*

The opposite of these resume elements has historically been the case. Why?

Arrogance, hubris and self-defense continue to be front and center as we have locked ourselves into what we are good at—academic performance, not what would be most valuable to our students, our customers. Not understanding, or wanting to understand, the nature of today's high tech electronic product design of assembly is another reason for having tolerated the status quo.

Whether the post-secondary educational system will admit it or not, the level of technological understanding to successfully compete in the high tech electronic global manufacturing marketplace has blurred the line between the trade skills and the engineering skills necessary for an original design provider (ODP) and electronic manufacturing services (EMS) provider. It is a hard transition for most general managers to substitute the traditional minimum wage assembly-line workers with a high priced engineer who can develop the automation to reduce the labor content of a product's assembly and test, as well as run and service the line[1]. However, there are some companies that are beginning to see the economic sense this makes.

A favorite TV show of my impressionable youth was Rod Serling's classic sci-fi series, "The Twilight Zone." One particular episode stands out when I ponder the current state of high-tech electronic product design and assembly education. The episode was entitled "To Serve Man." An alien civilization arrives on earth and wants to share all their advanced technology with us—medical, food production, space travel, energy, everything! An alien provides a large book written in his native language that is believed to be a roadmap to the alien's largess. At first, translators are able only to decode the title, "To Serve Man." As the effort to decode the text continues, the alien extends his advanced civilization's spirit of goodwill by inviting thousands of volunteers to visit his planet. In one of the final scenes as the spaceship is being loaded with humans, a frantic translator rushes the boarding queue and screams: "We finished the translation! Don't get on the ship! 'To Serve Man' is a cookbook!"

It is in the nature of many of us to think and hope for the best; give the benefit of the doubt; trust in the virtuous intentions of the "experts," who we entrust with a portion of our welfare—whether it be the defense of our country, the safety of the food and water supply, the safety and efficacy of the medicines we ingest, or the education of our children. The *cookbook* provided by our educational system must be in the students' best interest. Right?

That brings us to this month's topic: *The STEM Trap*.

As you are probably aware, STEM is an acronym for science, technology, engineering, and mathematics. In the U.S., the term accelerated in usage as dismal K-12 student academic performance compared to other countries and the exodus of tech jobs offshore broke into the public consciousness. There was political hay to be had by addressing this issue. Government at the local, state and federal level, of course, got involved —rightly so in this case since they have the core responsibility for the compulsory primary and secondary educational systems. The National Science Foundation (NSF) established guidelines on what learning disciplines fell under the STEM banner. Spending money is what governments generally do in these situations to demonstrate their concern and just how serious and important they perceive the problem.

In 2006, President George W. Bush announced the American Competitiveness Initiative that increased federal funding for advanced R&D programs.

President Barack Obama and former Secretary of Education in the Obama administration, Arne Duncan, have endorsed the not-for-profit *Project Lead the Way,* a large provider of STEM based programs to middle and high schools.

In his 2012 budget, President Obama renamed and broadened the *"Mathematics and Science Partnership (MSP)"* to award block grants to states for improving teacher education in those subjects[2].

And, it goes on and on and on as the government funding faucet has been turned wide open.

"Doesn't anyone recognize it as a real problem that a significant task in STEM education is the need to educate the educator?"

Doesn't anyone recognize it as a real problem that a significant task in STEM education is the need to educate the educator? Why hasn't the NEA (National Education Association) addressed these issues proactively? What the heck have they been doing for three decades, just collecting paychecks? Now, we are going to ask them to solve the problem they have helped create? What an outrage!

Manufacturing sciences are a relatively small part of the STEM initiative. This is ironic since offshoring manufacturing and product assembly were major contributors to the notion that the U.S. had a lot of work to do in stimulating educational interest in the sciences. I think what has happened is that, except for 3D printing and some other sexy advancements in manufacturing, the elite still associate electronic product assembly with the skills that Henry Ford required for his assembly line[3].

Who's driving this STEM train—academia, industry, or government? It's money that drives the train in this top down push for better education in science and math. But, where is the train going? The money, as with most government social engineering programs, goes to grants, and the grant money will be spent whether it results in an outcome the has value or not. Many times the *result* is that "we need more money."

Let's review the government track record on some other programs.

In 1977, President Jimmy Carter created the Department of Energy through a rearrangement of existing departments and creation of new agencies. This occurred while the U.S. was in the throes of an energy crisis that begin in 1973. One of the stated goals was to make the U.S. less dependent of foreign oil imports. The result: in 1977 the U.S. imported about 2.4 billion barrels of oil. In 2015 the number was about 2.7 billion barrels, after a previous decade of average imports well over 3 billion barrels a year[4].

> **"Who's driving this STEM train—academia, industry, or government? It's money that drives the train in this top down push for better education in science and math. But, where is the train going?"**

The *War on Poverty* began in 1964 as part of President Johnson's *Great Society*. The goal was to eliminate poverty in the U.S. At that time the poverty rate was about 19%. The government programs that were created included the Food Stamp Act of 1964, the Economic Opportunity Act of 1964, and the Elementary and Secondary Education Act of 1965. By 2012, about 126 anti-poverty programs were in operation. In 2014 this government attempt at social engineering turned 50 years old. After spending about $16 trillion during those 50 years, the poverty rate was about 15 percent[5]. The cost has significantly contributed to a national debt in 2016 of over $19 trillion.

In our industry, those of us that have been around a while have seen a common theme repeated every few years. Some person, company or government agency comes up with a catch phrase or new methodology. A new industry is generally built around this *revelation*. "You must incorporate this in your company or risk missing the train and being left at the station." The furor over the *new idea* usually lasts for a couple of years and then the gets tossed on the ash heap of tech history. Remember TCM, ISO 9000, Six-Sigma, and Lean Manufacturing? They are all still around but continue to upgraded with the next *great new idea*. When is the last time you've heard the Malcolm Baldrige Award discussed around the water cooler?

The problem is that most of this stuff is self-evident and has been just packaged repackaged in attractive ways by consultants.

For example, search the Internet for *Total Quality Management*. What you get is:

- "The 14 Principles of TQM"
- "The 3 Principles of TQM"
- "The 5 Principles of TQM"
- "The 7 Principles of TQM"
- "The 8 Principles of TQM"

And it goes on. So which one is it?

Many people quickly tire of the hype when it becomes clear that the virtue (i.e., value-added results), has become dominated more by politics, open-looped, unaccountable, grant money and consultant fees. More often than not the investment just doesn't pay back.

ISO 9000 is a good example. There are many valuable aspects of this certification, but here's what has happened in many cases. Companies usually apply for ISO 9001 certification because their customers require it, or it's thought to provide a competitive advantage to have it. The certification is not granted or performed by ISO, it is granted by one of many certification bodies.

The certification in many cases quickly becomes more important than the certification process. ISO 9000 is granted after a successful review is conducted by one of these independent qualified ISO 9000 auditors. There are many qualified ISO 9000 auditors out there to choose from, all competing for your business. There is a significant fee to take you through the process. Over time, each one informally develops a reputation as an "easy marker" or a "hard marker." Since the certification outcome is most important, the "easy marker" usually gets the business. So the auditor has a business advantage if they are perceived to be "easy markers." The real value to a company that is going through the process is to highlight and correct weak areas of its operation. However, this is lost in the overriding goal of getting the certification. "Hey, I'm paying a lot of money to go through the auditing process, I want the piece of paper."

What will cause an increase in value to a design and/or assembly operation are solid, statistically valid performance measurement techniques and an operational infrastructure that provides proactive process information. Some of these are: Quality Functional Deployment (QFD): to objectively measure the customer value of a pre-design product specification; DF MATERRS℠ (Design for Manufacturing, Assembly, Test, Environment, Repair, Reliability and Serviceability); Design of Experiments (DOE): to understand the significant assembly process independent variables and their linkage to dependent variables (process outcomes), process validation (Cpk measurement) and real time proactive automated process control (Meta Process Control)[6].

STEM education is a trap. It is a trap in the sense that all the words, good intentions, roadmaps and everything else this environment produces can lull us into a false sense of security—the delusion that the experts are fixing the problem—that they are on the case: "It's going to take some time, though—we'll get back to you, don't worry, you've got other things to do. We'll handle it."

The problem will never be solved with good intentions. The problem will never be solved until the defensiveness stops and we have the courage to confront the issue and root cause head on: In some industries the educational system has failed to produce graduates with the skill sets industry needs to successfully compete in the global marketplace.

The current academic community does not know what those skill sets are. Even if they did they could not teach them in their antiseptic environment, with instructors that have little real world experience.

And, they will continue to fail until it is recognized that the current educational system is not the source for the solution to the problem, they are the problem.

Hey, what do you have to say on this topic? I'd like to hear your thoughts. **SMT**

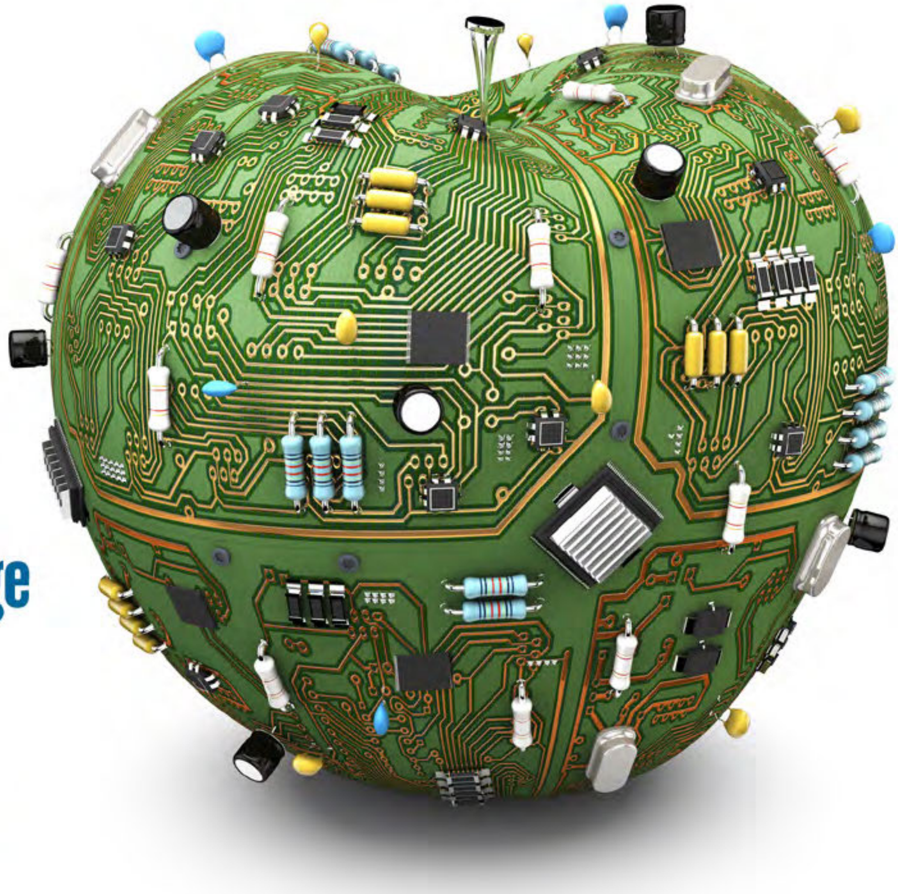
*Next Month: Paideia and Learning for Earning*

**References**


1. "... Like Holding the Wolf by the Ears ...The Key to Regaining Electronic Production Market Share: Breaking Free of the Division of Labor Manufacturing Model in High Labor Cost Global Regions," by Tom Borkes, SMTA International, Orlando, Florida, August 2008.
2. Jane J. Lee (14 February 2012). "Obama's Budget Shuffles STEM Education Deck," American Association for the Advancement of Science. Retrieved 2012-12-21.
3. SMT Magazine, May 2016.
4. U.S. Energy Information Administration
5. War on Poverty at 50 — Despite Trillions Spent, Poverty Won, by Michael Tanner, Cato Institute, January 8, 2014.
6. "Reducing Labor Content as a Strategy to Improve Competitiveness – An Analysis that Addresses the Value of Designing for Automation and an Empirical Analysis that Exploits the Automation Using META Process Control," by Tom Borkes and Lawrence Groves, Trans-Tec Yamaha, SMTA International, Chicago, IL, September 30, 2015.


**Tom Borkes** is the founder of The Jefferson Project and the forthcoming Jefferson Institute of Technology. To reach Borkes, click here.

FEATURE



# Package-on-Package Warpage Characteristics and Requirements

**by Wei Keat Loh,** INTEL MALAYSIA
**and Haley Fu,** INEMI

Electronics packaging technology has been relentlessly changing and pushing design boundaries[1-4], leading to adoption of new materials, assembly processes, ultra-small geometries, and 2.5D and 3D integration. These changes have driven multiple assembly and surface mount challenges, and among these are concerns about package warpage. Current qualification criteria and standards are not adequate to predict good yield results at first- and second-level assemblies. Furthermore, measurement methods (dimensional and test) are neither common nor up-to-date.

The International Electronics Manufacturing Initiative (iNEMI) organized the Warpage Characteristics of Organic Packages Project to identify primary factors that can contribute to the warpage performance of selected components during typical SMT processes. The project team's plan was to define a qualification method and a set of criteria (e.g., sample size, precondition, variations of material and processes at the first and second levels) that could be used to evaluate warpage characteristics of new and existing packages in the design and manufacture of products. Their objective was to better understand package warpage characteristics across different package types and attributes. The project has, to date, evaluated several types of packages. This article focuses on the work related to package-on-package (PoP).

PoP is widely used in mobile devices due to its integrated design, lower cost and faster time to market[5]. Understanding warpage characteristics and requirements of this type of package is critical to ensuring that both the top and bottom package can be mounted with minimal yield lost. The current state of PoP warpage requirements has not been reevaluated and formed in clear specification other than customer-specific requirements. The typical SMT defect modes, such as non-wet open, solder bridging, head and pillow, and non-contact open (Figure 1) are applicable to both the joints between the PoP bottom package with the board and the PoP memory package. Other gross SMT defects can occur when there are geometry interferences between the PoP packages. This shows there is a need for ensuring that the warpage between PoP bottom and memory package is compatible. Efforts to leverage the warpage character-

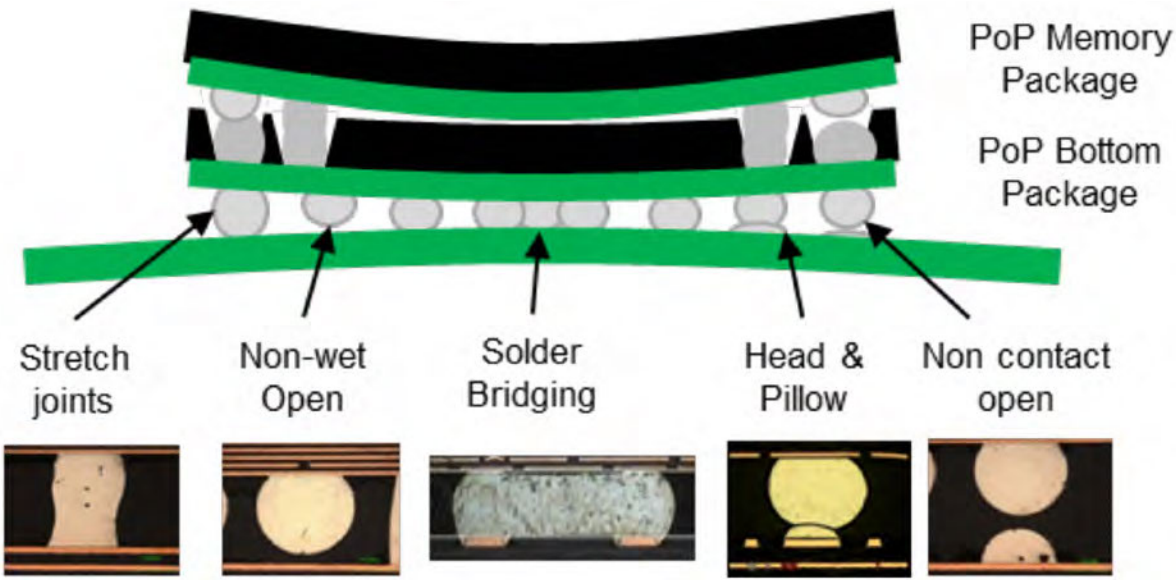



Figure 1: Typical SMT defect modes.

istics of PoP package warpage to predict SMT yield performance are highlighted by Jie[6] and Chiavone[7].

New PoP technologies continue to emerge, and iNEMI is working to establish PoP warpage characteristics and understand the effect of current measurement criteria that potentially address the component board assembly challenges. The project team's work also incorporates an evaluation of how to improve the package warpage qualification process, such as sample size used, reporting, shape definition and effect of environmental staging.

## Approach

### *Samples*

For this study, there were basically six types of PoP bottom packages with different geometry and construction, as shown in Table 1. The package size ranged from 12 x 12 mm to 14 x 16 mm, while the package thickness ranged from 500um to 600um (excluding the BGA ball height). There were a few variances of PoP memory package considered with size ranges from 12 x 12 mm to 14 x 16 mm as well.

The PoP package construction varies, depending on design choices, package thickness requirements and compatibility with PoP memory package. The samples acquired for this

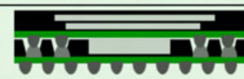
| ***PoP Design*** | ***Schematic drawing of package construction*** |
|---|---|
| Overmold TMV® |  |
| Expose Die TMV® |  |
| Bare Die POP |  |
| Interposer POP |  |
| Pre-stack POP package |  |
| MCeP® |  |
| POP Memories |  |

Table 1: PoP Packaging Technology Considered.

study were donated and limited geometrical information was given.

### *Dynamic Warpage Measurement Technique*

Electronic package warpage changes under the influence of temperature due to thermal strain mismatch among the materials used to construct the package. "Dynamic warpage" is the terminology commonly used to describe

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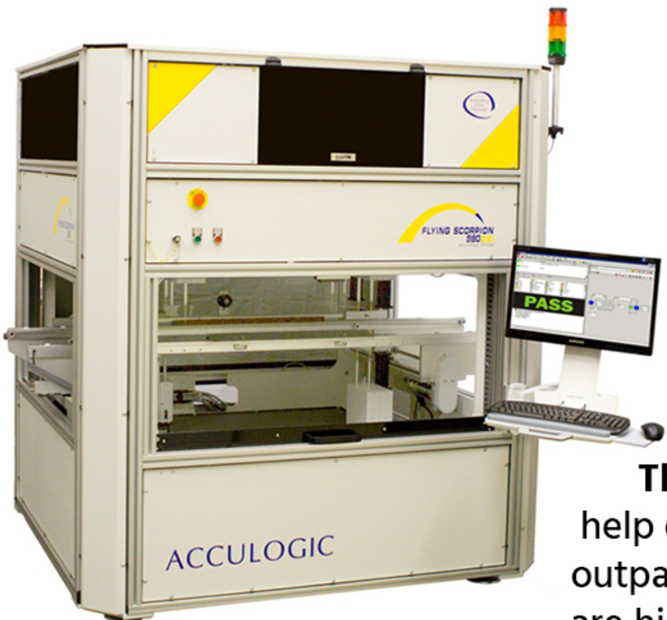


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## Flying Probe Tester

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Since flying probe testers require no test fixtures, they have few restrictions on board access, and can test boards with virtually unlimited number of nets. They also allow developers to complete test programs in a short time. For these reasons and more, flying probe testers have become indispensable tools in today's electronic manufacturing.

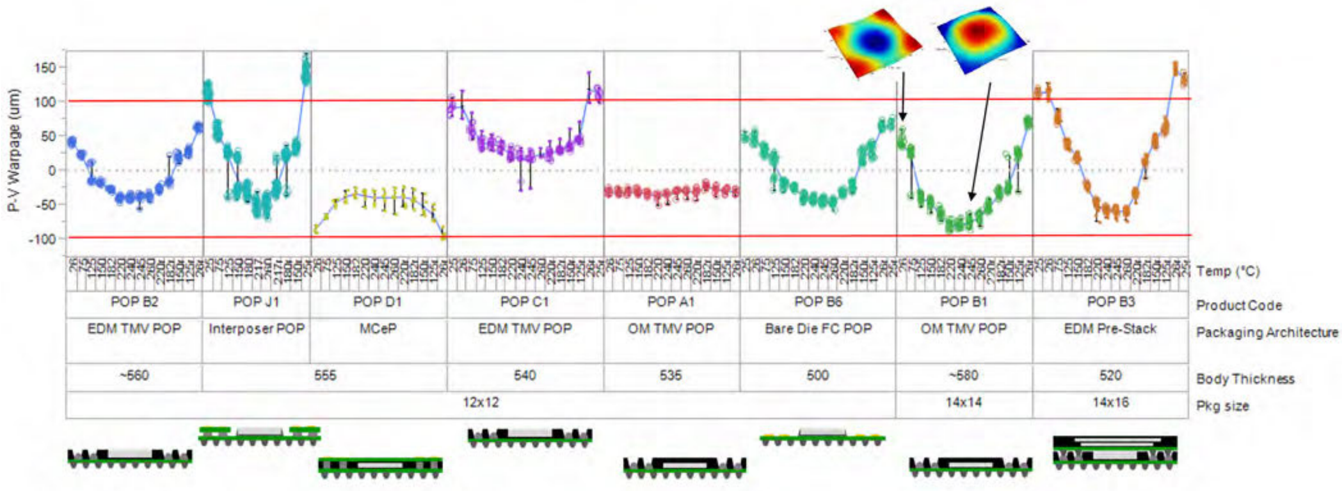


Figure 2: Dynamic warpage of PoP bottom package.

such behavior. Eslampour[5], lists many measurement tools that can be used to measure the dynamic warpage of a package. The most common tool made available for this study was the thermal shadow moiré tool. The ability to measure warpage at elevated temperature provides better risk assessment for the formation of component board assembly joints. The common convention used to define the warpage direction is based on "+" and "–" magnitude which represent convex and concave direction. However, there are shapes that are hard to determine just using these two signs.

The measurement was conducted based on the availability of the sample and perceived risk level. There were three preconditioning considerations: "as is," "bake" and "MET" (manufacturing exposure time), listed in Table 2. The purpose of these considerations is to mimic potential conditions prior to board assembly.

'As is' mimics the potential condition where packages are directly mounted to the board after taken out of sealed bags without much staging time. 'Bake' mimics the condition where the package is baked after being staged for unknown condition prior to board assembly. The baking process potentially alters the stress state of the package and removes any diffused moisture. MET nine days mimics the condition where the package is being staged in the factory floor for nine days, exposed to 30°C and 60%RH prior to component board assembly process. The typical MSL 3 calls for a maximum seven days of staging, but the work here extended to nine days to take into account any unforeseen circumstances.

| Preconditioning | Description |
|---|---|
| As Is | Units used for board assembly immediately after taken out of sealed bag. |
| Bake | Mimics condition where package moisture level being reset by baking it for 24 hours at 125°C. |
| MET 9 Days | Mimics 7 days component board assembly staging time + 2 days of unforeseen delays. Exposed to 30°C and 60%RH prior to warpage measurement. |

Table 2: Precondition.

These three precondition environments may potentially demonstrate different package warpage behavior and board assembly yield depending on the packaging technology used. Due to uneven samples acquired, some package types listed here were not subjected to all these preconditions.

### PoP Bottom and Memory Package Warpage Characteristics

The 'as is' dynamic warpage behavior for these PoP bottom packages is shown in Figure 2. It can be observed that the majority of the dynamic warpage behavior started from convex (+) at room temperature and changed to concave (–) at elevated temperature. One sample behaved in a unique way—it was concave at room temperature and less concave at elevated temperature. Other samples retained their shape of either concave or convex across the temperature range with minimal magnitude changes. Depending on the construction of the package, they exhibited different room temperature warpage magnitude ranges from ~50 µm to 150 µm, while at high temperature warpage floated more than –100 µm.


Figure 3: Effect of 'as is', Bake and MET 9 days to package warpage at room and peak reflow temperature for PoP.

The effect of Bake and MET at room temperature and 260°C are shown in Figure 3. It was determined that the package warpage was technically comparable among the preconditioning considered. There was some indication that baking the package reduced some variation of the warpage magnitude, but a more statistical approach is required to confirm this finding. In general, the data suggested that these ultra-thin packages were not sensitive to the preconditions considered, but this may not be generally applied to all PoP packages. This is because the package construction and material used can play significant roles in determining the dynamic warpage behavior and the impact of preconditioning.

As for the PoP memory package, the dynamic warpage of the individual memory with different attributes is shown in Figure 4. Depending on the memory package attributes, the dynamic warpage ranged from ~100 µm to –100 µm and exhibited different dynamic warpage characteristics depending on the construction and material sets used. Some packages showed predominantly convex shape at room temperature and became concave at higher temperature, while others could remain predominantly concave across the temperature range. The range of dynamic warpage seemed to be higher for thinner and larger package size. The reduction of ball pitch with thin package design may suggest a greater challenge in PoP component board assembly in the near future.

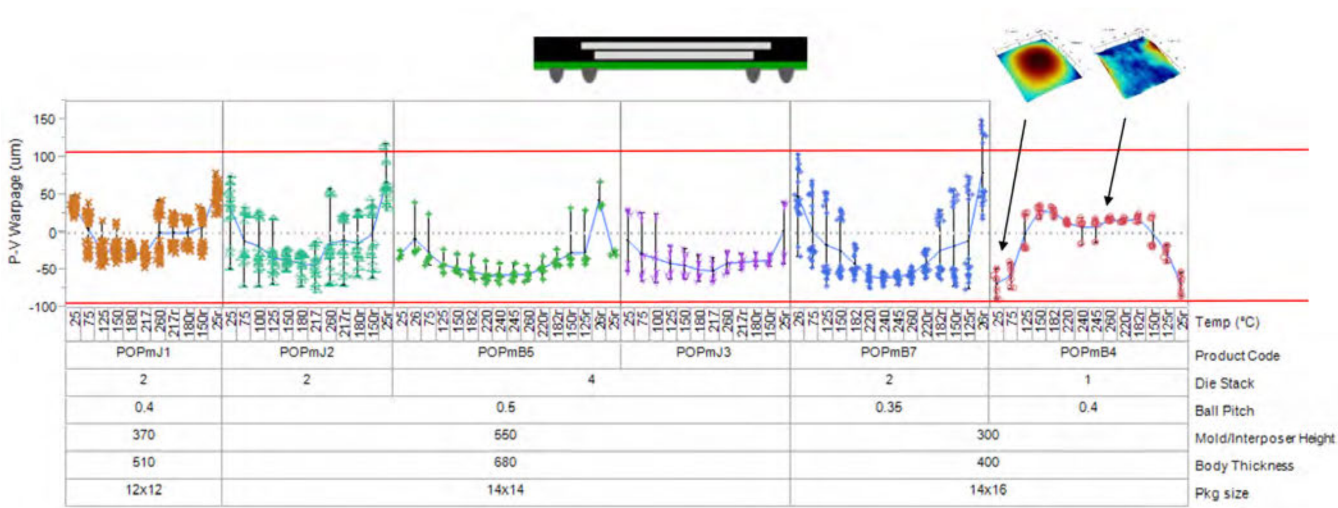


Figure 4: Dynamic warpage of PoP memory package warpage.

Based on warpage measurement defined by JESD22-B112A[8], the PoP package warpage can be extracted from just the BGA region along the peripheral edge of the PoP memory package. The peripheral warpage magnitude, as shown in Figure 5, was generally lower than the entire package area, as expected due to the smaller area of interest. The benefit of analyzing peripheral BGA warpage provided some perspective of which region of the package contributed the most warpage. For example, PoPmB5 had ~50 µm warpage for the entire package area, while <20 µm for the peripheral BGA warpage at elevated temperature. This shows that the region without BGA balls contributed part of the warpage magnitude. For PoPmB7, both package area and BGA area had approximately the same level of warpage.

Depending on the engineering assessment needed, the entire package area warpage plays a more critical role in PoP stack-up assembly because it gives better insight into any geometrical interference with PoP bottom package. However, the coplanarity specification in JEDEC Publication 95[2] only calls for measurement of the BGA area coplanarity, which may subject ambiguous correlation to PoP component board assembly yield.

As for the effect of preconditioning on PoP memory warpage, Figure 6 shows the interaction of room temperature and peak reflow temperature warpage magnitude as a function of as is, bake and MET 9 days. The room temperature warpage for PoPmB4 and PoPmB7 was affected by bake and MET preconditioning. PoPmB7 exhibited 50 µm increase in room temperature warpage while exposure to moist environment reduced the warpage. This could be due to stress relaxation that occurred during baking while the package swelled when exposed to a moist environment. However, the warpage at high temperature was not impacted among the PoP memory considered. This seems to suggest that baking- and moisture-induced warpage changes have less impact on thin packages at high temperature.

**Package Warpage Qualification Improvement Opportunity**

Based on the warpage data collected, the iNEMI project team has a fundamentally broad dataset to analyze further with respect to warpage qualification assessment. The reporting format for package warpage outlined in JESD22-B112A[8] and data reported elsewhere typically used a few samples due to limited resources and other specific constraints. When addressing board assembly yield-related issues, the limited sample used for dynamic warpage measurement may or may not explain the corresponding yield per-

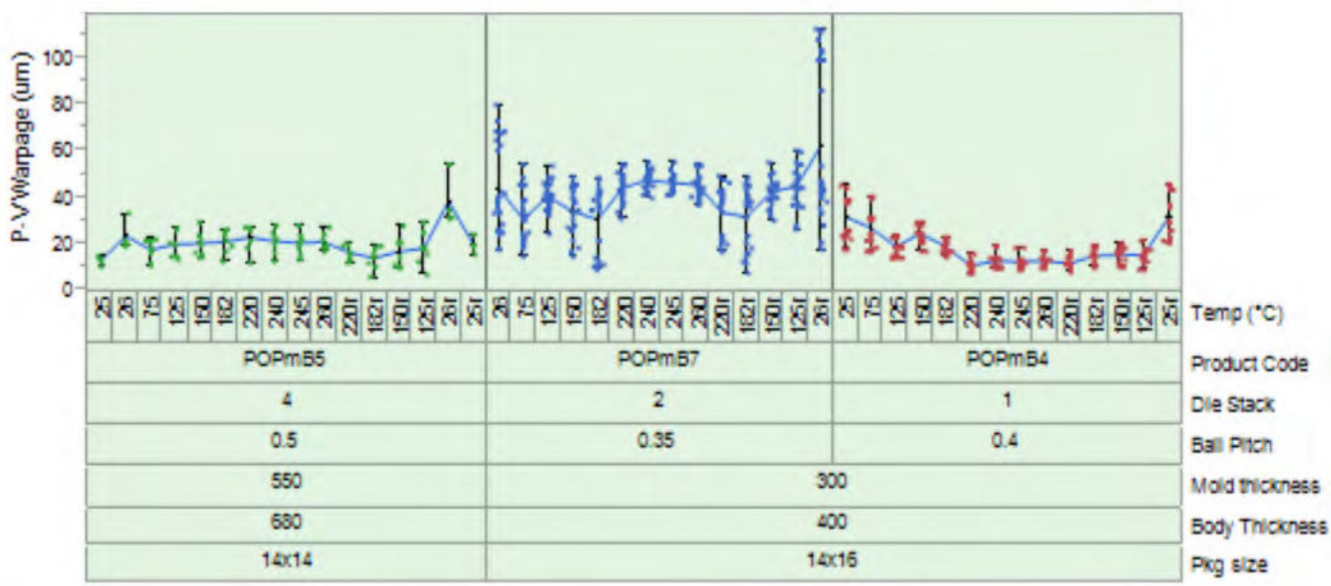


Figure 5: PoP memories package warpage for various designs. (Measurement area: BGA area only.)

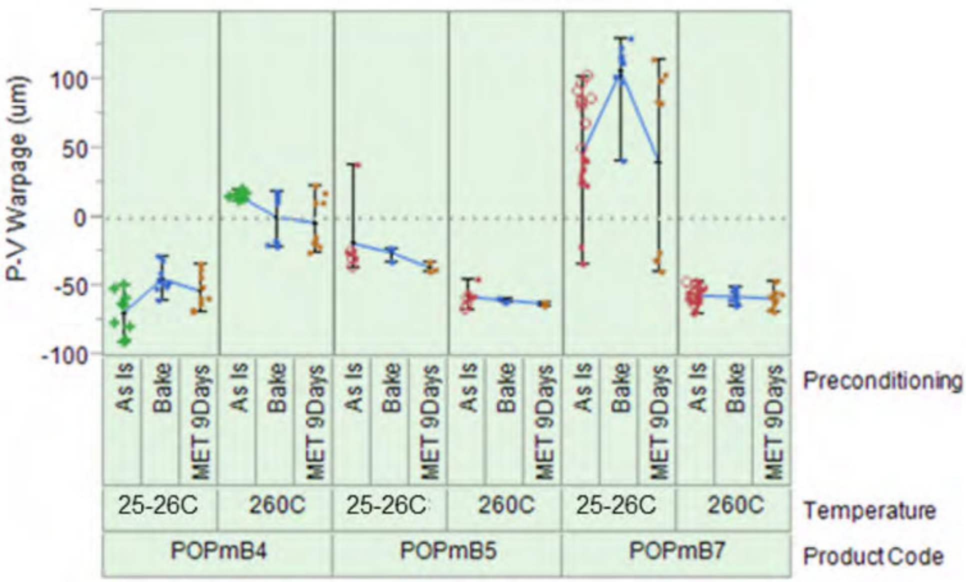


Figure 6: Effect of as is, bake, MET 9 days to package warpage at room and peak reflow temperature for PoP memory packages.

formance. Hence, some statistical method is required to determine the minimal requirement of sample size needed within allowable resources.

Figure 7 shows the warpage magnitude obtained from multiple random sampling simulations by selecting a pre-defined sample size from a pool of units. The pool of data was obtained by combining the earlier warpage measurement for as is, bake and MET 9 days for a given product candidate to capture the potential noises that may exist in a manufacturing environment. From the graph, the mean warpage and standard deviation will fluctuate more than 5% when less than five samples are chosen from the pool. The mean warpage and standard deviation are kept within 5% when sample size is nine or more. The same finding was established when repeating this sampling simulation on other products. This seems to suggest that a minimum of three samples—as stipulated in JESD22-B112A[8]—may not be enough in some cases. Furthermore, the sampling method may need to consider multiple assembly batches to establish a representation of the warpage magnitude range that is useful for component board assembly yield assessment[6, 7].

The dynamic warpage characteristics obtained for PoP bottom and PoP memory packages demonstrate that the electronic industry is creating packages with broad dynamic warpage characteristics that depend on the entire design and material set used. The warpage magnitude at peak reflow temperature can play a major role in surface mount yield, a fact with should be reflected in JEDEC or any industry guidelines. Alternatively, there are many customized component board assembly recipes that may be used to mount packages[6]. The impact of as is, bake and MET requires constant evaluation to ensure the dynamic warpage characteristics are understood. The impact of more complex warpage shapes like "M" and "W" in PoP stack-up analysis requires more focus to establish the fundamental of component board assembly yield assessment.

## Summary and Next Steps

The work here covered a very broad dynamic warpage characteristic of different PoP bottom and PoP memory packages. The impact of as is, bake and MET were quantified and requires more consistent characterization across component suppliers to establish the sensitivity to the precondition environment in order to mimic potential component board assembly. The sample size needed to establish a representation of warpage and the use of a statistical tool in package warpage reporting requires more focus if the attempt is to correlate with component board

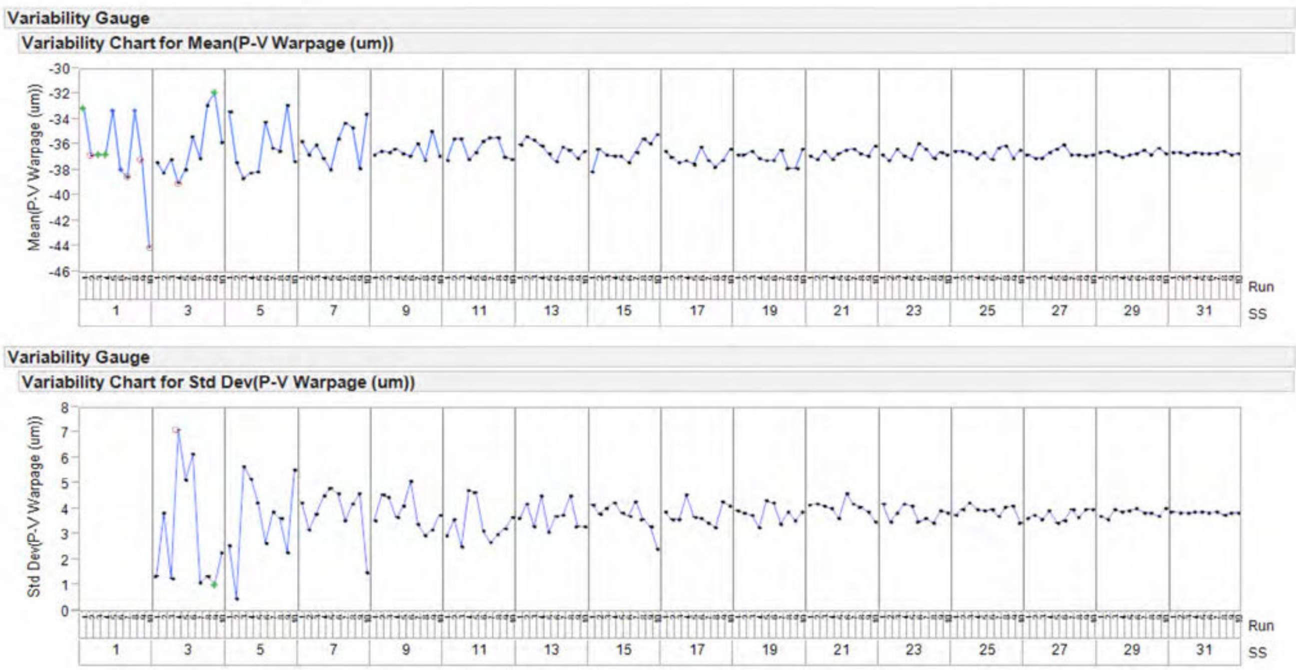


Figure 7: Effect of sample size used for dynamic warpage characterization.

assembly yield. This is because most of the yield lost may be due to extreme warpage characteristics that may not have been captured by using only a few samples. The data collected here requires further analysis to enhance the warpage qualification method. **SMT**

**References**

1. JEDEC Publication 95 Design Guide 4.22, Fine-pitch, Square Ball Grid Array Package (FBGA) Package-on-Package (PoP).

2. JEDEC Publication 95 Design Guide 4.5 Fine-Pitch Square Ball Grid Array Package & Fine-Pitch Interstitial Square Ball Grid Array Package.

3. Design Standard 4.6 Fine-pitch, Rectangular Ball Grid Array Package.

4. JEDEC Publication 95 Design Guide 4.17 BGA (Ball Grid Array) Package Measuring and Methodology.

5. Hamid Eslampour, Mukul Joshi, Seong-Won Park, HanGil Shin, JaeHan Chung, “Advancements in Package-on-Package (PoP) Technology, Delivering Performance, Form Factor & Cost Benefits in Next Generation Smartphone Processors,” Electronic Components and Technology Conference, 2013, pp. 1823–1828.

6. Dongji Xie, Dongkai Shangguan and David Geiger et.al., “Head in Pillow (HIP) and Yield Study on SIP and PoP Assembly,” Electronic Components and Technology Conference, 2009, pp.752–758.

7. Ken Chiavone, “Analyzing Package-on-Package (PoP) Reflow Assembly Interfaces with Interconnect Gap Analysis”, 36th International Electronic Manufacturing Technology Conference, 2014.

8. JESD22-B112A Oct 2009, “Package Warpage Measurement of Surface-Mounted Integrated Circuits at Elevated Temperature,” October 2009.

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# Electronics Industry News
## Market Highlights

**Over 8 Billion Connected Devices Globally**
As of year-end 2015, the world now contains 8.1 billion connected smartphones, tablets, personal computers, TVs, TV-attached devices and audio devices, according to the IHS Technology Connected Device Market Monitor report.

**Clinical Grade Wearables Accelerate Growth Opportunities for Internet of Medical Things Solutions**
New analysis from Frost & Sullivan finds the global healthcare wearable devices market earned revenues of $5.1 billion in 2015 and estimates this to reach $18.9 billion in 2020, at a CAGR of 29.9%.

**Global Pressure Sensor Market to Register 6.2% CAGR from 2014 to 2020**
The global pressure sensors market is poised to display a consistent CAGR of 6.2% from 2014 to 2020, according to a recent market study published by Transparency Market Research.

**Global Military Radars Market to Reach $13B by 2020**
The global military radars market was valued at $11.02 billion in 2015 and is projected to reach $13.04 billion by 2020, at a CAGR of 3.42% from 2015 to 2020.

**Growing Tensions Around South China Sea to Drive Defense Spending in APAC**
Rising tensions around the disputed South China Sea are expected to drive defense spending in the Asia Pacific region during the next five years. Total regional defense spending is forecast to increase by nearly 23 percent from $435 billion in 2015 to $533 billion in 2020, according to IHS Inc.

**Gartner Says Profit Opportunities Exist for PC Vendors**
The worldwide PC market registered one of its lowest quarterly growth rates in the first quarter 2016, but Gartner Inc. said several profit opportunities exist for PC vendors.

**Critical Communications Market Worth $18B by 2019**
The critical communications market, which includes police radios and other professional communications equipment, will be worth $18 billion by 2019, according to a new report from IHS.

**India Tablet Shipments Sluggish in Q1 2016**
Indian tablet market in CY Q1 2016 remained flat over previous quarter with total shipments of 0.86 million units, according to market analyst International Data Corp. (IDC).

**Graphene Electronics Market to Grow by 61% Annually from 2015 to 2025**
The global graphene electronics market will reach a valuation of $1.2 billion by 2025, increasing from $8.5 million in 2014 at a remarkable CAGR of 60.7% therein, according to a new report by Transparency Market Research.

**Energy Harvesting to Drive Semiconductor Sales to $3B by 2020**
Whether it's the IoT, wearables, or industrial automation, new devices and applications are portable, battery-operated and require continuous power. A new Semico Research report projects semiconductor sales for this market will reach $3 billion by 2020.

# Standardizing Platforms from Characterization to Production

**by Matej Krajnc**
NATIONAL INSTRUMENTS

Australia's first mobile phone call was made in a car on 9 August, 1981. It took a decade to reach the market, and it was sold for AUD $5,200. Then, it supported a single band, and it weighed and felt like a brick, for which it was famously named. Fast forward three decades: The mobile phone industry has undergone multiple disruptions caused by game-changing technologies, including the development of 4G network. The form and functionality of a mobile phone have also improved. The app ecosystems have grown, network speeds increased, and prices dipped.

However, the disruptions have also introduced new challenges for suppliers of RF components to surmount. According to a recent Databeans analyst forecast, the cost of radio frequency integrated circuits (RFICs) for mobile devices has dropped by more than 40% since 2007. This is despite the rise of device complexity. Ten years ago, a single-function GSM power amplifier was the norm. Today, many RFICs are significantly more complex. They support multiple radio standards and multiple bands with more advanced technologies such as dynamic power supplies, MIPI digital interfaces, and more.

To maintain profitable margins against lower retail prices, companies were in the past compelled to think of innovative ways to reduce the cost of semiconductor design and test. This eventually led to RFIC suppliers switching their focus on decreasing the cost of manufacturing test. Over the past decade, this intense focus has produced a significant shift from using turnkey ATE solutions to building in-house and cost-optimized testers based on off-the-shelf instrumentation. This shift to a custom tester approach has been a large factor in the success of modular instrumentation platforms like PXI in manufacturing particularly because modular instruments have shown excellent value per performance.


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**Competition and Innovation Increase Pressure on Cost**

As market competition intensifies at an ever-accelerating pace of wireless innovation, shortening the product design cycle using standardized design and test tools have become an increasingly popular strategy. In the past, product development teams often used different design and test practices and equipment in each phase of product development. Today, many companies are adopting an integrated platform approach to help reduce overlaps and in turn total test costs as well as time to market. As the 2015 McClean Report put, organizations must place greater effort into "decreasing IC design, development, and fabrication expenditures in order for the industry to maintain its continuous reduction in cost per function."

"Today, PXI instruments offer the measurement accuracy required for R&D and the speed required for manufacturing test."

Innovations in test equipment are now making the desire to use a common test platform from design to test possible. A decade ago, the test equipment engineers used in their characterization labs was unable to keep up with high-volume manufacturing test, and different tools were used throughout the product life cycle. Today, PXI instruments offer the measurement accuracy required for R&D and the speed required for manufacturing test. As a result, organizations are increasingly standardizing modular instrument platforms throughout the entire design cycle, which directly reduces the cost associated with correlating measurement results. In addition to the improved speed and measurement quality of PXI, application-specific systems, such as the NI Semiconductor Test System, build on the PXI platform by adding a rugged enclosure, fixturing, DUT control, and the turnkey software required for the semiconductor manufacturing environment.

**Mergers and Acquisitions Drive Standardization**

A series of mergers and acquisitions within the semiconductor industry have also driven the need to standardize common design and test platforms. Although the consolidation of suppliers enables companies to address a larger set of components in a particular mobile device, it uniquely impacts the engineering teams responsible for delivering products to market.

In the past, geographically distributed engineering teams set their own preferred programming languages, test strategy, and tool investments. Product development inefficiency often emerges when distributed teams do not share common best practices. Today, many organizations are in the midst of standardization. One critical focus is using a single codebase from automated measurements in R&D to automated measurements in manufacturing test. By sharing a common codebase of test software, along with using the same core measurement technology throughout the design cycle, organizations have reduced test software development cost and ultimately decreased time to market.

**Status Quo Leaves Money on the Table**

Just as the digital age commoditized digital IC, the information age is commoditizing analog IC. Commoditization comes with lower cost, and it requires a dramatically new approach to test. In an era where test strategy is considered a competitive advantage, organizations are using standardization on a common platform as a method to reduce test costs. However, an organization has a Buckley's chance of success if it does not consider a common platform approach for test. Although the old way is sometimes easier, the additional cost and inefficiency leave company profits on the table. **SMT**

**Matej Krajnc** is the managing director for ASEAN and ANZ at National Instruments.

# Selecting a Selective Soldering System, Part 4

**by Robert Voigt**
DDM NOVASTAR

In the previous three chapters on selective soldering, we covered the different applications well-suited to this technology, the various types of fluxing and soldering methods available, and nitrogen inerting. In this chapter, we'll cover programming software.

### How Selective Programming Works

Hybrid boards can be challenging to program because of the interface with SMT components and the nature and arrangement of addressable through-hole points. Figuring out the best sequence to optimize production speed is usually a combination of common sense along with available software features.

The first step is to "acquire" the board into the software, and there are a number of methods to get started:

1. Scan the bottom of the board with a flatbed scanner.
2. Take a digital photo of the board, such as with a cell phone.
3. Import data from a CAD file.
4. Teach the software.

Starting with the last one, the teach-in method is no longer widely used because it can be more difficult to manage than the other methods, which are also far more common.

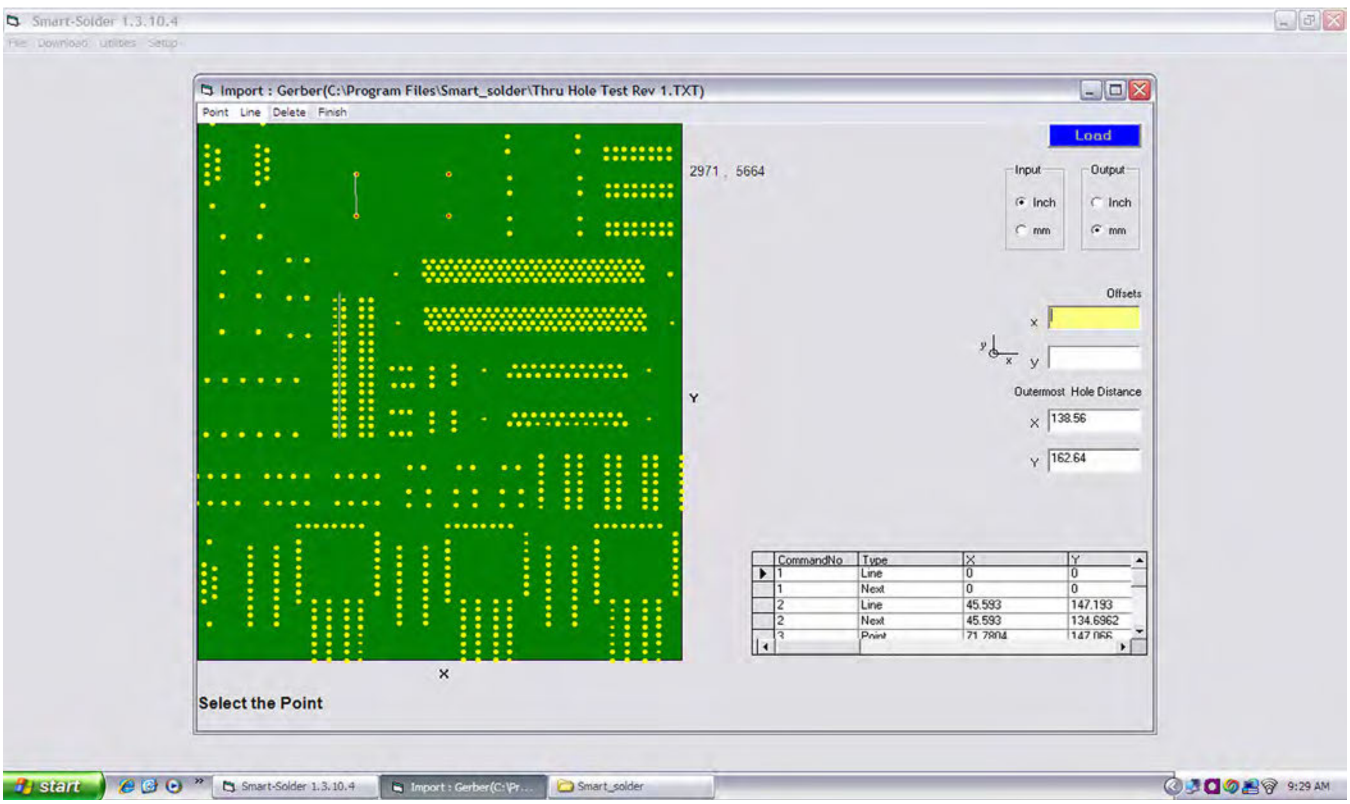


Figure 1: Example of a Gerber file.

More often than not, if a board has been designed in a CAD system, using the exported data will result in the easiest and most reliable method of importing the data. This data is known as a Gerber file, a 2D vector file that describes everything about the board for manufacturing, as well as populating and assembling them. It defines multiple layers of images that make up the board, including the size of pads, centroids, through-hole locations, etc.

Once the board has been acquired, the methods for programming the board vary widely, so evaluating the available methods against your particular processing needs will help guide the selection process. It's easy to add expensive bells and whistles, but for a low volume application or shop, they may not be necessary. On the other hand, some medium to high volume applications will benefit significantly from the time-saving options that improve productivity.

## Importing Board Data

Software for selective soldering machines is nearly always hosted on an offline PC. The idea is to import the board data, whether it's a visual representation from a scan or photo, or from a digital Gerber file, then scale its length and width on the computer screen to match the physical dimensions of the board itself. So, now that the board image has been imported into the software, it appears as an overlay of the coordinates of the points behind the board image.

With a simpler software interface, additional PCB data may need to be entered (in addition to the border and size of the board)—such as all the solder process data (temperature, preheat speed, preheat dwell), as well as the up/down Z-axis speed.

And this is where it gets tricky.

Selective solder is not just a pattern of dip points on a board. It also represents opportunities to drag solder across multiple points without changing the elevation, or height (Z), from the board. Furthermore, if nozzle changes will be necessary to accomplish some solder operations, they should be minimized to reduce dead time. On some boards, using a single nozzle to perform less efficient operations than would otherwise make sense for a different nozzle may still be faster than a time-consuming nozzle change.

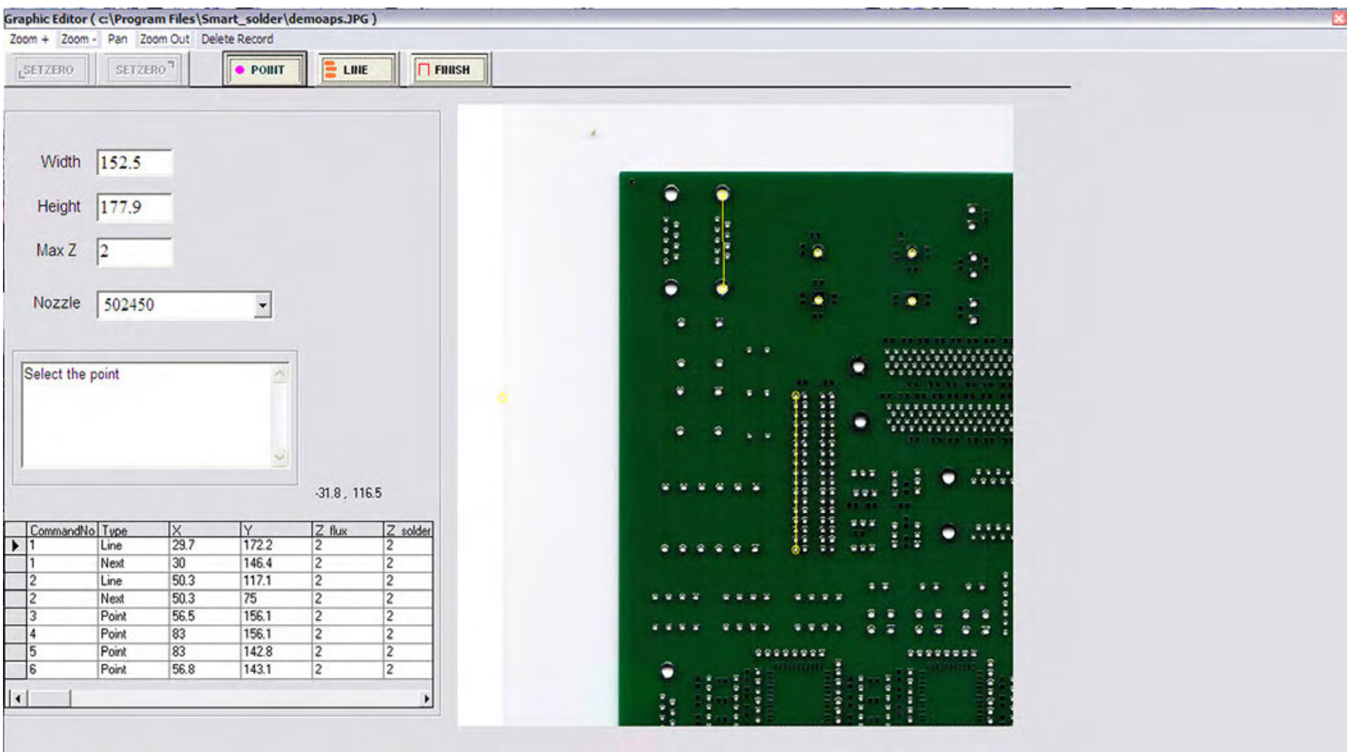


Figure 2: Programming from image file.

Figure 3: PCB data file example.

A good software package will be intuitive and easy to use. And while many of these decisions can be made by a thoughtful and experienced board programmer, some sophisticated software packages offer optimization tools to achieve the best pattern for complex board geometries. Such software packages will, along with the judgment of the operator, be capable of deciding whether changing a nozzle would be advantageous or not.

NOTE: If nozzle changes are dictated, they must be done manually. The machine interface will alert the operator any time there's a manual operation to be performed.

As the operator defines how the board will be processed, the software will prompt the user to instruct the machine what to do at each point or drag selection. Typically, the default command is to flux, preheat and solder each contact at one time, then change the nozzle height and move on to another selection; however, there may be special cases where the board design may require handling some of the operations separately. That flexibility is key if it's important for your board production.

After the board has been configured, the file is sent to the machine to begin processing. Most software programs have a menu option that allows for easy download of the saved program to the machine controller, usually via a serial, USB or Ethernet connection.

### How to Evaluate Software

The selective soldering machine you buy will always offer its own software; however, if you like the machine but its software isn't exactly what you want, you can often purchase a third-party program which can also export the formatted board back to the machine.

Any respectable machine manufacturer will offer a free demo version of their software for you to evaluate before purchase. It will allow you to see how easy (or difficult) it is to import graphics files, configure them, and program special circumstances that may arise in your production routines.

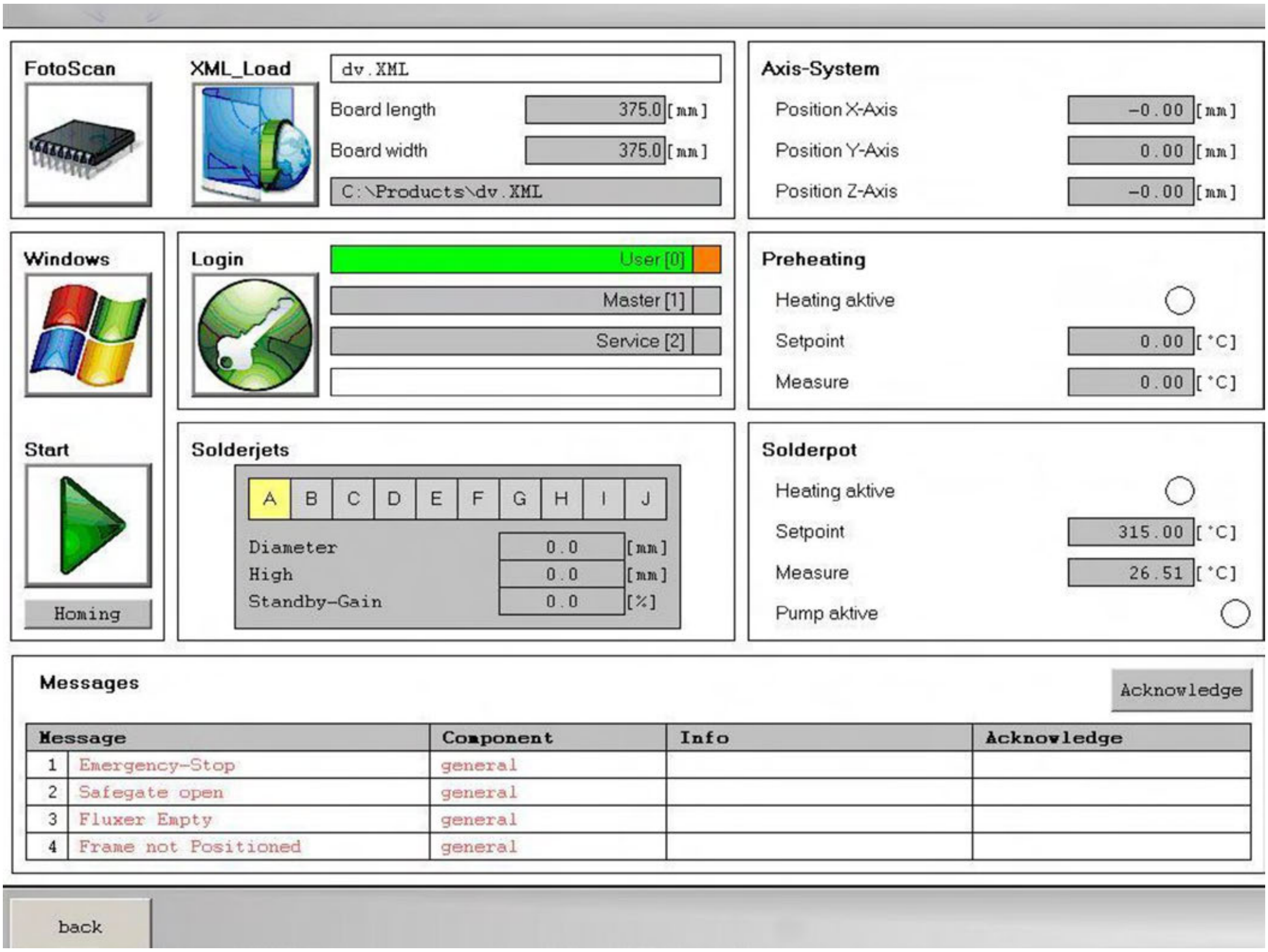

Figure 4: Easy Windows interface example.

As mentioned earlier, many suppliers offer lots of time-saving capabilities with their software, but a good rule of thumb is to test drive a number of different types to find your sweet spot, which will be a balance between performance and price. There's no need to pay more for a capability that you will rarely use. A trial will also quickly help you decide whether the software will be easy for your staff to learn.

Use patience in your evaluation process. Every manufacturer's software is very different from the other's, meaning there's very little uniformity among selective programming routines compared with what you may experience in other assembly processes. But choosing a selective machine is a major investment, and it deserves any amount of time you can afford to give it a proper evaluation.

## Check References

Remember to consult a variety of machine providers, talk to the manufacturers themselves if possible, and get references to contact before making a purchase. An important consideration for a complex machine such as a selective soldering system and associated options is factory support, specifically training, software, upgrades and spare parts. **SMT**

*Next chapter: Selective Soldering Wrap-up*

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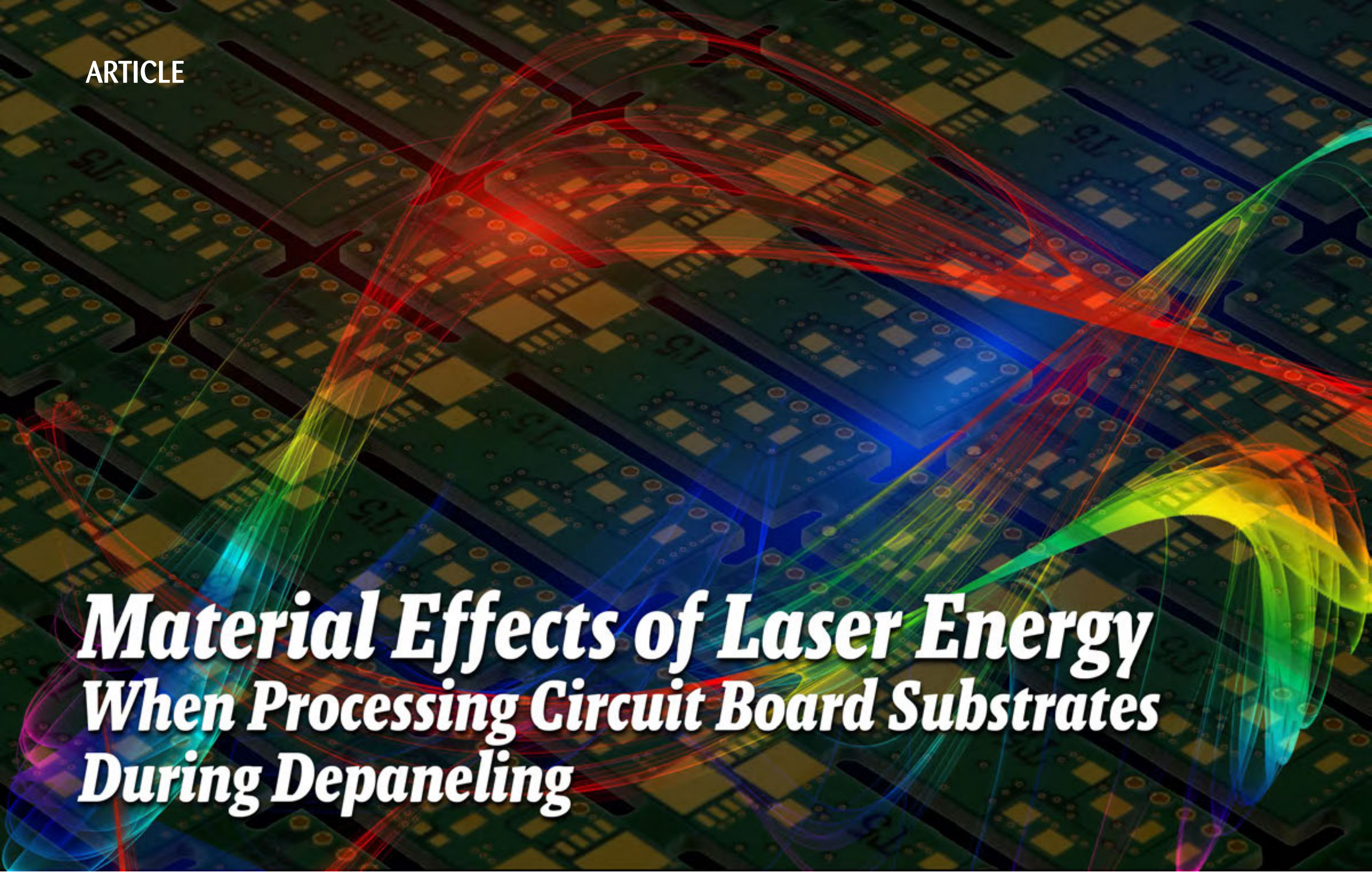


ARTICLE

# Material Effects of Laser Energy When Processing Circuit Board Substrates During Depaneling

**by Ahne Oosterhof**
EASTWOOD CONSULTING

Using modern laser systems for the depanelization of circuit boards can create some challenges for the production engineer when it is compared to traditional mechanical singulation methods. Understanding the effects of the laser energy to the substrate material properly is essential in order to take advantage of the technology without creating unintended side effects. This paper presents an in-depth analysis of the various laser system operating parameters that were performed to determine the resulting substrate material temperature changes. A theoretical model was developed and compared to actual measurements. The investigation includes how the temperature increase resulting from laser energy during depaneling affects the properties of the PCB substrate, which varies from no measurable change to a lowering of the surface resistance of the cut wall depending on the cutting parameters. In addition, the amount and properties of the ejecta that are potentially resulting from the laser processing is investigated. Understanding the composition and quantity of any resulting residue may have a great impact to both the board design and the selection of the appropriate circuit board singulation method that will achieve the best possible results. An energy dispersive X-ray analysis method (EDX) was performed to investigate if any unwanted material compounds are present on the cutting sidewalls of an FR4 circuit board substrate as a result of laser energy induced during the depaneling process.

## Depaneling Methods

Many depaneling methods are being used in the industry, such as:

1. punching/die cutting
2. v-scoring
3. wheel cutting/pizza cutter
4. sawing
5. water jet
6. routing (+nibbling)

Some of these are useful only in very low cost, minimal quality applications; others can only be used for rectangular boards. Several can

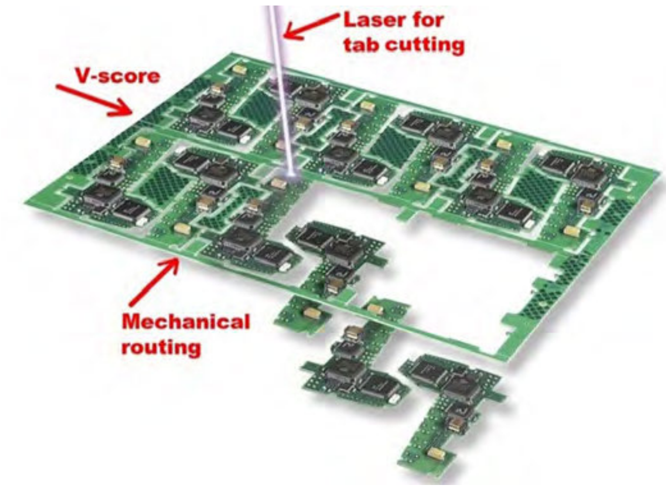



Figure 1: Combining various singulation methods in the one panel.

do damage to the board edges because of significant pressure and/or bending forces potentially causing some delamination which may impact long-term reliability. All this means that during the board layout care must be exercised to keep fragile components and sometimes circuit traces away from board edges. And the waterjet method has hardly been explored.

The most commonly used method is the routing where a kerf is cut around each board, regardless of board shape, by the panel manufacturer. To keep the board in the panel during the assembly process in a few locations the kerf is interrupted. The routed kerf in the panel typically is about 3 mm wide, which means that in a case with many small boards a significant amount of panel space is used for cutting slots. Sometimes, with many slots in the panel, the panel becomes less rigid and panel supports or a pallet is required during the assembly process. Typically, holes are being drilled in the connected areas to make it easier to break the boards from the panel which means that during board layout these locations must be decided and fragile components must be kept away from them.

### Laser Cutting

The latest method added is laser routing, which can be done after the last step in the board assembly process. This means the panel retains its rigidity throughout the previous assembly steps. Like a router, the laser cuts completely through the board, so no bending or pressing on the edges of the board occurs, which means no stresses are exerted on the board material. With the use of a laser, cutting any board shape can be accommodated, and the changeover to different boards is very quick as the process is completely computer controlled.

### Laser System

The three main parts of a laser cutting system are the laser, the X-Y table for panel movement and the scanner to move and locate the beam.

To cut various materials, several types of lasers are available. These have varied from CO2 at about 10 um wavelength available for well more than 20 years to UV lasers at about 350 nm wavelength showing up around 10 years ago. About 20 years ago the Nd:YAG lasers at 1054 nm wavelength were introduced to be used in stainless steel stencil cutting systems.

As the wavelength gets shorter the lasers have been more difficult to be produced economically, which has led to the gradual timewise availability of the different systems. Shorter wavelength lasers and those with very short pulse widths have typically been much more expensive, which is why it has taken time to get them deployed in the industry.

Figure 2: Example of a laser depaneling system in an in-line setting for automatic loading and unloading.

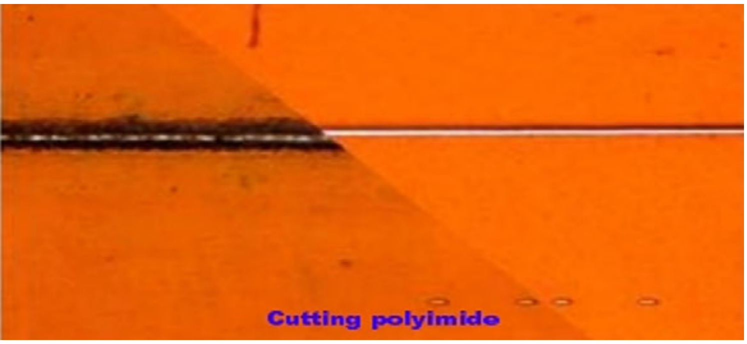



Figure 3: Infrared cut versus ultra violet cut.

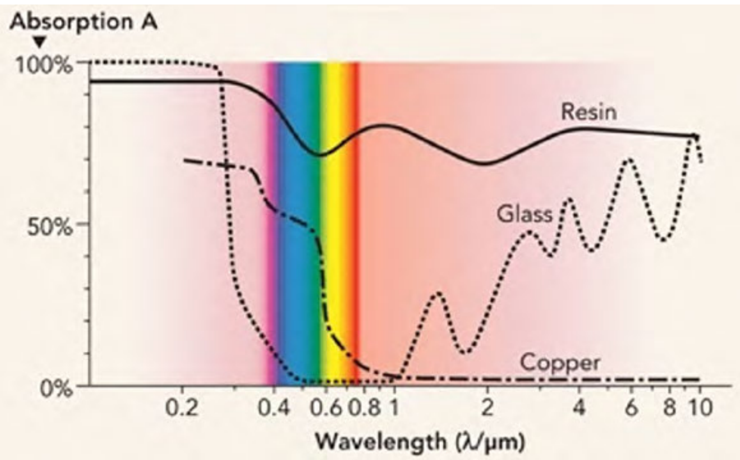



Figure 4: Reaction of various circuit board constituents with different wavelengths.

Infrared lasers can be called “hot” lasers as they heat and burn a path in the material to be cut. With UV lasers it is possible to ablate the material. A short high-energy pulse enters the top layer of the material and evaporates and explosively removes a layer of the material. By going over the same path several times, ultimately a cut is obtained through the material. As very little heat is produced by the UV beam, there is very little or no burned material on the edges of the cut depending on how the laser is being used (Figure 3).

Depending on the wavelength of the light, some materials reflect it and some are completely transparent. For the ablation method to work, the laser beam has to penetrate into the material to be cut. Figure 4 shows how various circuit board constituents react with different wavelengths. To be able to ablate all of them the UV laser is a good choice. UV lasers (wavelength ~350 nm) have become economically attractive only for the past 10 years.

Shorter wavelength and excellent optics allow for a very small beam size, often around 15 to 25 µm. This allows cutting a very narrow kerf in the panel resulting in minimal waste between boards, especially as the mechanics of the system allow very precise beam location. The example in Figure 5 shows part of a panel with very small boards. When the routing process was used the number of boards per panel was approximately 125, and after re-layout of the panel to use laser cutting the number of boards increased almost three-fold. This resulted in a very significant economic advantage.

In the laser system used in this example, a panel is placed on a perforated surface with downdraft, or mechanically mounted on the high precision X-Y movable table to prevent the panel from moving during the cutting operation. For boards with components on both sides a special support pallet is required.

To cut all the paths on a panel the area is divided in blocks of 50 x 50 mm in which the laser beam is moving using precision computer controlled mirrors mounted on galvanometers. The beam movement speed within this area is well controlled and can be as high as 1000 mm/s. While cutting, airflow passes across the panel as shown in Figure 6 to remove debris and

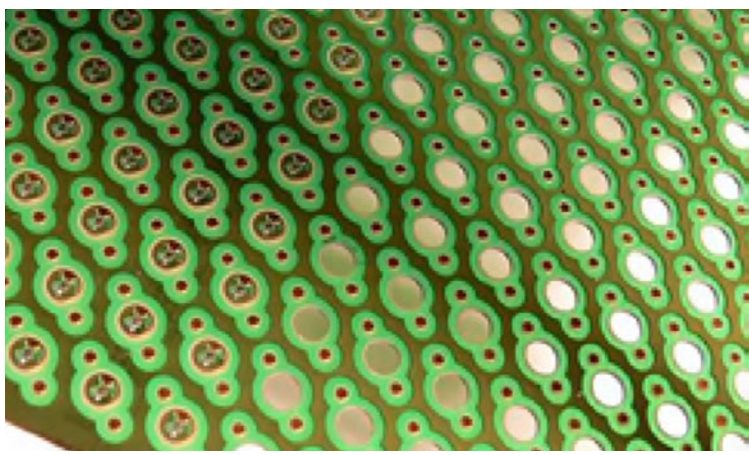


Figure 5: Example for a panel with very small circuits.

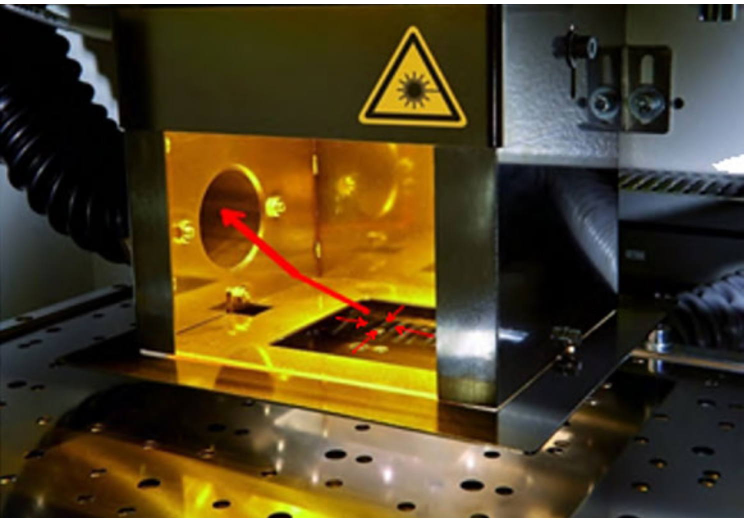


Figure 6: Airflow and exhaust.

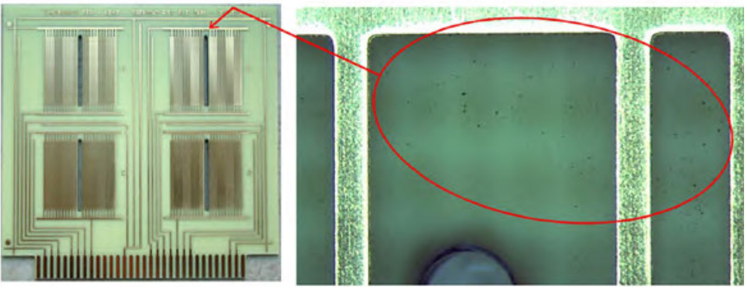


Figure 7: Surface after laser cutting.

minimizing any deposits on top of the panel. When the cutting inside the 50 x 50 mm area is finished, the table is moved to the next square until the project is finished.

**Location precision**

From the original design data (e.g., Gerber file) the laser system can use panel fiducials to locate where the cut is intended to go. The table movement, in conjunction with the galvo movements, is computer controlled and allows the beam to be located within 25 µm of where it is supposed to be. However, when singulating boards or flex circuits, the precision of the panel image is typically less and therefore it often becomes necessary to use additional fiducials for smaller portions of the panel. It is even possible to use recognizable sections of the board pattern for more precise board edge location requirements.

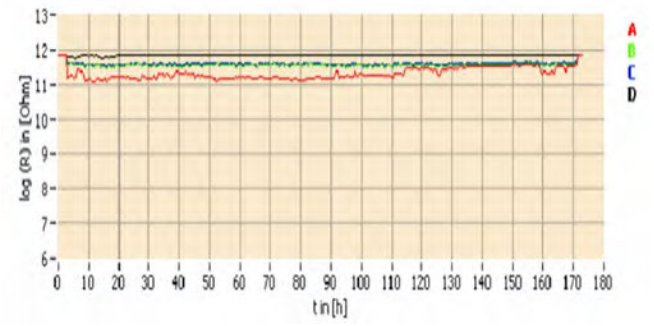



Figure 8: Surface resistance measurement.

**Residue on Board Surface**

Even though an airflow passes across the area being cut (Figure 6), not all of the material expelled from the kerf is caught. Some remaining particles are powdered epoxy and glass particles. None of these are measured to be larger than 20 µm and they averaged around 10 µm. (For reference see the circled area in Figure 7.) Their size and quantity should not raise any concerns.

But to determine if the redeposited material can cause any problems, a test board was designed made of FR4 material, 800 µm thick (Figure 7). The test board had four patterns with sets of two groups of interdigitized fingers. Each pair of these fingers was connected to the edge of the board for easy measurement of the surface insulation resistance (SIR). As part of the test, a slot was cut in close proximity to the fingers. After cutting the slot, these test boards were subjected to a climate test (40°C, RH=93%, no condensation) for 170 hours and the SIR was measured. In all measurements, the values exceeded 10E11 ohm—indicating that the SIR is not negatively impacted (Figure 8).

If so desired, a simple cleaning process can be added and will remove the remaining particles. This can be done by wiping with a smooth dry or wet tissue, using compressed air or brushes.

**Thermal Effects**

Even though UV laser can be called "cold" lasers, there still is some heat being generated. Its impact is very dependent on the settings of the laser system. The laser beam inserts some heat into the material being cut and heat is be-

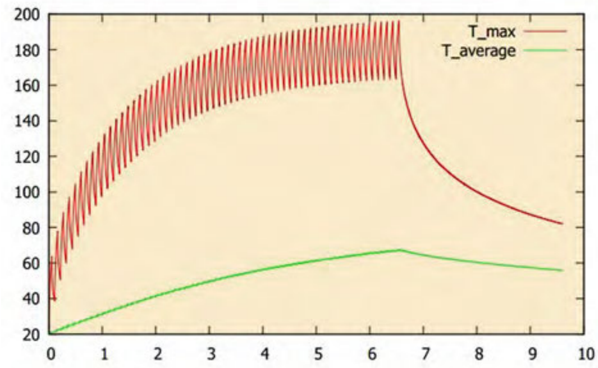



Figure 9: Simulation of heat accumulation.

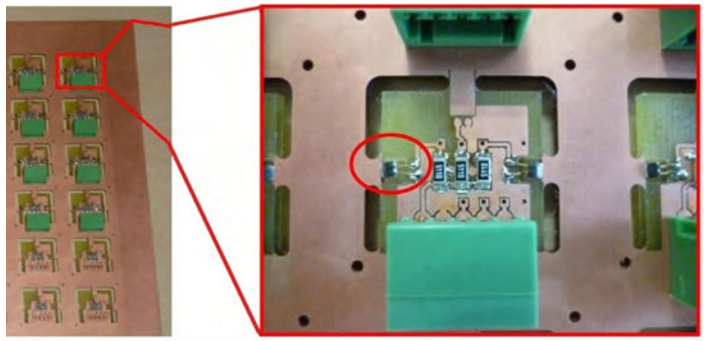


Figure 10: Linear temperature sensors (circled) on the test board.

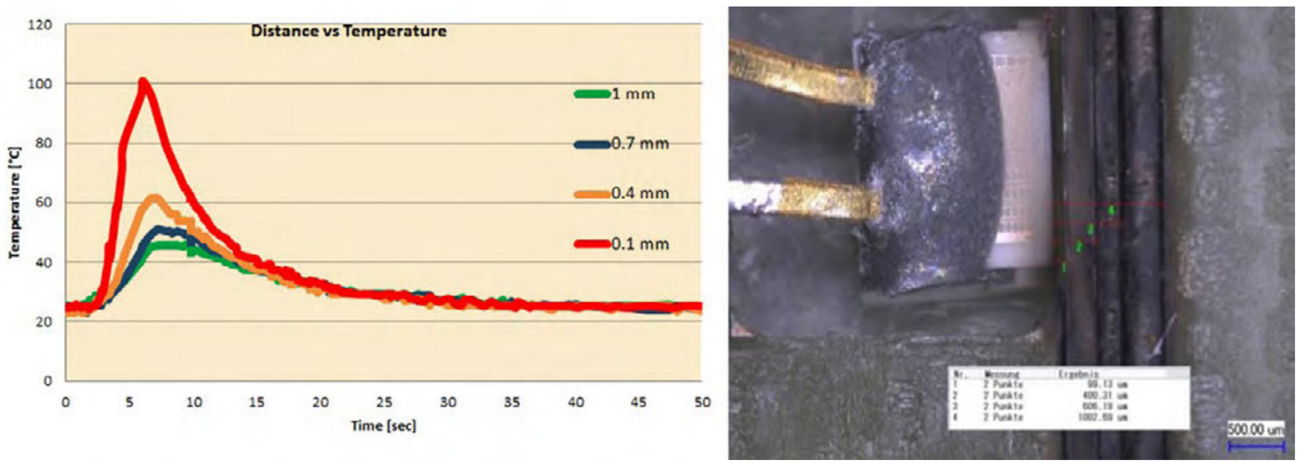



Figure 11: Cutting in one material type, measuring at different distances.

ing removed by dispersion into the material, radiation into the environment and convection into the air using forced air flow over the material.

The heat equation is a parabolic partial differential equation that describes the distribution of temperature in a given region over time.

$$\frac{\partial u}{\partial t} = \beta\frac{\partial^2 u}{\partial x^2} - \alpha(u^4 - u_0^4) + q(x,t) \quad \text{Equation 1}$$

The resulting graph (Figure 9) shows the gradual increase in temperature for multiple passes with the laser beam along a cutting path. Ultimately a balance will be reached between applying heat and dispersing, radiating and convection of heat away from the cut area.

In order to determine what actually occurs in the circuit board material near the kerf cut by the laser, linear temperature sensors were placed on a test board (Figure 10).

In this test, the tabs were cut, some of which are bare FR4, some are FR4 with copper and some are FR4 without the routed slots and the nearby temperature rise was measured.

The tabs where the sensors were placed were cut with the cutting path at different distances from the sensor. Even when cutting within 0.1 mm from the sensor, the temperature reached only 100°C, well below any temperature the board is normally being exposed to during the soldering process.

The cutting parameters for this example were: P = 12.4W, v=244 mrn/s, rep = 30, CT = 100 ms, full-cut FR4 (thickness 400-450 µm).

Cooling time (CT) is the time it takes for the beam to return to the same location. During this time other sections of the outline are being

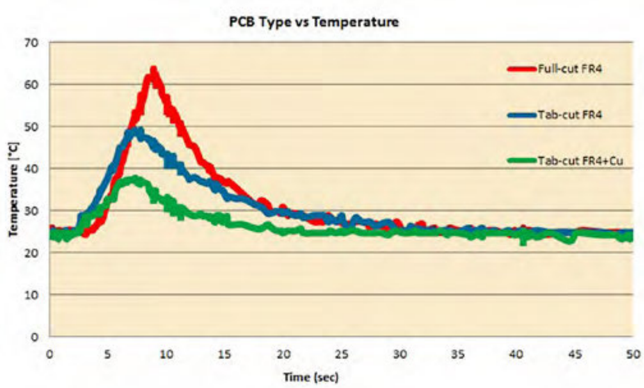



Figure 12: Comparing temperatures in different materials.

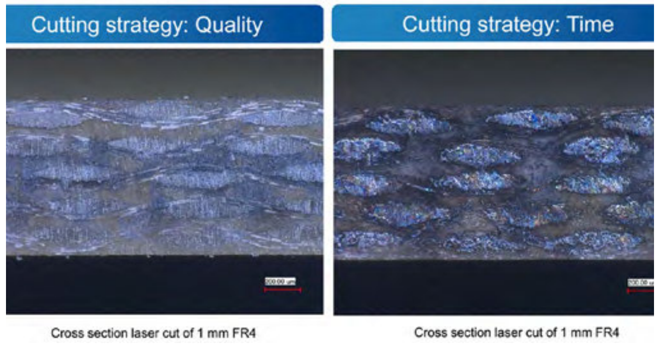



Figure 13: Visual difference between high quality/ low speed and fast speed/lower quality.

cut and it can also include a rest period between repetitions. The cooling time in this example was 100 ms.

To compare examples of cutting through the different materials, bare FR4, FR4 with copper and a full-cut FR4 were investigated, with the results showing in Figure 12.

Because different efforts are needed to cut through different materials, different cutting times result and for the more difficult situations higher temperatures are being measured. Still the temperatures at a distance of about 0.1 mm remain quite acceptable.

## Quality vs. Time

As mentioned, the laser beam does apply some heat to the workpiece. In order to minimize the impact of the heat the beam is scanned multiple times over the cutting path to distribute and minimize heat build-up. For this reason, the beam control system allows adjustment of the movement speed and beam power, but it is also possible to insert rest periods between cutting paths. These rest periods are more important when the cutting path is short and the beam would be back in the same location more quickly.

When board layout and component placement are done well away from the sides of the individual boards, the cleanliness of the sidewalls is of less concern and the laser parameters can be selected for maximum cutting speed, meaning higher beam power, faster beam speed and shorter rest periods between cutting paths.

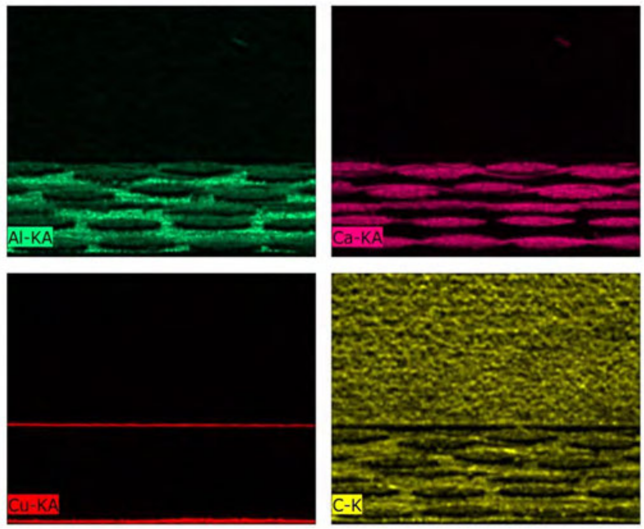



Figure 14: Polished and cleaned sidewall.

On the other hand, when the cleanliness of the sidewall is critical, more care has to be taken in the selection of the machine settings. Figure 13 presents a visual difference between these two strategies.

## Surface Analysis

To determine the spectrum of chemical components left on the cut surface the energy dispersive X-ray (EDX) analysis method was performed. For reference a routed sidewall was carefully polished and cleaned to show the normal composition of a board. Spectral lines from four chemical components are displayed in false color for the polished sidewall (Figure 14) and

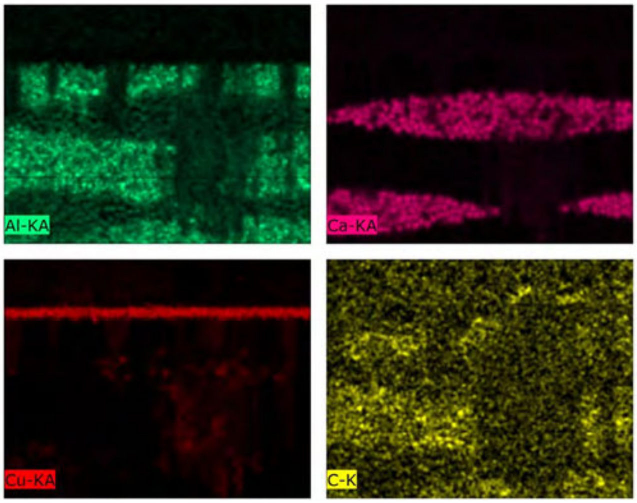



Figure 15: Untreated laser-cut sidewall.

for the laser cut sidewall (Figure 15). The variation is too small to expect significant issues.

### Pin-point EDX Analysis

Additional EDX probing was done on cut walls of boards with different thicknesses and with differences in laser system setups. From those, ones were selected for an 800 µm board (33 mil) cut with setup conditions as in Table 1 and comparing those to a cut made in a similar board which was depaneled with a router.

A finely focused beam was used to be able to measure the chemical components on the epoxy and also on the glass fibers. In the tests, probes 3 and 4 are done with different cooling

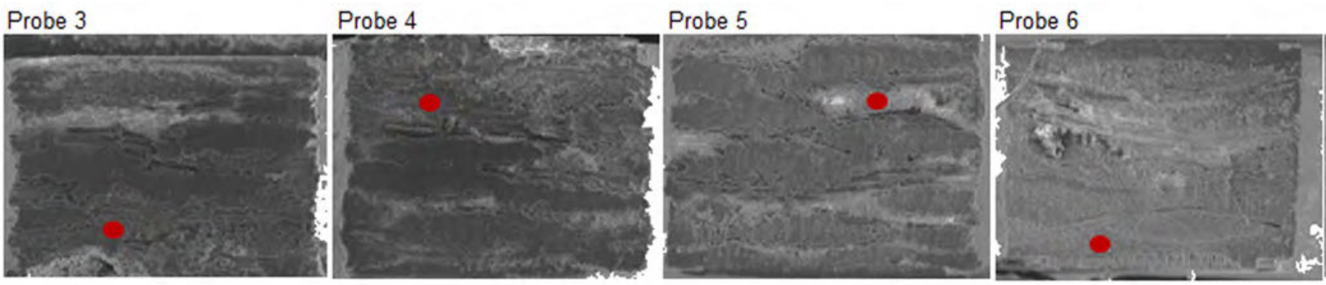



Figure 16: Inspecting epoxy areas.

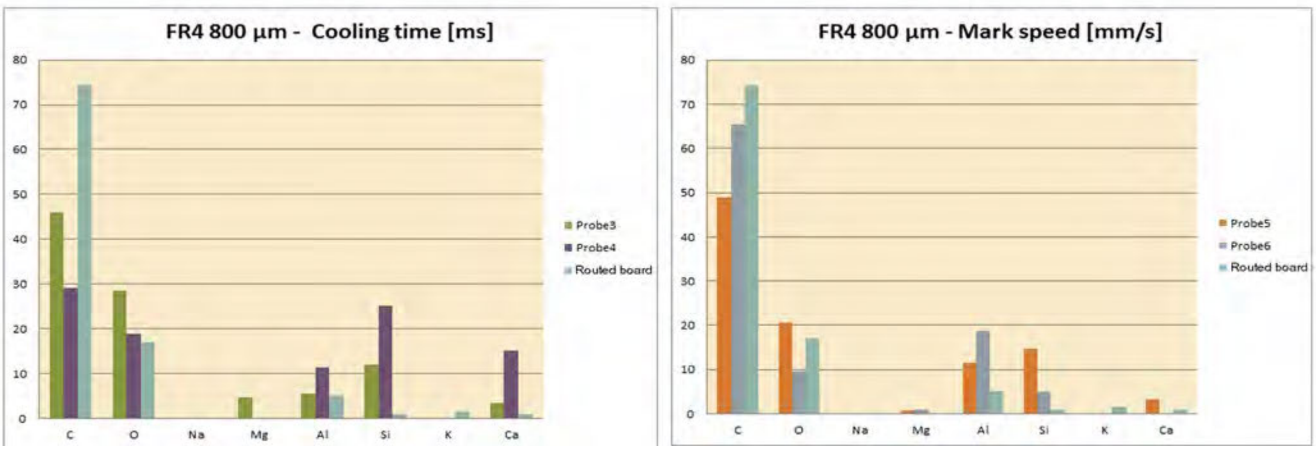



Figure 17: EDX analysis epoxy area.

| | P [W] | f [KHz] | v [mm/s] | Repetition [x] | Cooling time [ms] | FR4 Thickness [µm] |
|---|---|---|---|---|---|---|
| Probe6 | 12,4 | 40 | 600 | 180 | 300 | 800 |
| Probe5 | 12,4 | 40 | 100 | 30 | 300 | 800 |
| Probe4 | 12,4 | 40 | 244 | 35 | 385 | 800 |
| Probe3 | 12,4 | 40 | 244 | 35 | 175 | 800 |

Table 1. Comparison between cut walls of boards with setup conditions and boards depaneled with a router.

(or rest) times between passes thereby allowing the surface to remain cooler.

Figure 17 shows that with shorter cooling times a slightly higher amount of carbon and oxygen are present.

For probes 5 and 6 the cutting speed was changed significantly, which means that with the slower speed a complete cut is obtained with fewer repetitions. With the higher cutting speed more carbon and less oxygen remains present.

All the tests were compared to a routed side wall where in each case more carbon was present there while the amount of oxygen did not vary significantly.

The chemical element that would raise most concern is carbon, yet in all these laser cut cases, the presence of this element is lower or at most similar to that in the routed board.

## Conclusions

Using a laser for depaneling can have significant economic advantages because more boards can be placed on the same panel. But also one can expect better long-term reliability as the board's edges are not exposed to bending strain when breaking the last connecting points to the panel.

In addition, the board edges are not seeing high levels of compression when they are being cut. The panels retain their original rigidity during assembly which may make it possible to work without pallets.

During the laser cutting, process temperatures near the edges are lower than temperatures encountered during soldering and therefore no negative impacts are detected. When the cutting is well controlled by the system operator, no carbonization occurs, which otherwise might reduce the surface resistance of the cut edge.

Finally, the high precision of locating the outline of the board insures that the cuts do not encroach into the areas of the board where runs or even components are located and also assure a proper fit in a tight and well-designed enclosure.

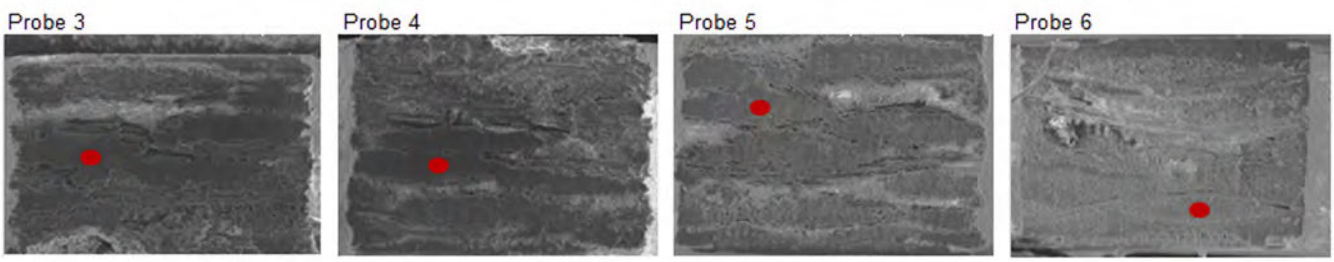



Figure 18: Inspecting surface of glass fibers.

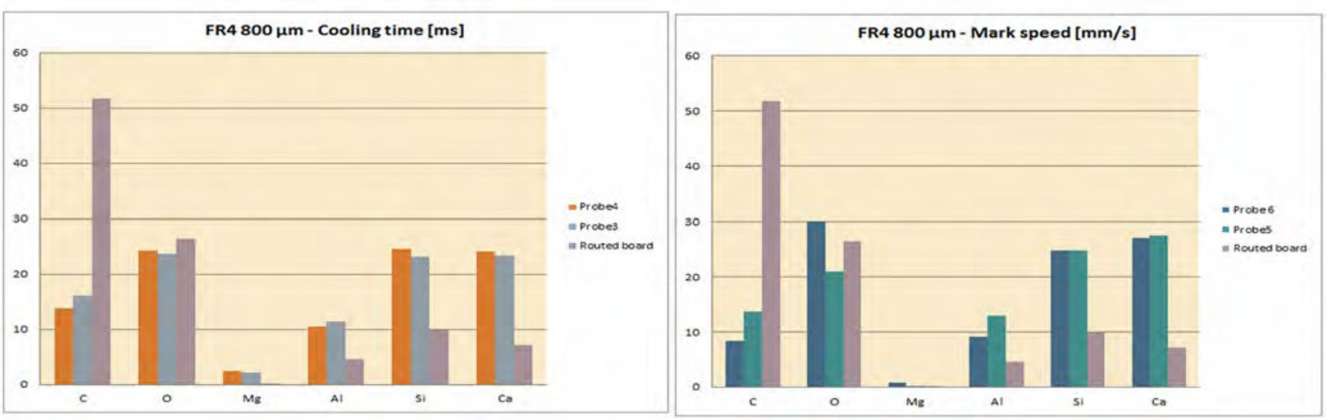



Figure 19: EDX analysis on glass area.

**Acknowledgements**

The author would like to acknowledge the images provided in the paper by LPKF USA and LPKF Laser & Electronics AG, Garbsen, Germany. **SMT**

**General References**

1. "Laser Ablation—Cutting systems for the Electronics Industry," Ahne Oosterhof, Mark Hueske, Dieter Meier; Industrial Laser Solutions, June 2007.

2. "Flex Circuit Depaneling: How UV Lasers Meet Today's Trends," Shane Stafford, Industrial Laser Solutions, September 2012.

3. "Laser Cutting of Printed Circuit Boards: Evaluation of possible corrosive effects of residuals using SIR-test and optical inspection," Manfred Zäske, Siemens AG, CT RTC ELE EOM-DE, June 2013.

**Ahne Oosterhof** currently consults for LPKF Laser & Electronics North America.

# New Nanomaterial Offers Promise in Bendable, Wearable Electronic Devices

An ultrathin film that is both transparent and highly conductive to electric current has been produced by a cheap and simple method devised by an international team of nanomaterials researchers from the University of Illinois at Chicago and Korea University.

The film—a mat of tangled nanofiber, electroplated to form a "self-junctioned copper nano-chicken wire"—is also bendable and stretchable, offering potential applications in roll-up touchscreen displays, wearable electronics, flexible solar cells and electronic skin.

The new film establishes a "world-record combination of high transparency and low electrical resistance," the latter at least 10-fold greater than the previous existing record, said Sam Yoon, a professor of mechanical engineering at Korea University and one of two corresponding authors on the publication.

The film also retains its properties after repeated cycles of severe stretching or bending, according to Alexander Yarin, UIC Distinguished Professor of Mechanical Engineering and one of the corresponding authors.

Manufacture begins by electrospinning a nanofiber mat of polyacrylonitrile, or PAN. The fiber shoots out like a rapidly coiling noodle, which when deposited onto a surface intersects itself a million times.

The naked PAN polymer doesn't conduct, so it must first be spatter-coated with a metal to attract metal ions. The fiber is then electroplated with copper—or silver, nickel or gold.

"We can then take the metal-plated fibers and transfer to any surface—the skin of the hand, a leaf, or glass," Yarin said. An additional application may be as a nano-textured surface that dramatically increases cooling efficiency.

Yoon said the "self-fusion" by electroplating at the fiber junctions "dramatically reduced the contact resistance." Yarin noted that the metal-plated junctions facilitated percolation of the electric current and also account for the nanomaterial's physical resiliency.

# A New Dispensing Solder Paste for Laser Soldering Technology

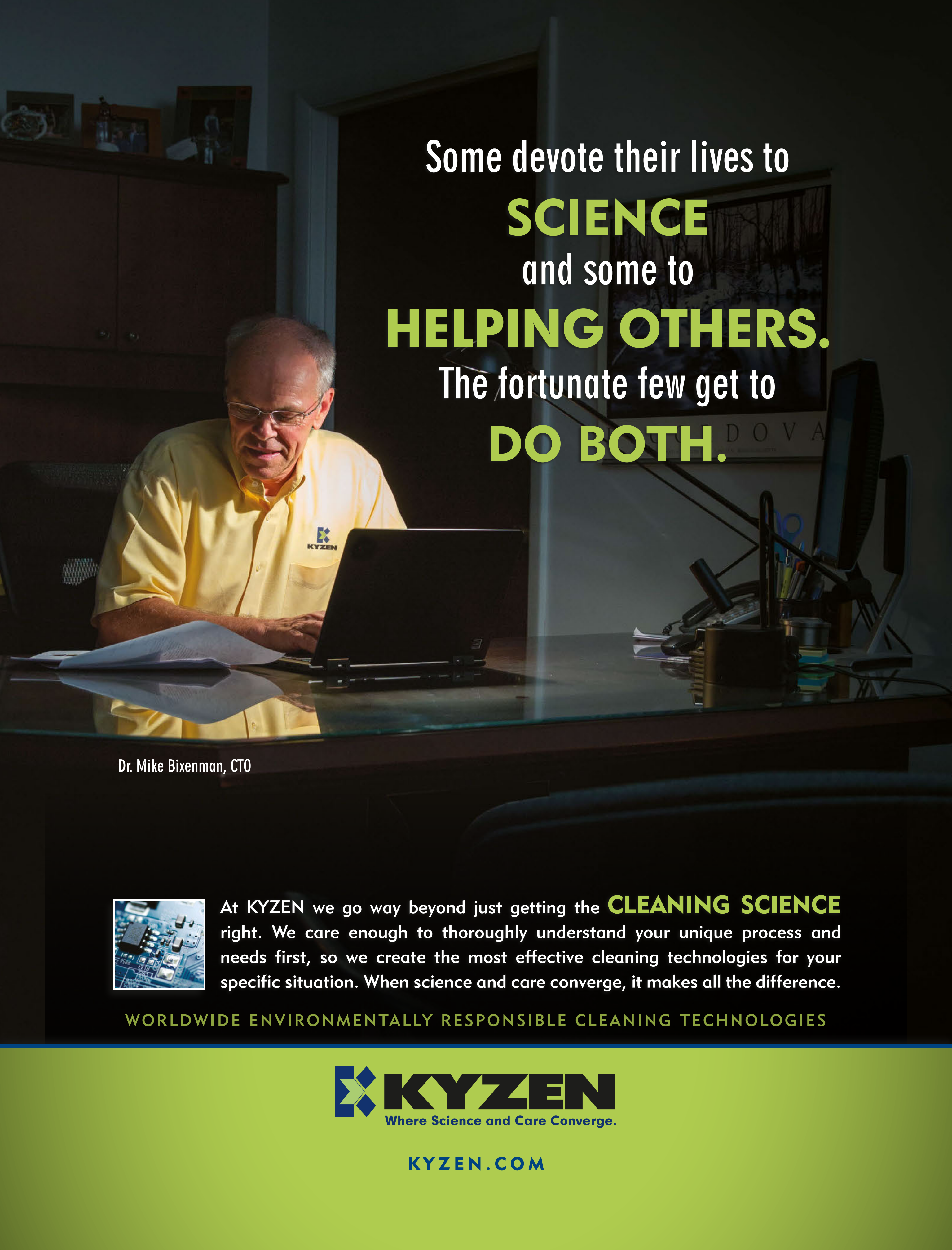
**by Hsiang-Chuan Chen, Ya-Ching Chuang, Jen-Yio Shiu, and Chang-Meng Wang,**
SHENMAO TECHNOLOGY INC.
**and Watson Tseng,**
SHENMAO AMERICA INC.

**Abstract**

Laser soldering method becomes attractive in the packaging and assembly of surface-mounted devices and microelectronics. The method transfers laser energy for reflow process with a non-contact procedure and determines the soldering location precisely. It is critical to consider formulated solder paste due to the amount of heat absorbed by flux and alloys when applying the method to reliable joints. A new solder paste of alloy composition of Sn-3.0Ag-0.5Cu in a dispensing way is developed for the automatic laser soldering processes. This paper presents the results of soldering BGA spheres on circuit boards with minimal voiding and no splash or solder balling issues. Cross-sectional studies showed the reduction of intermetallic formation in well-formed solder joints. In addition, the joints have high shear strength due to lower thermal stress during the process. This new solder paste was proved to be suitable for repair of electronic components and manufacturing electronic parts that cannot be soldered in a conventional reflow oven.

**Introduction**

With the miniaturization of modern electronics with selective soldering and the uses of heat-sensitive electronic components, conventional reflow soldering process can no longer satisfy the requirements in advanced packaging. In recent decades, several alternative reflow soldering processes, such as infrared radiation reflow, vapor phase reflow, and laser soldering, were proposed[1]. The inferior uniformity of temperature is mostly concerned as the use of infrared radiation reflow though the running cost is inexpensive. The characteristics of vapor phase reflow soldering is absolutely opposite to infrared radiation reflow. Compared with various soldering processes, laser soldering technology has distinct advantages over both former ones, in which the entire assembly is passed through an oven that can lead to problems concerning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and some to
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the heat-resistance properties of components or the printed circuit boards (PCBs). The key benefits of laser soldering are listed below[2]:

1. Non-contact and controlled heating: In laser soldering, a precisely focused laser beam not only provides a strict control of quantity heating on the desired soldered location leading to a fast and non-destructive of an electrical joint, but also minimizes energy consumption for the demand of low running cost.

2. Precise and controllable process: The process parameter can be accurately controlled based on different components types to provide repeatable results. Furthermore, it enables soldering in narrow confines on high-density board assembly[3].

3. No excessive thermal damage. This local confined energy transfer as heat input will not lead to damage to the surrounding materials, especially to the heat-sensitive components.

4. Reduce mechanical stress. The warpage issue of package during reflow process can be mitigate due to the relatively small rise of package temperature with rapid ramping and cooling.

5. Easy to apply in a variety of demands for soldering, such as components that cannot be reflow in a conventional oven, using different substrates that require a soldering temperature different than the usual ones, repair of electronic components, and joining of fine wire bonds.

Hence, laser soldering have attracted more attention as a new soldering method in the packaging and assembly of microelectronics, optoelectronics, and flat package IC [4, 5], even for flip-chips bumping in 3D package[6].

In 1976, laser was first commercially applied in interconnections of microelectronics by C.F. Bohman[7]. During the last few years, soldering process using laser have been a well-established technology, mostly taking into consideration of various parameters of the soldering process: deposition of solder paste, different alloy compositions, types of laser beam used, and both time and power of laser soldering[8-9], in order to optimize technological procedure of laser soldering. This paper presents a new specific formulated solder paste in a dispensing way for laser soldering with high quality solder joints. The first part of the research revealed some important details how a solder paste has been developed to be applicable in dispensing and laser soldering in terms of flux formulas in the solder paste. The correlations were realized on the study of rheological characterization of solder paste and thermogravimetric analysis by rheometer and thermogravimetric analyzer (TGA), respectively. In the second part of the work, experiments on the ball-grid-array (BGA) solder spheres with solder paste on pads were carried out. The voiding check was observed by X-ray machine. The cross-section inspection of IMC formation was investigated by scanning electron microscopy (SEM) with energy dispersive X-ray (EDX), as well as the quality of joints soldered.

## Experimental Procedure

### *Preparation of Solder Paste and Test Vehicle*

The new dispensing solder paste for laser soldering was developed in mixing solder powder and flux. Alloy of Sn-3.0Ag-0.5Cu (SAC305) was used with the particle size of Type 4, which is followed by the Standard of IPC-TM-650 2.2.14 as Table 1. It is commonly used in assembly of PBGA components nowadays.

Flux mainly comprises rosins, thixotropic agents, activators, solvents and other additives. In the first part of the research, two kinds of fluxes are formulated with different ingredients, in which rosins, thixotropic agents and additives are controlled the same, in order to realize the effects on dispensing characterization and soldering performance using laser. Table 2 present the brief summary of the flux compositions for both samples. These two solder paste samples with different flux formulas in this study are named SP1 and SP2. SP1 is a newly developed for laser soldering technology in a dispensing way, and SP2 is a conventional one.

In the second part of the research, BGA test vehicle was simply carried out using BGA

| Less Than 1% Larger Than | 90% Minimum Between | 10% Maximum Less Than |
|---|---|---|
| 38 µm | 38–20 µm | 20 µm |

Table 1. Type 4 powder size—% of sample by weight.

| | | SP1 | SP2 |
|---|---|---|---|
| Alloy | | SAC305, T4 | |
| Alloy loading (wt%) | | 87.5±1.0% | |
| Flux | Rosins | R | |
| | Thixotropic agents | T | |
| | Activators | $A_1$ | $A_2$ |
| | Solvents | $S_1$+$S_2$ | $S_1$+$S_3$ |
| | Additives | O | |

Table 2. The description of two lead-free solder pastes.

spheres (SAC305, 0.64 mm in diameter), soldered on the pads (0.50 mm in diameter, two kinds of surface finish, OSP and ENIG) of PCBs. Prior to soldering, the pads were covered with a thin layer of additional solder paste of SP1 to ensure good solder joint formation.

### *Laser Soldering Process*

Traditionally arc lamp pumped semiconductor diode laser (Likuan LLU-450101) has been used in laser soldering. Semiconductor diode laser has advantages over $CO_2$ and Nd:YAC lasers to the facts that the wavelength of energy produced is highly absorbed by the metals used in solder but less absorbed by PCB materials [10]. In order to provide uniform heating along the BGA spheres and solder paste, the diameter of the laser beam has to be compatible with the size of the objects to be soldered. Laser beam delivery may be by X-Y-Z stage motion of the laser head. In addition, an arrangement facility of solder paste dispensing can be applied. The process can be monitored using a microscope and a CCD set on the optical axis, thus it is possible for direct observation during laser soldering. The schematic experimental setup of the laser system, and the temperature profile of heating with power control for both parts of the research were illustrated as Figures 1 and 2.

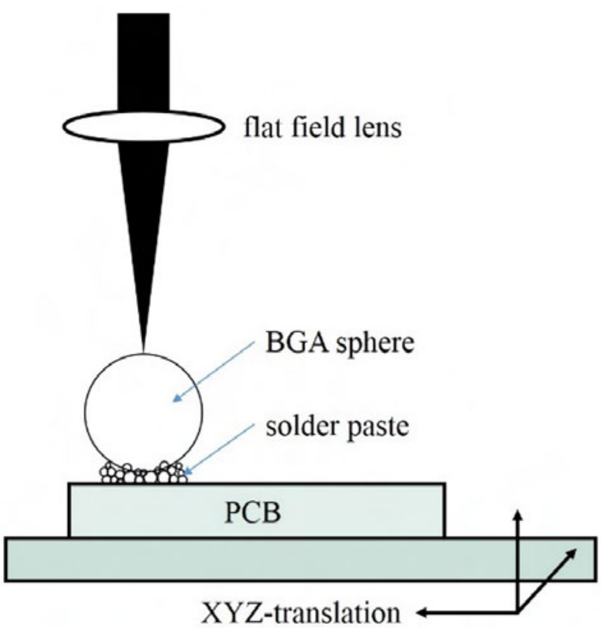


Figure 1: The schematic experimental setup of the laser system.

### *Analysis and Observation*

Evaluation of rheological properties of solder pastes, such as viscosity against shear rate and visco-elastic behavior, on the applicability for dispensing was determined via measurements obtained by a rheometer (Physica MCR101). The correlations between flux formulas in solder paste and soldering performance using laser were also investigated on the study of thermogravimetric analysis of solder paste by TGA (PerkinElmer Diamond TG/DTA). Soldering performance of SP1 and SP2 was observed by digital microscope (Keyence VHX-2000). In the second part of the research, voiding check

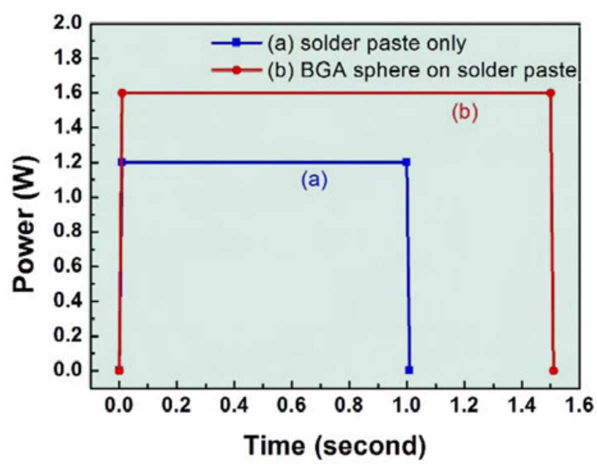


Figure 2: Applicable power profile for (a) solder paste only, and (b) 0.64 mm BGA spheres on pads with a thin layer of solder paste.

was observed by X-ray machine (Dage 7600NT). Micrographs and chemical element analysis of the IMC layer in solder joints were performed on cross-sectioned samples using SEM and EDX, respectively. We dipped the cross-sectioned samples into 5 cc. HNO3 acid solution, in order to highlight the IMC layers. The mechanical properties of the joints were measured by shear test on a bond tester (Condor Sigma Lite) with the shear speed of 100 μm/sec.

## Results and Discussion

### *Rheological properties of solder paste*

The rheological properties of the two solder pastes were determined via measurements obtained during rheological tests[11-12]. For paste dispensing, viscosity of solder paste plays an important role because it should be controlled in the workable range for dispensing. For example, viscosity must be low enough to force the paste flowing through the dispensing needle, but high enough to support the deposit to retain the shape without slumping. The viscosity of solder paste for dispensing is recommended in the range of 100±30 Pa.s, technically. The viscosity of SP1 and SP2 was measured to be 107.5 Pa.s and 95.2 Pa.s by a viscometer, indicating suitable for dispensing. A plot of viscosity against shear rate for the samples was presented in Figure 3. As applied shear rate increased, both SP1 and SP2 showed the same trend of decreased viscosity. That means the solder paste sample shear-thinning behavior as non-Newtonian fluids. The difference of viscosity as a function of shear rate can be resulted from the flux system composition due to different solvents inside.

Furthermore, the oscillatory stress sweep test, which basically applied at a constant frequency of 1 Hz and in the range of 0.5–500Pa, is to characterize the visco-elastic behavior that can help to understand the structures changes occurring under stress during process. The results from the oscillatory test were shown in Figure 4a, 4b. Generally, two modulus were presented in the plot: the storage modulus G' measures the elasticity of solder paste, and loss modulus G" measures the plasticity. Linear visco-elastic region can be identified as the be-

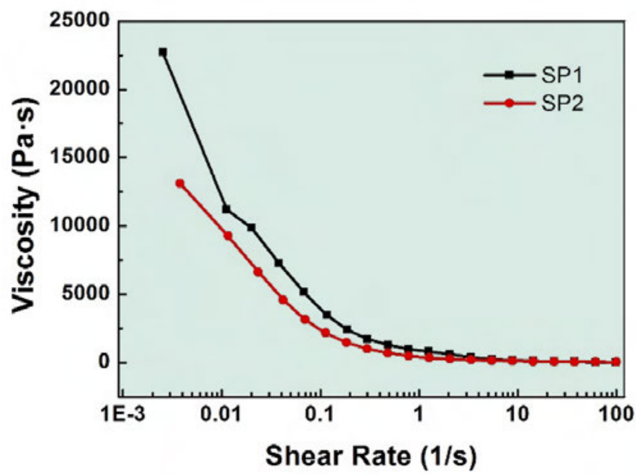


Figure 3: Viscosity against shear rate of solder pastes.

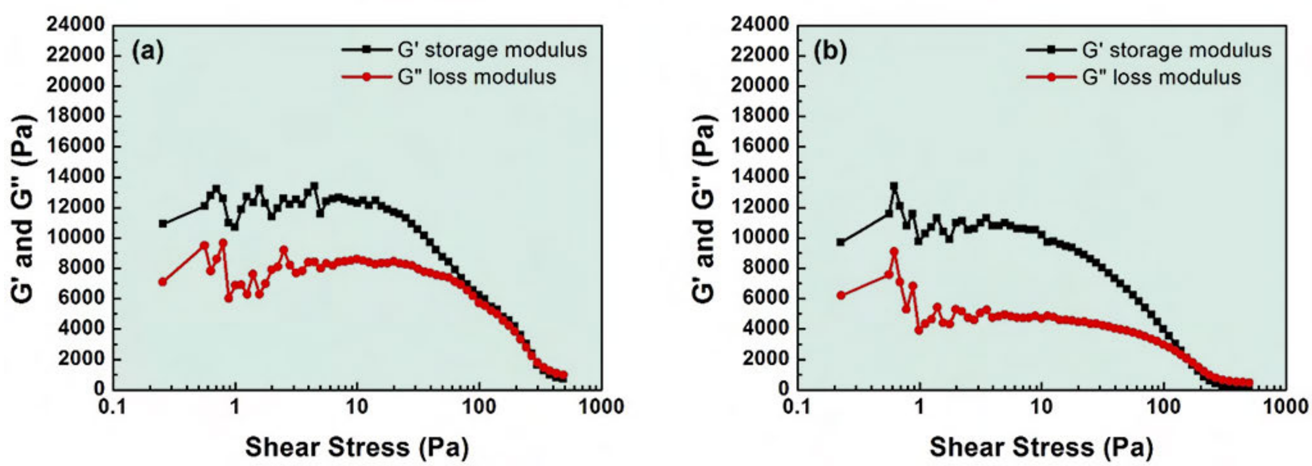


Figure 4: Storage and loss modulus as a function of shear stress for (a) SP1 and (b) SP2.

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ginning of drop in G′ value, and defined as the maximum deformation that can be applied to the solder paste prior to structure breakdown. The broader linear region and higher G′ value of SP1 over SP2 indicate that SP1 has better structure resistance towards applied stress and can withstand higher stress without structure breakdown[11]. In addition, the stress at G′=G″ can be used as an index for the cohesiveness of the solder paste. From the plot, SP1 showed the higher stress value at G′=G″ of 248 Pa than SP2 of 153 Pa. The lower the stress at G′=G″, the more liquid-like the solder paste which could contribute to fracture or leaking deposits during dispensing process. Therefore, based on the fundamental designation of flux formulas in solder paste and its rheological properties, SP1 is proved to be more applicable for dispensing process.

### *Thermogravimetric Analysis of Solder Paste*

As stated, flux formulas in solder paste dictates the thermal behaviors of solder paste during soldering process, and there are numerous attempts to correlate the thermogravimetric analysis of flux in solder paste and soldering performance. Splash of flux or solder balling around solder joints is primarily concerned when using laser soldering due to the rapid heating-up and cooling rate. This phenomenon is considered to be caused by exploding of flux ingredients during soldering process. Accordingly, the splash issue can be reduced through proper selection of flux ingredients. The volatility, hygroscopic property and wetting speed during soldering were considered to have a great influence on splash phenomenon[13].

The results of TGA showed in Figure 5. A heating rate of 10°C/min in air atmosphere was performed in this study. The weight loss of flux at the temperature below 100°C is assumed to be volatilization of moisture, and the presence of moisture is mostly due to hygroscopic properties of chemicals. Two stages of weight loss can be found from the TGA results, in which the first stage of weight loss is mainly caused by volatilization of solvents and a fraction of activator derivatives, and the following stage is related to chemical reactions of activator de-

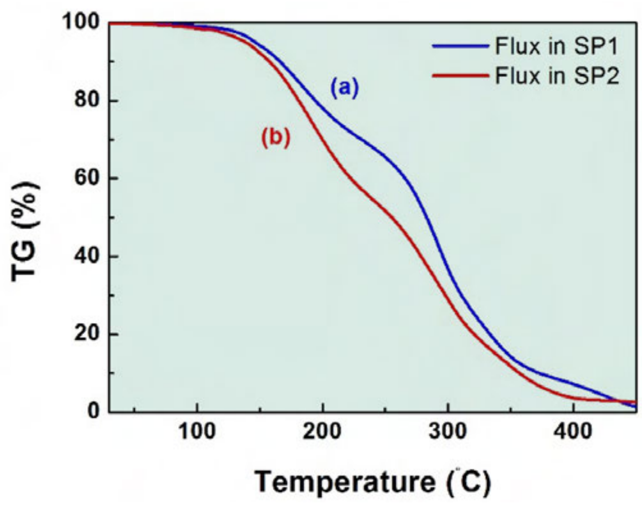


Figure 5: Weight loss curve as a function of temperature of (a) flux in SP1 and (b) flux in SP2.

rivatives. The comparative value of initial temperature and total weight loss of each stage of the samples were showed in Table 3.

For the results of the first stage, it was apparent to figure out that decrease in weight of flux in SP2 is greater than the flux in SP1 due to the different boiling point solvents and the activator derivatives. Typically, more than two solvents of different boiling points are used to formulate a flux in order to offer compatibility to the other ingredients and avoid solvent evaporating simultaneously which can result in splash or solder balling issues. To discuss how volatility of solvent affects the flux splash in this research, three solvents of different boiling points were used to formulate two fluxes, as showed in Table 2, in which flux in SP1 contains solvent S1 and S2 while flux in SP2 contains S1 and S3. Solvent S2 has the highest boiling point followed by S1 and S3, indicating flux in SP1 is more stable at higher temperature with lower risk of flux splash than flux in SP2. On the other hand, the formation of activator derivatives occurred when flux manufactured. Solvent S1 is the common solvent whose functional group can react with activator in the formation of activator derivatives. For the concept of designation, flux in SP1 was assumed to form more activator derivatives due to the easier reactions between solvent S1 and activator A1, resulting in less weight of solvents retained. That is the rea-

| | | Flux in SP1 | Flux in SP2 |
|---|---|---|---|
| First stage | Initial temp. | 134°C | 121°C |
| | Weight loss | 19.2% | 20.1% |
| Second stage | Initial temp. | 200°C | 183°C |
| | Weight loss | 10.5% | 12.8% |

Table 3. Summary of weight loss and temperature for fluxes in SP1 and SP2.

son why the weight loss at first stage of flux in SP1 is smaller than the flux in SP2. Furthermore, the formation of activator derivatives can be an important factor of wetting behavior. It can indicate to have improvements on the splash or solder balling issues during laser soldering, and will be discussed in following sections.

The second stage of weight loss is related to chemical reactions of activator derivatives. As mentioned, the carboxylic acid functional group of activator reacts with coexisting ingredients to form activator derivatives when flux was manufactured. Then during soldering process, the free carboxyl group can be regenerated by thermal dissociation of activator derivatives, meanwhile, volatilization of the regenerated coexisting ingredients occurred. These two causes bring the decreasing in weight at the second stage. The reaction diagram in details was showed in Figure 6. In addition, it has been reported that wetting speed of activator derivatives could have influence on flux splash and concluded that this issue can be minimized by using activator which has a characteristic of slow wetting speed[14]. Therefore, in this research, different activators of $A_1$ and $A_2$ in these two samples are chosen to make a difference in the wetting behavior. The TGA results showed that the temperature of wetting behavior occurred of flux in SP1 is about 200°C and 183°C

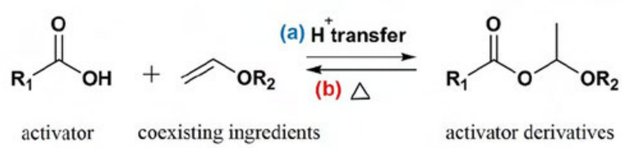


Figure 6: The reactions diagram when (a) flux manufactured; (b) soldering process.

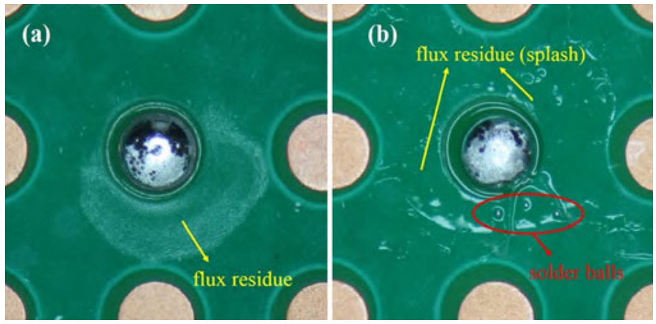


Figure 7: Optical image illustrating solder joint appearance after laser soldering for (a) SP1 and (b) SP2.

for flux in SP2 since activator derivatives begin to react after solvents vaporize, indicating that flux in SP1 has a slower wetting behavior than flux in SP2 during soldering process. In other words, SP1 could be contributed to mitigate the splash issue when soldering using laser.

### *Investigation of Soldering Performance using Laser*

To discuss the relationship of paste characterization and soldering performance using laser for SP1 and SP2, the laser soldering trial on solder paste only was carried out. The best results was obtained in the case of using SP1, as can be seen in Figure 7a. It is obvious that no flux splash and solder balling were found around the solder joints. For the case of using SP2, few solder balls around solder joints can be observed, as shown in Figure 7(b). That issue could be a result of solder splash because of fundamentals of flux formulas, such as the properties of volatility, hygroscopic property and wetting speed. Therefore, as we expected, the splash or solder balling could be eliminated from a point of view of formulated solder paste by the modification of flux compositions.

### *Reliability of Solder Joints*

SP1 was used in the second part of the research, to understand the reliability of solder joint after laser soldering, including voiding check, the microstructure of the interfaces and mechanical properties by a shear test. X-ray inspection for the samples on both OSP and ENIG surface finishes was showed in Figure 8, that the

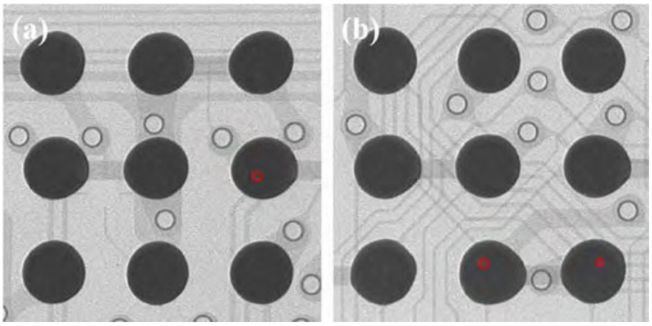


Figure 8: X-ray inspection of (a) OSP and (b) ENIG surface finishes.

solder joints realized using laser contain a very low volume of voids. This type of defect would lead to poor mechanical and electrical properties. The voids are a result of evaporated gas from flux being constrained inside the solder joint due to the surface tension. Because of the fast outgassing using laser, this defect is minimized, so laser soldering produces good results in voiding.

One of the major influences on reliability was the solder joint's microstructure. Therefore, investigation of the interfacial reactions is important and crucial to the understanding of solder joint during laser soldering. Figure 9 showed typical SEM micrographs of the interfaces between the SAC305 solder and two kinds of pads just after soldering using laser processes. From the images, a continuous and uniform IMC layer was found at the interface, and the thickness of IMCs was lower than 1 μm since laser soldering is a very rapid process, that joints were formed within few seconds as energy delivery. The difference in IMC thickness for both OSP and ENIG surface finishes was not so apparent though it has been reported that laser energy is sensitive to the color of surface finish due to the reflection rate of laser beam. The composition analysis results of EDX showed that the reaction products at the interface were close to $Cu_6Sn_5$. The $Cu_6Sn_5$ IMC dispersed inside the bulk solder as the shape of rods and small particles. In the case of ENIG surface finish, Ni and P elements were also detected in the IMC layer, as shown in Figures 9(b) and 10, indicating a Cu-Sn-Ni-P with P-rich layer was formed. Although it cannot be seen on SEM images, this kind of IMC layer has been believed to be more brittle and could degrade the reliability of solder joints.

Figure 11 is a SEM image of interface between solder and OSP pads after the first reflow in a conventional hot air oven. The IMC layer was much thicker than the former one as discussed when soldering using laser, because the longer heating time during reflow process to make IMCs gather and grow into a large flake[15]. For SMT assembly, the thickness of IMC layer is usually required to be in the range of 2–3 μm after the first reflow to be believed to the de-

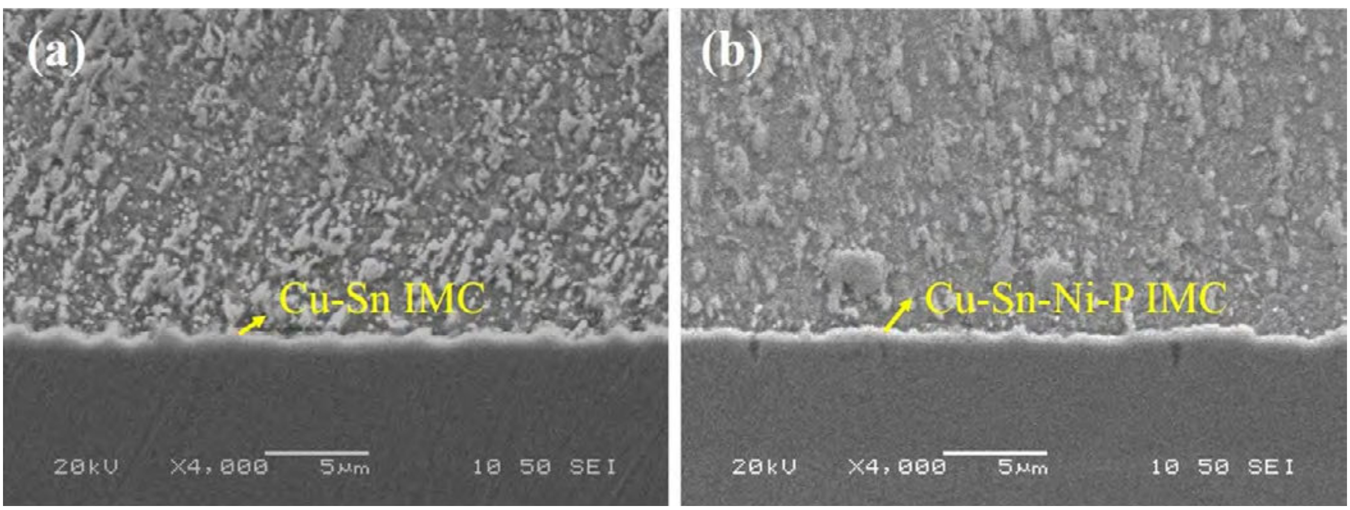


Figure 9: SEM images of the interfaces between the SAC305 solder and (a) OSP and (b) ENIG for laser soldering.

veloping of a strong interconnection. However, the presence of excessive IMC layer will weaken the long-term reliability of solder joints, not only because most IMCs are brittle, but also because the coefficient of thermal expansion (CTE) mismatch exists between the IMCs and solder joints. Furthermore, numerous micro-voids were also seen in the solder matrix and the interface between the IMC layer and solder. These micro-voids comes from the unbalanced in diffusion rate of Sn, Cu, Ag and Ni during reflow process, and can provide initiation sites and propagation paths for cracks whose formation degrades the reliability of solder joints. The study of the effects of isothermal aging on long-term reliability will be necessary in the future.

Mechanical properties of BGA spheres soldered by laser soldering and hot air reflow process with same solder paste SP1 were shown in Figure 11. It was believed that the shear strength above 10N is strong enough for the connecting of microelectronic components. The results of shear strength revealed two important aspects: first, in the case of using laser soldering, the shear strength of BGA sphere soldered on ENIG pads was inferior to soldered on the OSP pads, and also had a larger deviation of shear strength. As discussed before, a thin additional P-rich layer at the interface between solder and IMC layer could be the main reason. Secondly, it was found that the shear strength of solder joints by the laser soldering was slightly lower

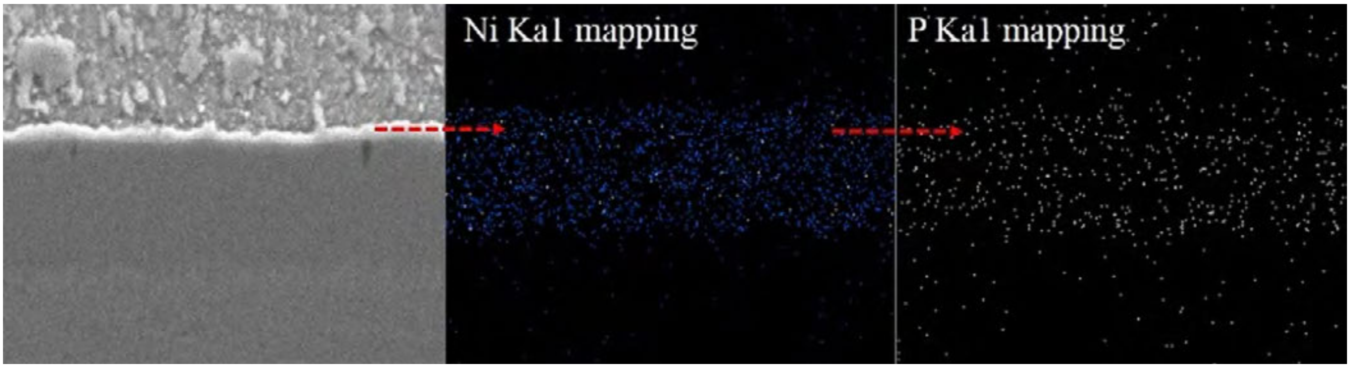


Figure 10: Composition analysis of IMC by EDX mapping for ENIG pads.

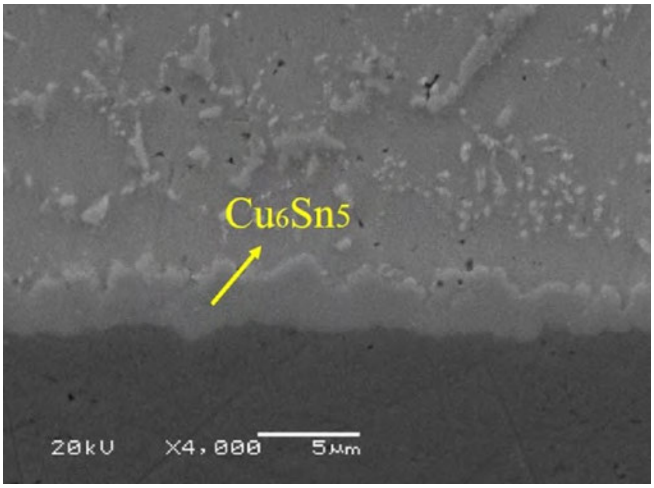


Figure 11: SEM images of the interfaces between the SAC305 solder and OSP after the first reflow process.

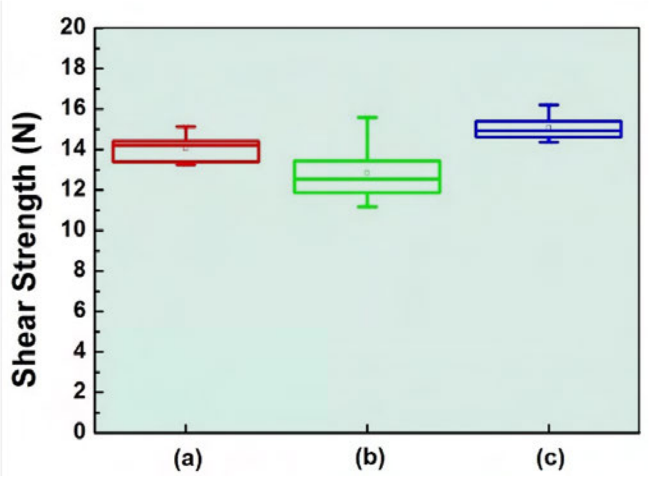


Figure 12: The results of shear strength for (a) OSP with laser soldering, (b) ENIG with laser soldering, and (c) OSP with reflow process.

than that of joints soldered by the first reflow process. The reason for the slight difference in shear strength can be assumed to be the grain structure of IMCs. Typically, the total time of reflow process is around 8–10 mins for a commercial reflow oven with 12 zones, including initial ramp, soaking, spike in general. The heating time is longer enough to form a uniform flat IMC layer with larger grain size. On the other hands, the lower thermal stress was induced during laser soldering to enhance the strength of solder connection. Besides, the thickness of IMC layer is much lower in case of using laser soldering (<1 µm), because the very short soldering time. We also can deduce the energy delivery was sufficient for the formation of strong solder connection with finer grain structure due to a rapid cooling rate and leading to solidification fast. As stated above, this is also a positive result, as it leads to better electric and thermal characteristic.

## Conclusions

Laser soldering provides a clean non-contact process which involves transferring energy to the soldering location using a precisely controlled beam. Hence, laser soldering can not only used in assembly of electronic components as a candidate to other soldering technologies, but also illustrated a good prospect for particular applications.

In this research, we bring theory to practice that a novel solder paste of alloy composition of SAC305 in a dispensing way is developed for laser soldering technology. The following conclusions can be formulated:

1. According to the rheological properties of solder paste based on the flux formulas, SP1 is proved to be more applicable for dispensing process.

2. The relationship between fundamental design of flux and soldering performance was investigated by thermogravimetric analysis. It is clear that SP1 could be contributed to mitigate the issues of splash and solder balling when soldering using laser.

3. Reliability test of soldered joint with SP1 showed good results in voiding and mechanical properties. Since laser soldering is a very rapid process, each joint can be completed in the range of a second and the wasted energy is minimal. An additional advantage is that the joint cools very quickly that brings tougher joints with better mechanical properties owing to the finer grain structure and short inter-metallic zone. This leads to excellent electrical and thermal solder joint characteristics.

## Acknowledgement

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## References

[1] N. Suenaga, M. Nakazono, and H. Tsuchiya, “Laser soldering,” Welding International, vol. 2, no. 3, pp. 269–276, Jan. 1988.

[2] Y. H. Tian and C. Q. Wang, “12 Laser soldering A2 – Zhou, Y.,” in Microjoining and Nanojoining, Woodhead Publishing, 2008, pp. 299–326.

[3] P. M. Beckett, A. R. Fleming, R. J. Foster, J. M. Gilbert, and D. G. Whitehead, “The use of lasers for the soldering of high density interconnects,” in 1994/220), IEE Colloquium on Interconnection Technology (Digest No, 1994, pp. 4/1–4/4.

[4] A. Flanagan, A. Conneely, T. J. Glynn, and G. Lowe, “Laser soldering and inspection of fine pitch electronic components,” Journal of Materials Processing Technology, vol. 56, no. 1–4, pp. 531–541, Jan. 1996.

[5] Z. Han, S. Xue, J. Wang, X. Zhang, L. Zhang, S. Yu, and H. Wang, “Mechanical properties of QFP micro-joints soldered with lead-free solders using diode laser soldering technology,” Transactions of Nonferrous Metals Society of China, vol. 18, no. 4, pp. 814–818, Aug. 2008.

[6] T. Oppert, G. Azdasht, E. Zakel, and T. Teutsch, “Laser assisted soldering and Flip-Chip attach for 3-D packaging,” in 31st International Conference on Electronics Manufacturing and Technology, 2006, pp. 86–86.

[7] C.F. Bohman, “The Laser and Microsoldering”, Society of Manufacturing Engineering, Tech. paper N0 AD74-810 Mich 48128, 1974, pp.19–20.

[8] R. Batorfi, Z. Illyefalvi-Vitez, O. Krammer, R. Bunea, and P. Svasta, “Optimizing technological process for laser soldering of fine-pitch

flip chips," in 32nd International Spring Seminar on Electronics Technology, 2009. ISSE 2009, 2009, pp. 1–6.

[9] R. Bunea, P. Svasta, Z. Illyefalvi-Vitez, R. Batorfi, and A. Geczy, "Optimizing laser soldering of SMD components: From theory to practice," in Design and Technology in Electronic Packaging (SIITME), 2011 IEEE 17th International Symposium for, 2011, pp. 55–58.

[10] S. M. Naveed and R. L. Woods, "Diode laser soldering: a lumped parameter mathematical model and comparison of different optical soldering technologies," 2003, vol. 4973, pp. 142–157.

[11] R. Durairaj, S. Ramesh, S. Mallik, A. Seman, and N. Ekere, "Rheological characterisation and printing performance of Sn/Ag/Cu solder pastes," Materials & Design, vol. 30, no. 9, pp. 3812–3818, Oct. 2009.

[12] S. S. Zhang, Y. J. Zhang, and H. W. Wang, "Effect of particle size distributions on the rheology of Sn/Ag/Cu lead-free solder pastes," Materials & Design, vol. 31, no. 1, pp. 594–598, Jan. 2010.

[13] N.-C. Lee, "6 – SMT Problems During Reflow," in Reflow Soldering Processes, Burlington: Newnes, 2001, pp. 107–142.

[14] D. Manjunath, S. Iyer, S. Eckel, P. Damodaran, and K. Srihari, "Minimizing flux spatter during lead-free reflow assembly," Soldering & Surface Mount Tech, vol. 18, no. 3, pp. 19–23, Jul. 2006.

[15] J. Liu, H. Ma, S. Li, J. Sun, A. Kunwar, W. Miao, J. Hao, and Y. Bao, "The study of interficial reaction during rapidly solidified lead-free solder Sn3.5Ag0.7Cu/Cu laser soldering," in 2014 15th International Conference on Electronic Packaging Technology (ICEPT), 2014, pp. 949–952.

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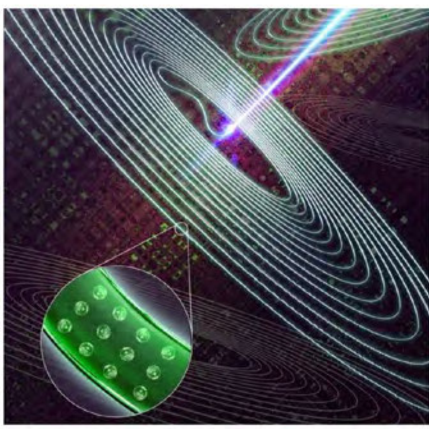
**Hsiang-Chuan Chen** is section manager and **Ya-Ching Chuang** is the senior researcher for the Advanced Material Development Center at Shenmao Technology Inc.

# Glass Now Has Smart Potential

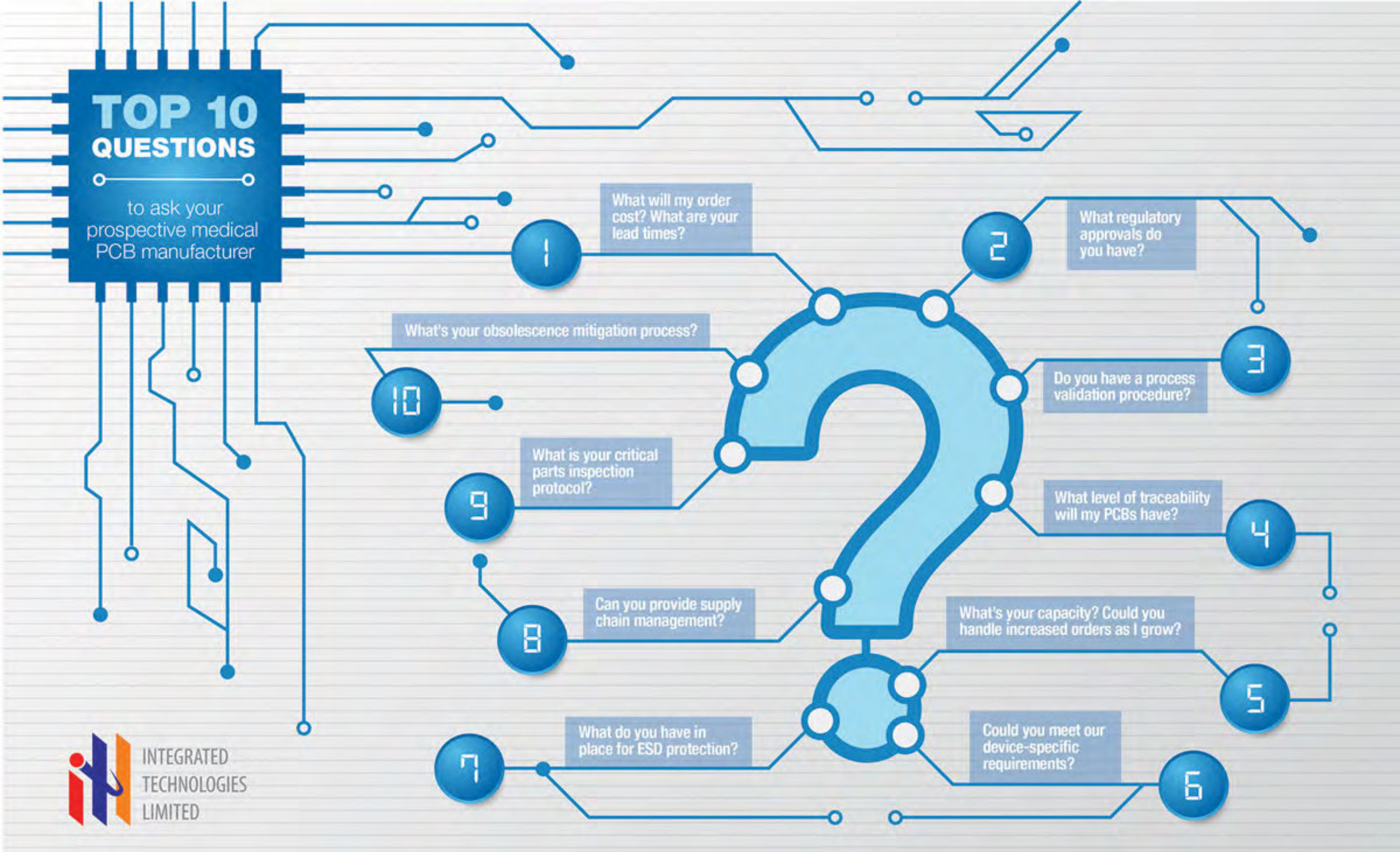
Researchers at the University of Adelaide have developed a method for embedding light-emitting nanoparticles into glass without losing any of their unique properties—a major step towards "smart glass' applications such as 3D display screens or remote radiation sensors.



This new "hybrid glass" successfully combines the properties of these special luminescent nanoparticles with the well-known aspects of glass, such as transparency and the ability to be processed into various shapes including very fine optical fibers.

"These novel luminescent nanoparticles, called upconversion nanoparticles, have become promising candidates for a whole variety of ultra-high tech applications such as biological sensing, biomedical imaging and 3D volumetric displays," says lead author Dr. Tim Zhao, from the University of Adelaide's School of Physical Sciences and Institute for Photonics and Advanced Sensing (IPAS).

Although this method was developed with upconversion nanoparticles, the researchers believe their new "direct-doping" approach can be generalized to other nanoparticles with interesting photonic, electronic and magnetic properties.




# How to Overcome Medical Electronics Manufacturing Challenges

**by Carl Lincoln**
INTEGRATED TECHNOLOGIES LTD

It's an exciting time to be part of the global medical device industry; a large percentage of companies have found opportunities for growth, investment in medical device research has increased and there has been a surge in collaborations, which have led to significant technological advancements.

In recent years, the regulatory landscape for medical devices has become more and more risk-focused with the aim of ensuring patient safety by taking a process rather than product-based approach. When you look closely at manufacturing processes for critical parts, such as PCBs, the specific challenges encountered mean that companies often bring in a trusted medical electronics manufacturing partner to negate risk.

Electronics are at the heart of a medical device and are responsible (alongside the software and firmware) for correct, safe and continued operation. If a medical device fails in the field, patients can't be treated or diagnosed and that is a serious problem. This leads to a high level of business risk for the legal manufacturer (the business that is outsourcing) as they will incur the costs of replacing or repairing the device and may have fines or compensation clauses in their supply contracts.

A challenge for medical EMS providers is the need for continual supply. Once a medical device has become part of clinical practice there is an expectation from users that it will always be available where needed. Electronics have a relatively short lifespan and so an EMS provider can provide added value by helping their customers to manage these risks by implementing obsolescence mitigation strategies.

Medical electronics manufacturers must also be able to manage change control and it is vital that changes made to the design of a

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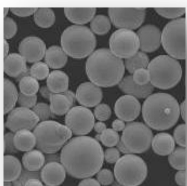

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medical device are properly documented. This is ultimately the responsibility of the legal manufacturer but an EMS company will have to ensure that the introduction of any change is properly controlled and documented on their side too.

Supplier management is also an important consideration. A medical PCB manufacturer is required to maintain a compliant supply base for components, bare boards and so on. This is likely to involve regular auditing and continued maintenance of an approved vendor list.

When planning for the manufacture of medical electronics, cost and budget is a significant challenge. Investing in facilities, machinery, extra staff and everything else needed is a substantial expense. With big outlays comes big risk—in a nutshell outsourcing minimizes that risk and frees up a lot of capital.

There are a lot of things to consider when choosing who to work with and it is worth taking time to make sure the partner fits your needs. In the past, many organizations would be tempted by the lowest quote or fastest turnaround, but it is worth thinking more strategically than that. It is important to look beyond the present and ask questions like: If your production increases, could your preferred supplier meet these new demands? What are the benefits of working with a supplier with a quality management system (QMS) in place? Safeguarding for the future is paramount.

To help you make comparisons between suppliers, ITL has listed a set of questions to ask your prospective medical PCB manufacturer. These will help ensure that the manufacturer you work with has the right experience and expertise for you.

### Top 10 Questions to Ask Your Prospective Medical PCB Manufacturer

When you're looking to change supplier or are outsourcing for the first time, you want to know that the company you are partnering with has the right experience and expertise. So what should your key criteria be for employing your medical PCB manufacturer? Here's ten top things to ask that will help you to easily make comparisons:

**ONE: What will my order cost and what are your lead times?**

Cost and lead times are going to be the primary factors in your decision—in our industry everyone's looking to get best value for money and has deadlines to keep. But don't look at these in isolation—it's important not to sacrifice quality for speed. Make sure you strike the right balance between quality, value and lead times.

**TWO: What regulatory approvals do you have?**

A manufacturer doesn't have to have medical specific regulatory approvals such as ISO 13485 if they're only producing the PCB that is integrated elsewhere. However, if they do have a quality management system (QMS) in place, you can be sure that the entire process of purchasing, producing, handling and testing PCBs is highly controlled. So, looking for a PCB manufacturer with these approvals will give you extra security and protection.

**THREE: Do you have a process validation procedure?**

Some subcontract PCB manufacturers will produce straight from your bill of materials, while others validate their processes before they start. Process validation is a way of ensuring high yields before manufacturing starts as opposed to having to rework boards that fail.

What you need depends on factors such as which markets you are selling into (e.g., if you sell your device in the USA, your process will need to be validated to FDA standards). As a critical part of the device, the FDA may want to audit your PCB supplier.

**FOUR: What level of traceability will my PCBs have?**

Traceability can range from critical parts to full component level. The level of traceability needed depends on the class of your medical device. For a low-risk Class I device you may only need the critical parts to be traceable and if these aren't on the PCB your manufacturer may not need any traceability at all. That said, it is worth considering the balance between what is required by regulation and what makes sense to

protect your business and your customers in the future.

**FIVE: What's your capacity? Could you handle increased orders as I grow?**

Your manufacturer may be able to produce the volume of PCBs that you need now, but will they still be suitable in future?

You need to consider whether you want to go through the process of knowledge transfer, re-training and re-validating when your volumes increase or whether you would rather select a manufacturer that can grow with you.

You should also ask your manufacturer how flexible they are. Do they insist on minimum order quantities? What fixed forecasts will they hold you to? Could they still meet lead times if you double your order quantity?

**SIX: Could you meet our device-specific requirements?**

If your device has any specific requirements such as flexible PCBs, multi-layer boards or uncommon storage conditions, don't assume that every PCB manufacturer has these capabilities. If you find a perfect fit but they don't have everything, ask if they would be willing to invest—this is also a good test of their commitment to you as a customer.

**SEVEN: What do you have in place for ESD protection?**

Electrostatic discharge, the sudden transfer of electricity from one object to another, can damage components. The smallest amount that can be felt by a human (when you touch something and feel an electric shock) is around 2000 volts, but sensitive electronic components can be damaged by as little as 20 volts of static electricity.

There are a multitude of measures that a PCB manufacturer can put in place to mitigate the risks of ESD damaging your boards and they should be able to demonstrate them to you.

**EIGHT: Can you provide supply chain management?**

Can your manufacturer take on value-added activities such as supply chain management? There are more burdens in this area than you might think, examples include auditing suppliers, negotiating prices and RoHS compliance.

If your business isn't geared up for sourcing and handling components you may be better off outsourcing this to your manufacturer too. Plus, they will already have good relationships with component suppliers and might be able to get preferential terms.

**NINE: What is your critical parts inspection protocol?**

According to the requirements of ISO 13485, if your critical parts list includes components on your PCB, these need to be inspected at goods-in and recorded by the manufacturer. A specialist medical device PCB manufacturer will have this built in to their process, whereas a general EMS company may not.

**TEN: What's your obsolescence mitigation process?**

Component obsolescence is something that cannot be avoided but can be managed. Can your PCB manufacturer help you with strategies such as re-designs, bulk buys and last-time buys to avoid any breaks in supply? If not, you're likely to lose money and be left with few options.

Now you know what to ask, you can start looking for your ideal PCB manufacturer. Forging an effective relationship with your supplier can help drive your business forward and contribute to success—so it's important to get it right. You want to know that your supplier has the expertise, experience, facilities and capability to meet, and even surpass, your expectations. **SMT**

**Carl Lincoln** is a marketing and business development coordinator at Integrated Technologies Ltd.

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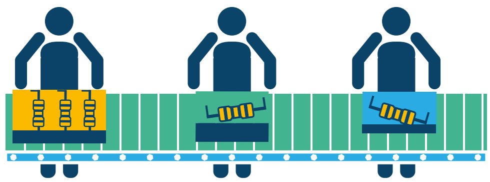

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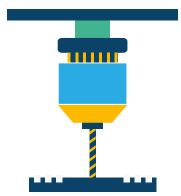

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# Recent Highlights from SMT007

## 1 SMTA West Penn Chapter Plans Manufacturing Boot Camp in August

DRS Technologies' Bill Capen, who is also the president of the SMTA West Penn Chapter, talks with I-Connect007's Patty Goldman about their expanded Chapter Expo & Tech Forum, and their plans of doing a boot camp in August.

## 2 IPC President John Mitchell Discusses IPC's Footprint in China

At the Capital Club in Beijing, IPC's president John Mitchell met with I-Connect007's Edy Yu to discuss the current activites of IPC China. Some of the topics covered included the growing China membership, training, trade shows and IPC China's standards development effort.

## 3 Soldering Experts on Hand at SMTA's West Penn Chapter Expo & Tech Forum

At the recent SMTA West Penn Chapter Expo & Tech Forum, Marilyn Lawrence, founder and president of Conformance Technologies Inc., speaks with I-Connect007's Patty Goldman about the importance of solder training, and how far it has come through the years.

## 4 SMTAI Conference Program Finalized; Registration Now Open


The program for the SMTA International conference, which is scheduled to take place September 25–29, 2016 at the Donald Stephens Convention Center in Rosemont, Illinois, is now finalized and available online, and registration is now open.

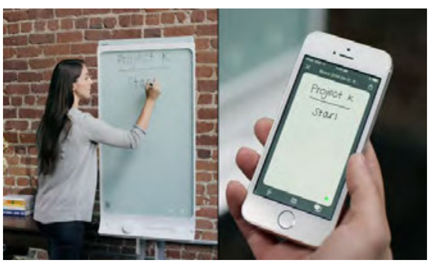
## 5 IPC Standards Committee Reports, Part 2 – Assembly and Joining, Component Traceability, Flexible Circuits, High Speed/High Frequency

These standards committee reports from IPC APEX EXPO 2016 have been compiled to help keep you up to date on IPC standards committee activities. This is the second in a series of reports.

## 6 Salcomp Expands Manufacturing Capacity in India

Salcomp has decided to set up its second Indian factory in the Noida City, in Delhi, India.

## 7 Foxconn to Acquire SMART Technologies



SMART Technologies and Foxconn Technology Group have entered into an arrangement agreement under which Foxconn has agreed to acquire all of the outstanding common shares of SMART for a cash payment of $4.50 per common share.

## 8 Ryder Wins Blackstar Manufacturer of Excellence 2016 Award

Ryder Industries Ltd has received the "Manufacturer of Excellence" award from Blackstar for the second consecutive year.

## 9 IPC Unveils Results of IPC Rework Experience Competition at SMT Hybrid Packaging 2016

The first ever Rework Experience Competition was held at this year's SMT Hybrid Packaging international exhibition and conference.

## 10 HANZA and Free2move Forms Partnership on IoT Device Manufacture

EMS firm HANZA has signed a cooperation agreement with Free2move regarding industrialization and manufacturing of the company's current and future products.

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# Events

For IPC's Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing, check out SMT Magazine's full events calendar here.

**Capital Expo & Tech Forum**
August 30, 2016
Laurel, Maryland, USA

**Medical Electronics Symposium 2016**
September 14–15, 2016
Portland, Oregon, USA

**IPC India 2016**
September 21–23, 2016
Bengaluru, India

**SMTA International 2016**
September 27–29, 2016
Rosemont, Illinois, USA

**electronicAsia**
October 13–16, 2016
Hong Kong

**IPC-SMTA Cleaning and Conformal Coating Conference**
October 25–27, 2016
Chicago, Illinois, USA

**IMPACT Europe 2016**
November 1, 2016
Brussels, Belgium

**PCB Carolina: Regional Trade Show**
November 2, 2016
Raleigh, North Carolina, USA

**electronica 2016**
November 8–11, 2016
Munich, Germany

**International Printed Circuit & Apex South China Fair (HKPCA)**
December 7–9, 2016
Shenzhen, China

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