PCB007 PRESENTS

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the pcb magazine

AN I-CONNECT007 PUBLICATION

FLEX & RIGID FLEX

Registering High-End Rigid-Flex Multilayers for Lamination

by Victor Lazaro Gallego & Roberto Tulman—page 12

Image courtesy of Chemplate Materials S.L.

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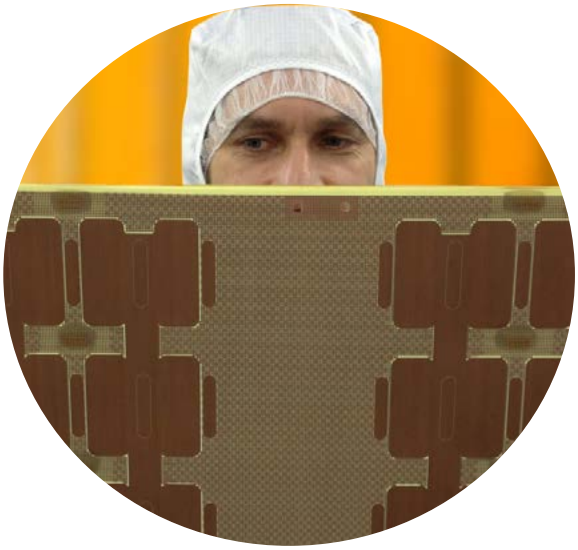
Flex & Rigid-Flex

This month, *The PCB Magazine* presents the many sides of flex and rigid-flex circuits, which have myriad applications in just about every sector of the electronics industry. Their ability to be formed into complex three-dimensional geometries, or to withstand multiple cycles during their functional life, adds a third dimension to the concept of the interconnecting substrate.



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THE WAY I SEE IT

China Stumbles

by Ray Rasmussen
I-CONNECT007

The need to see China fail verges on jingoism. Americans distrust the Chinese model, find that its business practices verge on the immoral and illegal, that its reporting and accounting standards are subpar at best and that its system is one of crony capitalism run by crony communists. On Wall Street, the presumption usually seems to be that any Chinese company is a ponzi scheme masquerading as a viable business. In various conversations and debates, I have rarely heard China's economic model mentioned without disdain. Take, as just one example, Gordon Chang in Forbes: "Beijing's technocrats can postpone a reckoning, but they have not repealed the laws of economics. There will be a crash."

The above statement is from a blog by Zachary Karabell, president of River Twice Research and River Twice Capital, a regular commentator on CNBC, and a contributing editor for Newsweek/Daily Beast.

As mentioned in the blog, it's hard to know what's really going on in China. Nobody believes the government's official data, but even the official reports out of China confirm a significant slowdown in economic growth. The official line is now growth of 7.5%, which is a significant change from the 10% average rate of growth the country has experienced over the last two decades. With growth and exports way down, a housing bubble looming, international

pressure on currency exchange rates, rising wages and costs, along with environmental pressures, the country is in a deep mess. Of course the official spin makes it sound like things are under control. But that may not be the worst of it. A July 29 article on CNBC.com muses that there is actually no growth, or negative growth, and that the 7.5% Chinese government official number is nonsense.

Robert Barbera, co-director of Johns Hopkins Center for Financial Economics, had the following to say about China's economy, as he makes his case that things are much worse than they appear:

"If you take the top 10 trading partners with China and you add up their exports to China, you've got data that the Chinese government doesn't get to put their hands on," he said. "If you look at that data, what you've actually got is about minus 4%, year-over-year."

It would seem that China's in a tough spot.

Quite honestly, a big part of me is happy to see economic difficulties in the PRC. It's payback. And, now that I looked up the word, it's jingoistic as well. China's been riding high for way too long, building their economy on the backs of many small businesses here in the states, Europe, Japan and elsewhere. Tens of thousands of businesses have had to close their doors after Chinese competitors crushed them with artificially low-priced products. The Chinese government's artificial economic environment was so enticing that investment flooded into the country as companies were compelled to move their factories to far-off China just to survive. I think I know why the Chinese did it, but it wasn't fair. Thousands of small business people lost everything. Of course, our government officials allowed all this to happen so they're at fault, too. Enough said. Back to the meltdown.

"China's been riding high for way too long, building their economy on the backs of many small businesses here in the states, Europe, Japan and elsewhere. Tens of thousands of businesses have had to close their doors after Chinese competitors crushed them with artificially low-priced products."

Too Big to Fail

I've always liked this aphorism: If you owe the bank $20,000 (or any relatively small amount), you have a problem. If you owe the bank $20 million, they have a problem. The sad part is that in this case, regarding China's difficulties, we, the West, have a problem.

China's rapid ascension to become the second largest economy has put us all in jeopardy. The Chinese economy is integrated economically into just about every other country on the planet. It's an integral partner in the global economic system, which makes them a "too big to fail" partner. We (the West) have created a monster. We allowed China to play in our sandbox while making up its own rules along the way; shame on us for not demanding better controls and transparency. Having said that, we have trouble running our own economies, demanding our own transparency and enforcing our own rules so we really can't have much to say about China and the way the Chinese run things. At this point, our job is to help them even more to ensure they don't collapse and drag the rest of us down with them. Keep this in mind: The West sells a lot of equipment and systems into the PRC. A collapse or significant slowdown in the Chinese economy will have a dramatic effect on our industries. The good news is that we sell to the entire world, so problems in China won't kill our industries, but a China meltdown (which many claim is already underway) will ripple around the planet, weakening the fragile, global recovery.

I feel for China. Not the government, but the people. We all may want the Chinese government to take a few lumps for their dastardly deeds over the last decade or two, but they do have some ground to make up after their more than 50 years of communism. When we have problems in the West, people struggle financially, and we might see a few demonstrations and such, but with China, if they let things get out of hand, hundreds of millions of lives will be at stake. Their issues are potentially catastrophic. A structural collapse in China will cost millions of lives and set things back in that part of the world 10–20 years, which will affect all of us.

Here's another statement from Zachary Karabell's blog:

"The consequences of a Chinese collapse, however, would be severe for the United States and for the world. There could be no major Chinese contraction without a concomitant contraction in the United States."

You should read the blog entry The U.S. can't afford a Chinese economic collapse. Basically, he says that we may not like the idea of helping China out of this mess, but we have to. It's now in our best interest.

It's been my experience over the years that everything eventually comes back into balance. China will find its rightful place in the world economy; it will come into balance. It would seem as if that process is fully underway.

If you want to read more about the difficulties facing China, I've added a few links to some interesting articles. Enjoy! **PCB**

China's Economy stumbles in May, growth seen sliding in Q2

More Signs China's Economy Is in Trouble

Will China's economy crash?

China's environment: an economic death sentence

Will China's Slowdown Hurt the U.S. Economy?

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Registering High-End Rigid-Flex Multilayers for Lamination

by Victor Lazaro Gallego
CHEMPLATE MATERIALS S.L,
and Roberto Tulman
ELTEK LTD.

SUMMARY: The challenge of registering and improving productivity on complex rigid-flexes with mixed materials on high-density interconnect PCBs is becoming more complex and problematic. Today, boards include different materials, several sequential laminations, denser circuitry and smaller via pads. In this article, a team from Chemplate Materials and Eltek shows the techniques developed and the test results that prove the better registration achieved by this new system.

Introduction

Flex-rigid multilayer boards allow OEMs a significant degree of freedom and flexibility in design, permitting the form, fit and function of a product to be optimized. Flex-rigid boards gained popularity among medical, aerospace, military and industrial OEMs due to these reasons, and because of the inherent reduction in weight, volume, connectors, and assembly work. An additional advantage of such boards is the fact that they are much more reliable than the traditional option of joining several rigid boards using cables and connectors.

Flex-rigid boards are built using different materials in the same stack-up. Rigid layers are usually built around a flex leaf or several flex layers. Sometimes flexes are placed as outer layers, but generally they are interleaved between the rigid inner layers.

Building these boards is not simple and requires expertise and experience. It begins with the design, stack-up planning and selection of the appropriate materials, and continues with optimization of process parameters to allow sequential laminations, scale factor and registration considerations, improvement of adhesion between dissimilar materials, and so on.

Numerous parameters must be considered, including form factors, bending radiuses, process temperatures, registration, symmetry factors, and more. The flex-rigid build-ups usually

Figure 1: Build-up of a standard flex-rigid.

require different types of prepregs and bonding materials, acrylic adhesives and no-flow epoxy prepregs of different types and thicknesses.

The standard flex-rigid boards (Figure 1) are manufactured with a coverlay over the flex leaf, covering the entire surface of the inner layer; this coverlay usually contains an acrylic adhesive. During the final press lamination of the boards, pre-routed no-flow prepregs are used, covering only the future rigid sections of the board.

As seen in Figure 2, when building a "bikini" type construction, the prepregs are pre-routed to cover only the rigid parts of the boards, leaving a window in the flex areas. These flex areas are initially pressed with an acrylic adhesive coverlay.

This being the case, we see that we need to pre-press the flex inner layer with a coverlay only in the flex areas and press the boards again with the pre-routed prepregs.

The third case being analyzed here is shown in Figure 3. When a number of flex layers are pre-bonded, this is usually done with an acrylic type of adhesive and then the final board is manufactured with no-flow epoxy prepregs.

As we can see in all of the aforementioned fabrication methods, no matter how we design the boards and the type of materials we choose, they will be required to undergo a series of press

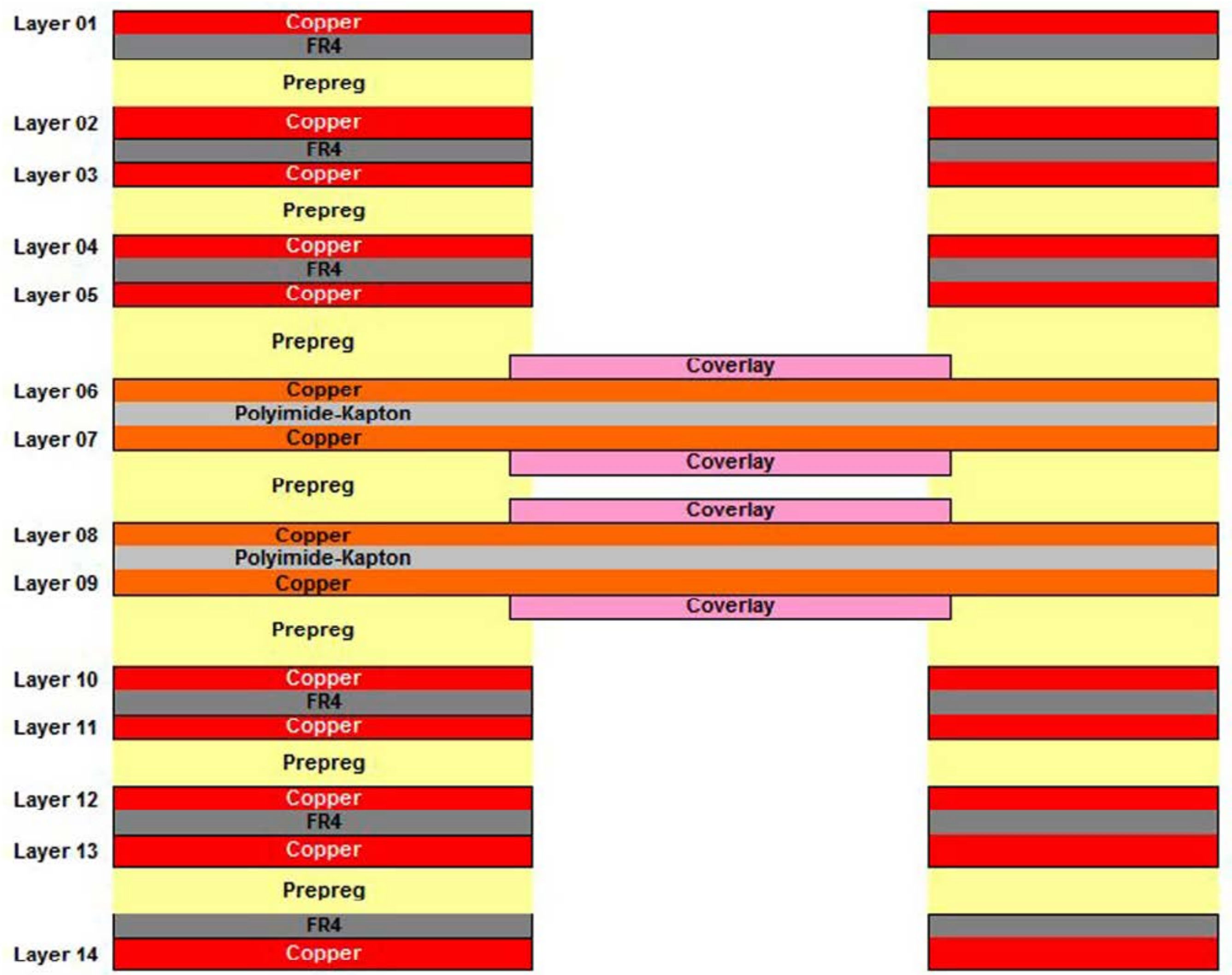

Figure 2: Build-up of a "bikini" flex-rigid.

cycles. These PCBs include different materials with different characteristics, with part of them covering only selective areas throughout the panel.

As can be seen in Figure 4, not only do the dielectric properties differ from one material to another, but also their degree of water absorption, mechanical characteristics and coefficients of thermal expansion. The figures in the table were copied from data sheets of high-end materials used and are not intended to serve for production purposes. These serve only as an example of the complexity of mixing materials in the manufacture of high-end boards.

Registration of the materials is often done manually, by applying the coverlay pieces or pre-routed prepreg onto the flex layer and bonding them at the corners to affix the parts in place until the layers are transferred to the press cycle. Such flex layers initially undergo a preliminary press cycle followed by a final press with the rigid inner layers—again using no-flow prepreg and sometimes also high-flow prepreg, depending on the build-up of the board. Today, boards often require additional subsequent laminations.

As a result of this process, the layers' dimensions change from cycle to cycle, especially the flex layers that are not constrained by a glass cloth. The actual final size of the flex will be

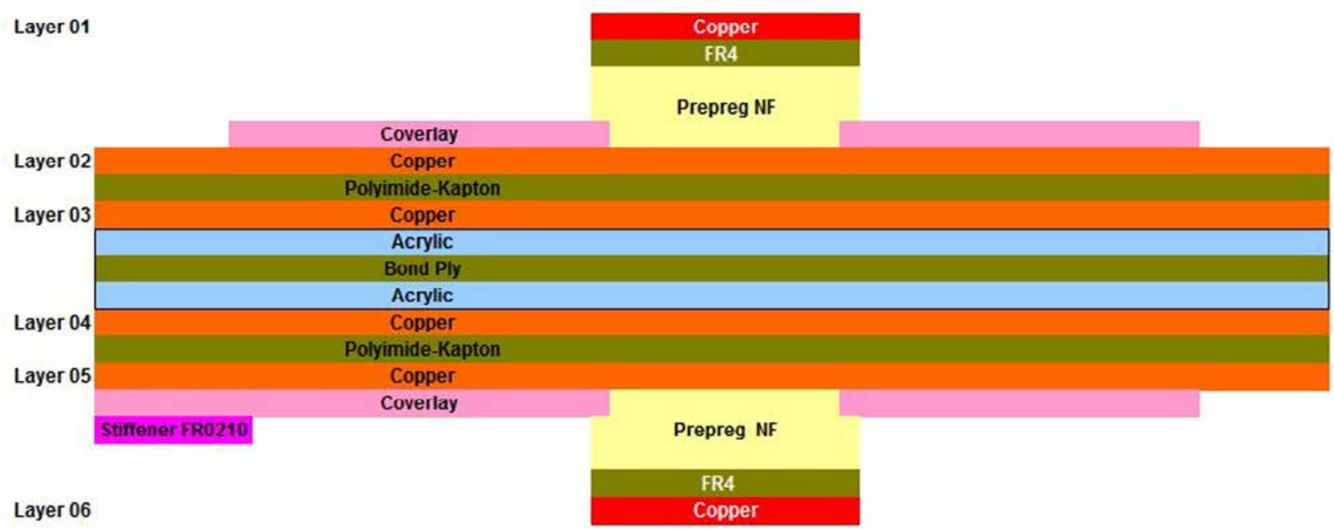

Figure 3: Build-up of a multi-flex flex-rigid.

Property	Epoxy layer	Epoxy no-flow	Acrylic adhesive
Dk (dielectric)	4.6	4.4	3.5
Young's Modulus KN/m2	20-25	18	low
reinforcement	Glass	Glass	None
Water absorption %	0.3	0.1	0.8
Tg (C)	170	170	~100
x-y thermal expansion ppm	15	15	Large
Z CTE (below Tg)	50	87	Large

Figure 4: Typical values of high-end materials for flex-rigid boards.

affected by many variable factors, among them: panel size, amount of copper and copper thickness, layer thicknesses, prepreg types, and pressure and temperatures parameters of press cycles.

Part of the dimensional changes can be foreseen and pre-adjusted by scaling the artwork to be used, but this is not always possible and, as a result, the finished board may exhibit misregistration between layers, deviations from the required dimensions, flow of prepreg into the flex windows and problems during final assembly.

Registration of layers during press cycles are done in one of two ways:

• **Pin lamination:** The flex and rigid inner layers are pre-punched or pre-drilled for pin insertion. This system usually uses a large number of pins. The layers are laid up onto a steel plate with pins, also the pre-routed prepreg sheets are drilled with holes to serve the same registration system. An upper steel plate closes the stackup, which is inserted into the press. After lamination cycle ends the subsequent disassembly includes de-pinning the boards for further production.

• **Pin-less lamination:** With this method, the layers are assembled in a jig with pins and are then introduced in a machine where the build-up is nailed with metal rivets or bonded using heat at different points around the panel—usually 6–10 points. The panel is then taken out of the jig and placed between steel plates into the press.

Benefits and Drawbacks

The use of pin lamination and rivets constrain the layers of the boards from moving too much. Holes are generally done by punching or drilling, many times using a time-consuming manual drill. This system usually results in better final registration, but causes large mechanical stress within the boards and limits the throughput of the plant.

On the other hand, pinless lamination is done only in the panel's parameter (sometimes riveting or pinning is also done in this way). The heat bonding around the panel allows for certain movement of the layers, thus permitting some stress-relief. The throughput achieved using this system is larger, but the registration achieved is not as good as with a multiple pin system for rigid-flex PCBs.

Future needs will require better registration, as designs become more complex, denser and more difficult to register. The flex layers' dimensional stability is still low and there are no signs this is going to improve in the near future.

To allow the manufacturability of such boards, new manufacturing systems and registration systems must be developed. This article will demonstrate the results of testing conducted with a newly developed machine (Indu-Bond® RFX) involving the benefits of both the pin and the pinless lamination systems.

The machine bonds the layers using induction heated areas in the boards, permitting these areas to be anywhere within the entire panel, not only around the perimeter of the panel. It also does not limit the number of bonded areas per panel.

Rigid-Flex Registration Process Introduction

Today's engineers involved in the registration and lamination of rigid-flex circuits are familiar with the instability of flexible layer dimensions that may cause misregistration or very inconsistent results after the lamination process.

These distortions are due to the high pressure and high temperature used in the lamination process. Their effects are in different magnitudes due to numerous variables in the process. Examples of the variables are: numerous combinations of stack-ups, various types of materials in combination, layer thicknesses, copper thicknesses, and of course, how the copper is distributed over the surface on each layer. All of these variables do not depend at all on the PCB manufacturer, but rather on the genius and unlimited imagination of the designers, or are simply due to the technical requirements of the final application. The truth is that PCB manufacturers have a substantial technical challenge to get a reasonable yield out of their production.

Basically, those dimensional distortions come from the flexible layers themselves. Despite the fact that there are different flexible materials on the market, none of them have fiberglass inside, which means that those materials or layers lack the internal structure to constrain the natural dimensional changes of the materials caused by the high pressure and temperature changes. This phenomenon simply causes different and sometimes random registration results from one panel to the next, even within the same work lot.

As mentioned at the beginning of this article, most of the high-end rigid-flex manufacturers use many tooling pins around a single PCB unit within the panel to try to minimize the distortions or movements of the layers, especially those of the flexible layers (Figure 5). In fact, this solution has been proven to give better

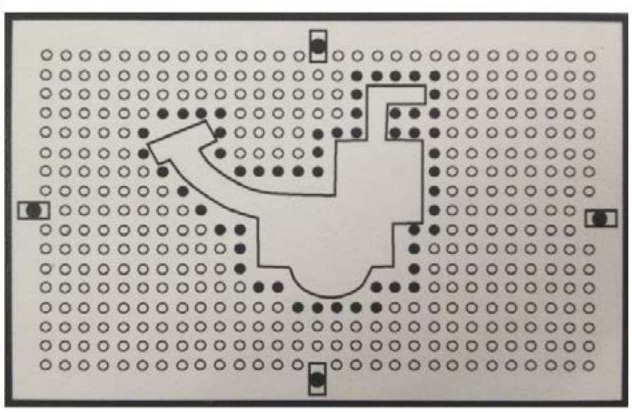

Figure 5: Grid lamination plate.

results than laminating without numerous pins around every single rigid-flex board. However, this system still shows significant low registration yields and other particular issues.

The process is time consuming and manual due to the need of punching or drilling every layer and prepreg sheet in many different locations with high accuracy, which may be different from one job order to the next. This means that a dedicated, accurate template tooling plate with a corresponding configuration of pins is needed to layup the layers for registration and lamination of each particular job.

Obviously, the registration of the layers highly depends on the tooling pins verticality, the pins-to-hole positioning accuracy and the tight tolerance in between layer hole and tooling pin diameter. However, keeping all those parameters under control and stable is tough, not to mention the challenge for the operator to build up thin layers 1–3 mils thick in a multiple pin registration tooling plate (Figure 5) without damaging the layer holes during pin insertion. (Every damaged hole means an extra gap between tooling pin and layer hole that causes layer movement or miss registration.)

The New Process/Equipment Development Introduction

The InduBond® RFX is a new system (process and equipment) that has been developed to improve crucial factors associated with the fabrication of complex multilayer PCBs (rigid, flex-rigid and flex), such as registration and increased yield, while increasing the throughput for today's rigid-flex industrialization. This is possible because the new process explained here joins the benefits of pin-lamination and the pinless lamination together. The capabilities of this new system give PCB manufacturers the tools to deal with the increasing challenge of inner-layer registration requirements of advanced rigid-flex designs.

At the Chemplate Materials in Barcelona, Spain, where InduBond® technology was first developed in 2001, the engineering team is continuously focused on the market need for an improved registration bonding process and on designing new processes to give better capabilities for today's high-end PCB makers.

The registration process starts right after layers have undergone print and etch. Due to the complexity of the flexible layers and the pre-routed prepreg layers, it is very difficult to automate their handling and registration with any camera alignment system, which means that a manual handling process using tooling pins is still required. Therefore it is necessary to create registration tooling holes in every layer. To facilitate this there are several choices depending on the type of material and the layer thickness (post-etch punching, post-etch drilling, and post-etch laser drilling or routing are the most common). In any case, no matter the method, it is crucial for accurate registration that, prior to drilling, punching or lasering the tooling holes, the system measures the front-to-back image registration and layer distortion using etched fiducials. This way, every layer will have the tooling holes with image compensation in the same place.

The next operation makes use of a highly accurate tooling plate (Figure 6), where the layer stackup is prepared by laying up the layers one by one. At this stage, the multilayer is perfectly registered with high accuracy; however, the large distortions, movements and dimensional changes will be determined by the lamination process. The novelty of the new process takes place inside the InduBond® RFX equipment, where the layer stackup is accurately registered by a tooling plate and bonded by induction heating in pre-designated locations anywhere throughout the area of the panel. In this way, the relative position between the layers at this stage of the production is fixed by bonding

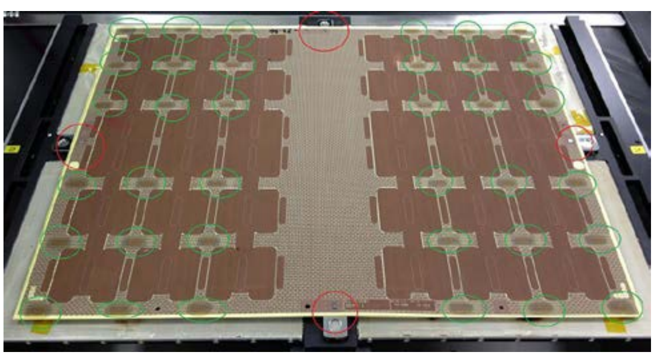

Figure 6: InduBond® registration and bonding tooling plate.

points welded vertically via induction heating (Figure 7).

Following this bonding process, the "sandwich" of layers is removed from the registration tooling plate and moved to the lamination area where it is placed in the lamination press along with outer copper and prepreg sheets. This means that the tooling pins are no longer required during hot press lamination. To better understand the InduBond RFX process, concept and benefits, a detailed explanation is required.

The InduBond® technology is basically a method of bonding the inner layers and prepregs constituting the multilayer printed circuit board by way of induction heating. To facilitate this, there is a need for specific devices to be located at strategic points around the panel that create a high-frequency magnetic field, inducing eddy currents in the copper of the inner layers (Figure 7). The key of this technology is that the energy generated by the eddy currents is transformed into the necessary heat such that the prepreg resins or bond sheets in between the layers will cure or polymerize. In fact, the InduBond® technology creates small lamination points to hold the registered layers held by the highly accurate tooling plate.

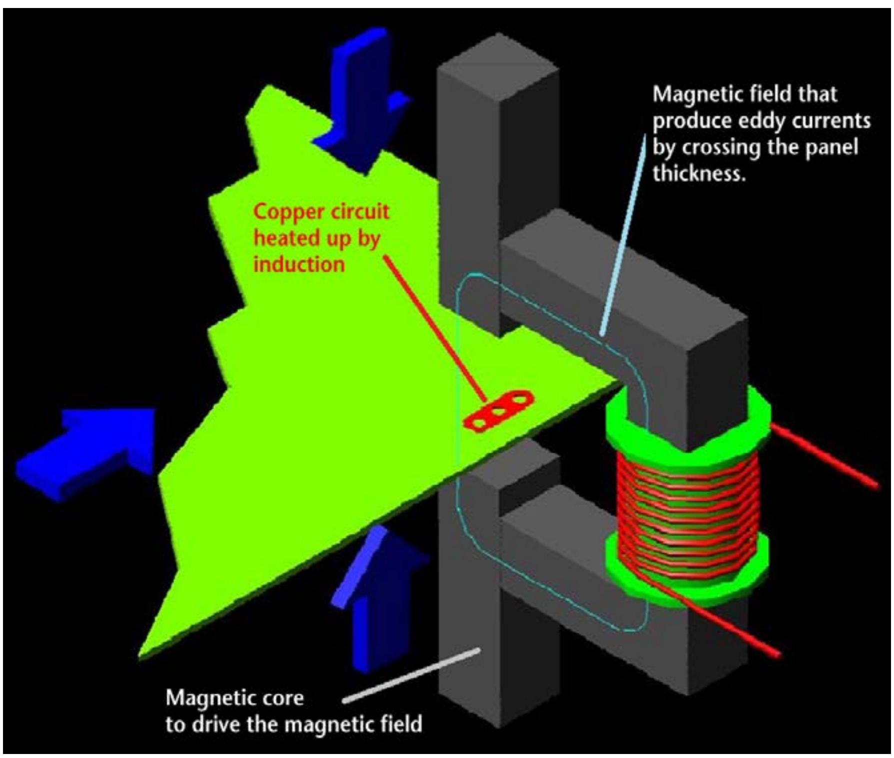

Figure 7: InduBond® principle.

Benefits for Rigid-Flex PCB Fabrication

The introduction discussed the inherent registration problems of today's rigid-flex circuits, and it explained that all layers undergo dimensional distortions, but that flex layers are especially prone to such distortions due to the lack of a stabilizing internal structure of glass fibers (present in rigid layers). The basic novel principle behind the design of the InduBond® RFX system is based on the idea of improving the flex layers' dimensional stability by prebonding them to the rigid layer prior to the lamination process. In this way, the distortions of the layers in the entire inner packet should be similar for all layers, due to the fact that the rigid layers (that have an internal glass fiber structure) will stabilize the flex layers' dimensional expansion and shrinkage that occurs during the press cycle.

Following extensive R&D it was found that if a rigid-flex panel is first registered using an accurate tooling plate (similar to Multi Line's 4-slot system) and bonded with the InduBond® technology (internally and externally) with many bonding points, working as virtual pins similar to the multiple tooling pins all around the PCB, yet laminated without the pin (pinless lamination), the following improvements were realized:

- Less flexible layer dimensional distortion (better scale constrain)
- Better final thickness stability all over the panel
- Better panel planarity or less warpage
- Better pressure distribution and topography

These significant improvements summarized in a phrase mean better yields. Not only does this technology present

PCB manufacturers with higher technical capabilities to face today's complex stackups, but also makes the registration and lamination processes more predictable, simple, repetitive and cheaper.

New Process/Equipment Description

The InduBond® RFX equipment is based on four inductive heads with independent X and Y axis movement. Utilizing this design the equipment is able to bond the panel in any place on the surface without the need for pre-drilling or punching the layers and prepregs sheets to accommodate internal tooling pin. This process is purely automatic, since the bonding points locations are determined at the CAD/CAM stage of the job preparation. The Indubond® RFX equipment simply reads the Gerber file (similar to a drilling or testing machine) and automatically obtains the coordinates of each bonding point without any limitation and with maximum flexibility. The machine simply moves each of the four bonding heads to the desired bonding locations and transfers the energy to cure the resin using a similar thermal profile to a hot lamination press. This process is then repeated until all the bonding points have been fixed. After that, the tooling plate is removed from the machine and pins are retracted automatically to leave the stack-up layers registered and fixed and ready for the next operation (final lamination).

The Test (Introduction)

Eltek knows very well all the mentioned limitations and technical challenges. Their experience and knowledge have been an invaluable contribution to the development of this new process. The equipment has undergone testing at Eltek's Israel facility. This allowed the equipment and process as a whole to be tried under actual industrial production with process variables set by the facility's engineers.

The goal of the test was to probe the improvement in production by using the InduBond® RFX system based on two parameters:

i) By the yield increase compared with the standard process

ii) By quantifying the results based on specific analysis

To quantify these parameters and to isolate them from other variables with the production process was a challenge, and for that reason we developed a very complex test to measure the evolution of the layers' movements or distortions in many locations all over the panel.

The first step was to choose the panel size. An 18" x 24" size was selected in order get significant results, considering that this is a relative large panel size for high-end, rigid-flex boards. An additional reason for choosing this size is due to the high demand for rigid-flex boards; PCB makers prefer to increase their throughput performance by increasing panel size, thus manufacturing more PCB units per panel.

The second stage involved designing a 12-layer rigid-flex circuit, of which six units were incorporated within a single 18" x 24"

CS1	CS			0.5
FR4	RIGID			0.004
2	S			1
	PP		2	0.0035
3	G			1
FR4	RIGID			0.004
4	G			1
	PP		2	0.0035
	PP	CL	1	0.0018
5	G			1
FLEX				0.002
6	G			1
	PP	CL	1	0.0018
	PP		1	0.0035
	PP	CL	1	0.0018
7	G			1
FLEX				0.002
8	G			1
	PP	CL	1	0.0018
	PP		2	0.0035
9	G			1
FR4	RIGID			0.004
10	G			1
	PP		2	0.0035
11	G			1
FR4	RIGID			0.004
PS12	G			0.5

Figure 8: Rigid-flex 12L stackup.

production panel. To quantify the distortions and inner-layer movements, we placed specific targets on each inner layer approximately every 3" in both the X and Y axes. These targets formed a 72-point matrix, which allowed us to measure the relative movement between the individual layers following lamination throughout the panel (Figure 9).

A Pluritec Inspecta X-ray machine was used to measure all the targets, taking about one hour to accomplish the measurement of a single panel with more than 750 values of data per panel.

In the test panels, we define a total of 36 bonding locations symmetrically placed on the panel in between the targets and real PCB units to simplify the analysis of the results.

In order to evaluate the difference between standard pin lamination, pinless lamination and the InduBond® RFX pinless lamination methods, a total of 24 panels were manufactured and divided in three groups (Figure 9):

- Eight panels were bonded only in the panels' perimeter edges (i.e., galvanic frame), labeled group C (yellow on Figure 9)
- Eight panels more were bonded in the galvanic frame and also internally close to the center of the panel, labeled group B (orange on Figure 9)
- Eight panels were bonded all around the surface of the panel, labeled group A (pink on Figure 9)

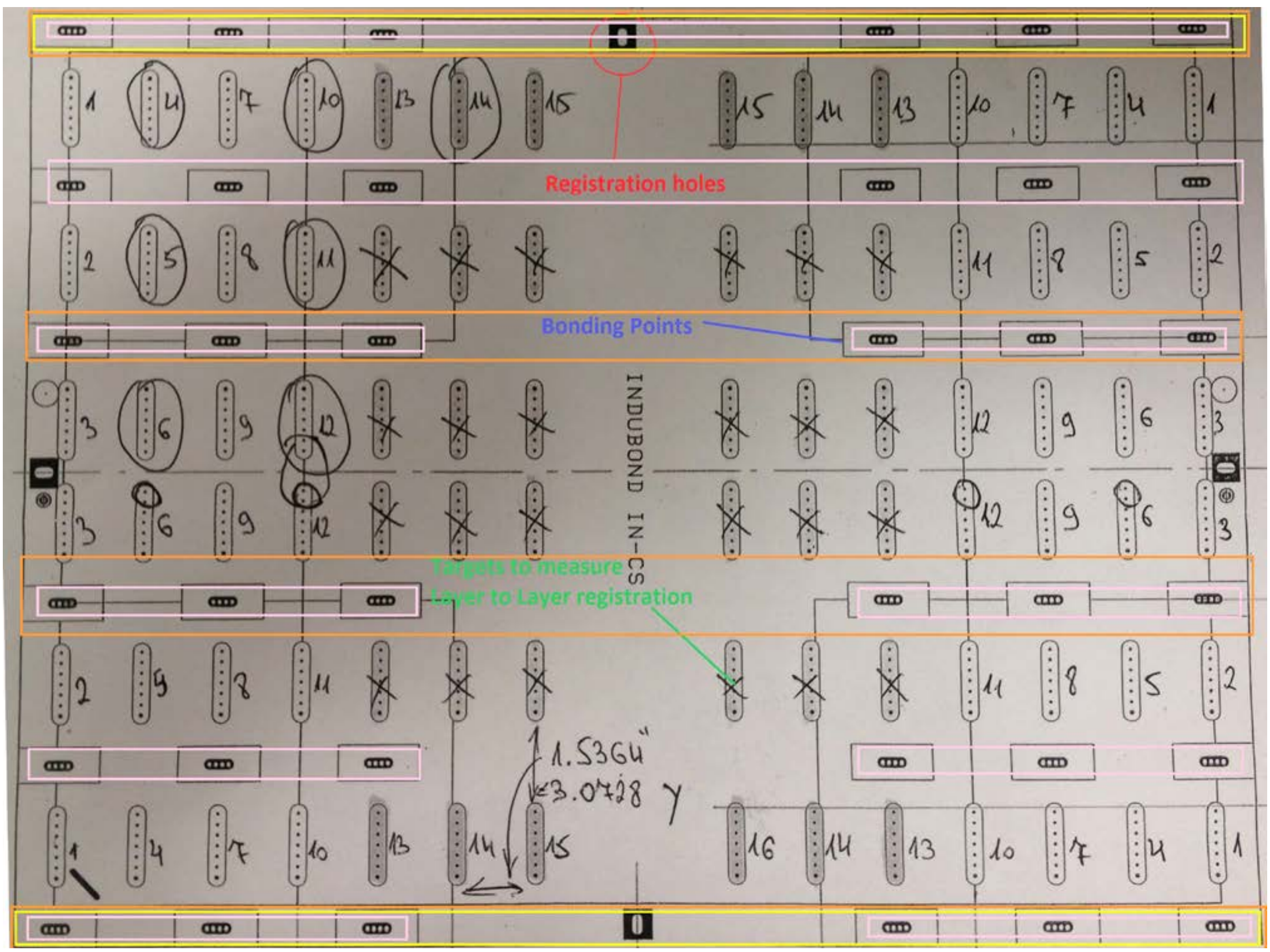

Figure 9: Test panel with four registration holes, bonding locations, targets to measure layer-to-layer registration, and bonding groups.

The Test Execution

All the layers of the 24 panels were post-etch punched with the same machine, (Multiline VPE 4 slots post-etch punch) with an image compensation system. Then, the layers of all 24 panels were registered with the same tooling plate and pins to avoid any error due to different tooling tolerances. The layers registration position, set by the same high accuracy tooling plate, was fixed by laminating small spots using the InduBond® technology. These small lamination spots are referred to as bonding points.

As mentioned before, eight panels were bonded just on the edges; eight more were bonded in the edges and internally close to the center of the panel, and the last eight panels were bonded in the edges and internally all over the panel surface—approximately every 2–3” (Figure 9).

After the InduBond® process, each panel was marked to track every single process variable. All were laminated at the same time in the same hot lamination press (OEM), with the same thermal profile. Temperature sensors were placed on every panel and according to the temperature data logger, and the 24 panels reached the same temperature at the same time with a maximum deviation of 7° C (Figure 10).

After lamination, the 24 panels were flash routed to remove resin flow from around the frame and visually inspected. All of the panels (independent of their group) were very flat as checked in reference to a granite table, with a maximum bow or bending effect of 0.1524 mm (0.006”) for an 18 x 24” panel size. This translates to good flatness in terms of a single final board (<0.75% of thickness according to the norm for surface mount components) (Figure 11).

The topography of the panels was also uniform at less than 10% of the average thickness. The maximum difference measured was 0.0975 mm (0.004”).

The next and most valuable step of the test was to measure the relative position between every inner layer within the test panels at numerous points using an X-ray (Figure 12). To analyze and understand all the measured data, a very powerful measurement analysis tool developed by Xact PCB in the UK was used. All the data acquired from the X-ray machine was stored in a data base readable by the Xact software, where with the help of the Xact PCB team we were able to study the results.

With a relatively small sample of only 24 panels of 8 panels per each group, a lot of data was collected to at least certify a tendency. The analysis revealed that all 24 panels had good registration. However, the group of eight panels that were bonded at several points inside the panel area (group A), and displayed better scale constrain in between the layers, especially when comparing flexible layers. In other words, the superposition of a single pad on each layer,

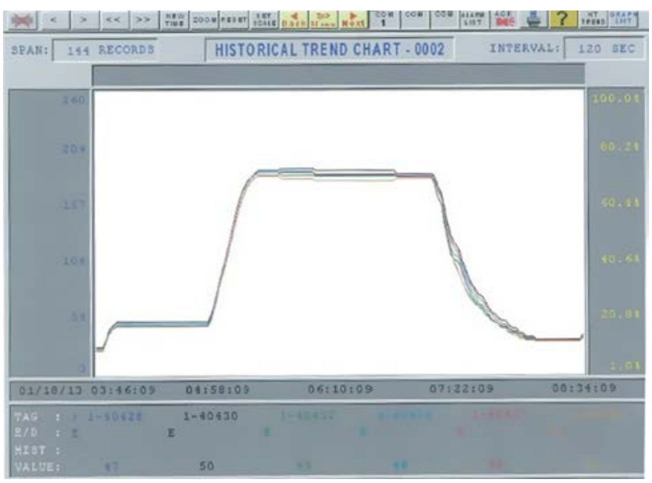

Figure 10: Lamination thermal profile.

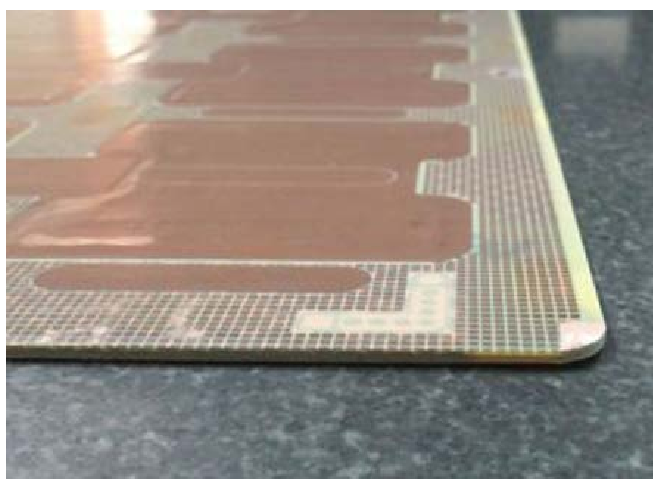

Figure 11: Panel planarity and topography.

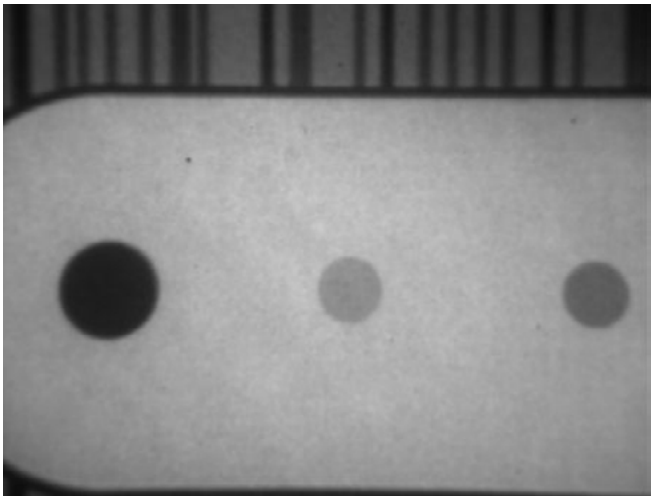

Figure 12: X-ray view of the measurement targets.

including those on flexible layers, was on average tighter, thus allowing improved interconnection after drill and plating processes.

Test results

As mentioned, data was collected and produced within the scope of this test that cannot be included in this article for obvious reasons, so to illustrate the results efficiently several screenshots are displayed as evidence of the differences found between the test groups.

The pictures show the results of the X-ray measurements just at one set of targets located on the corners of the panels, where the dimensional distortions are usually the largest (target 4 on Figure 9).

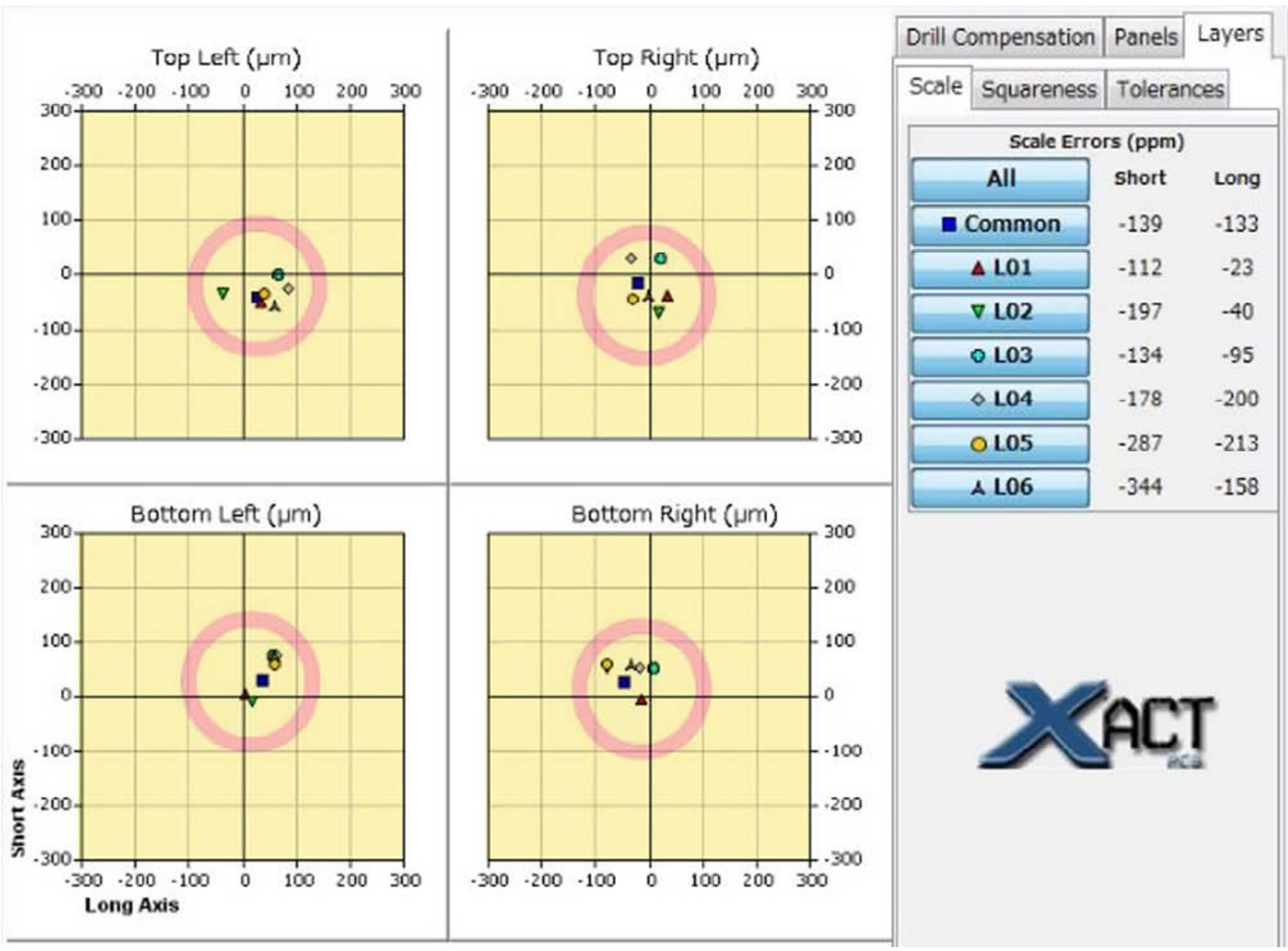

Figure 13: The relative position in between all the layers of one of the panel from the group of panels that were bonded only on the edges of the panels (group C).

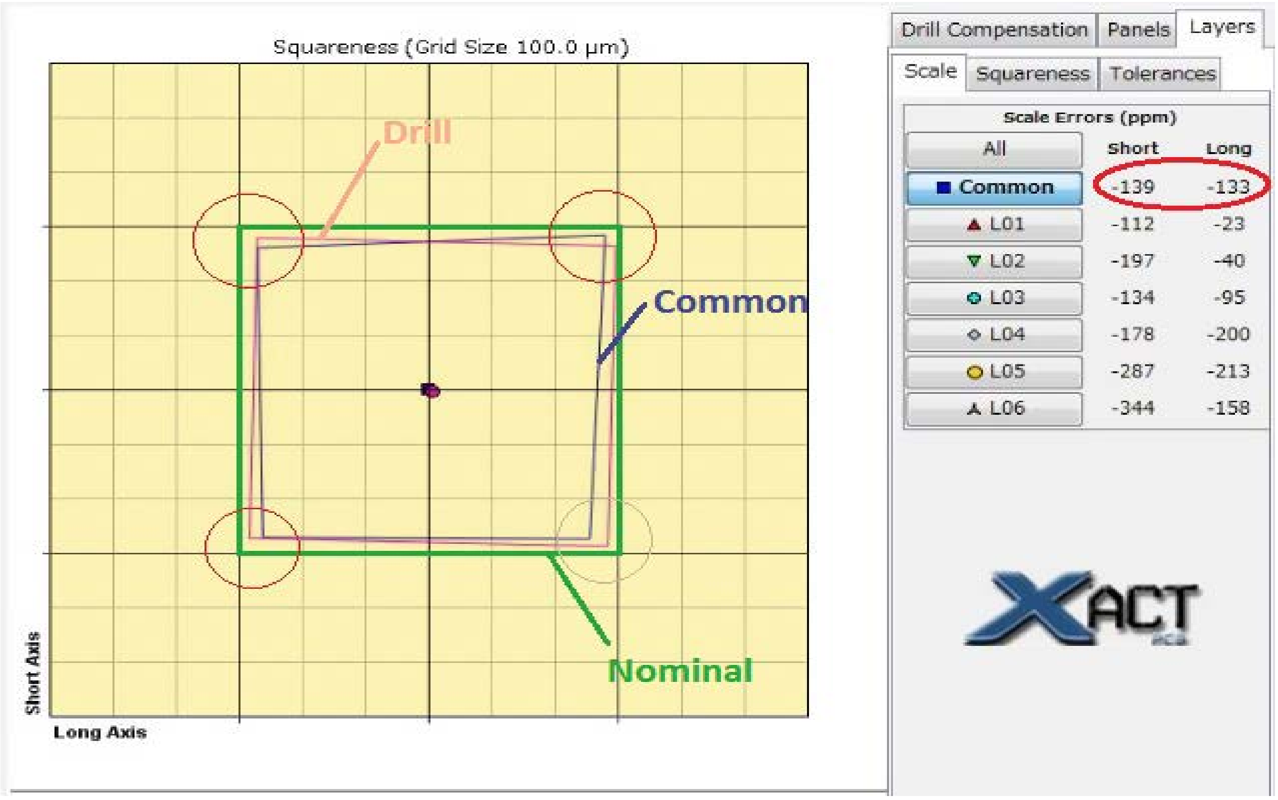

Figure 14: The squareness of the common, the nominal and the drilling compensation (group C).

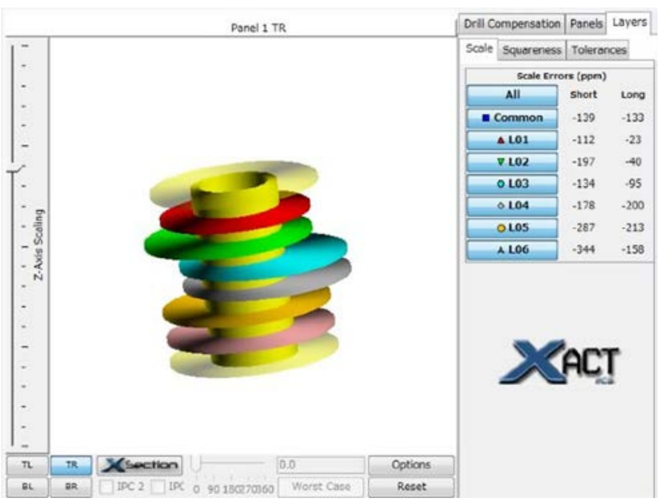

Figure 15: 3D representation of one of the measured targets with its best drill position (group C).

To summarize, the above figures are representative of all the analyzed results for the same location in each of the two groups (A and C). From the figures, the following can be deduced:

1. Panels in group A (bonded in many internal and external locations) display the common dot that represents the center of the pads' superposition (the coordinates for optimal drill position) very close to the nominal value.
2. The layers relative target positions in all of the test groups were all within the same magnitude of measurement, but were closer to the nominal in group A—proving a local shrinkage constraint.

Registration Process Improvements

Looking at all of the process stages, improvements were found across the board, which include reduction of time-consuming processes, less manual operations, less material preparation, less tooling and less tooling maintenance. Figure 19 summarizes all the differences or improvements that were found during the entire manufacturing process with the new InduBond® RFX process compared with the traditional process.

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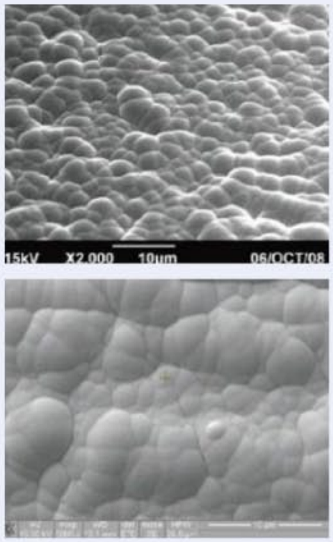

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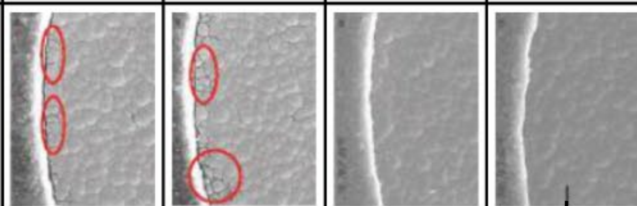
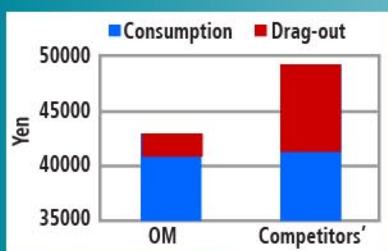
Au bath	Conventional IG	Conventional IG	OM	OM
Au content	2g/L	1g/L	1g/L	0.5g/L
NBath	Conventional Ni	Conventional Ni	930	930
SEM				

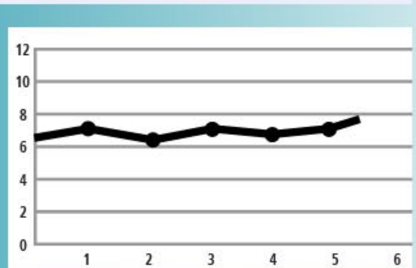
Ni attack is heavier in low Au

Ni attack not observed at 1g/L

New Combination OMG 930 and OM Gold will further decrease the potential for Ni attack



Au cost for 10g plating



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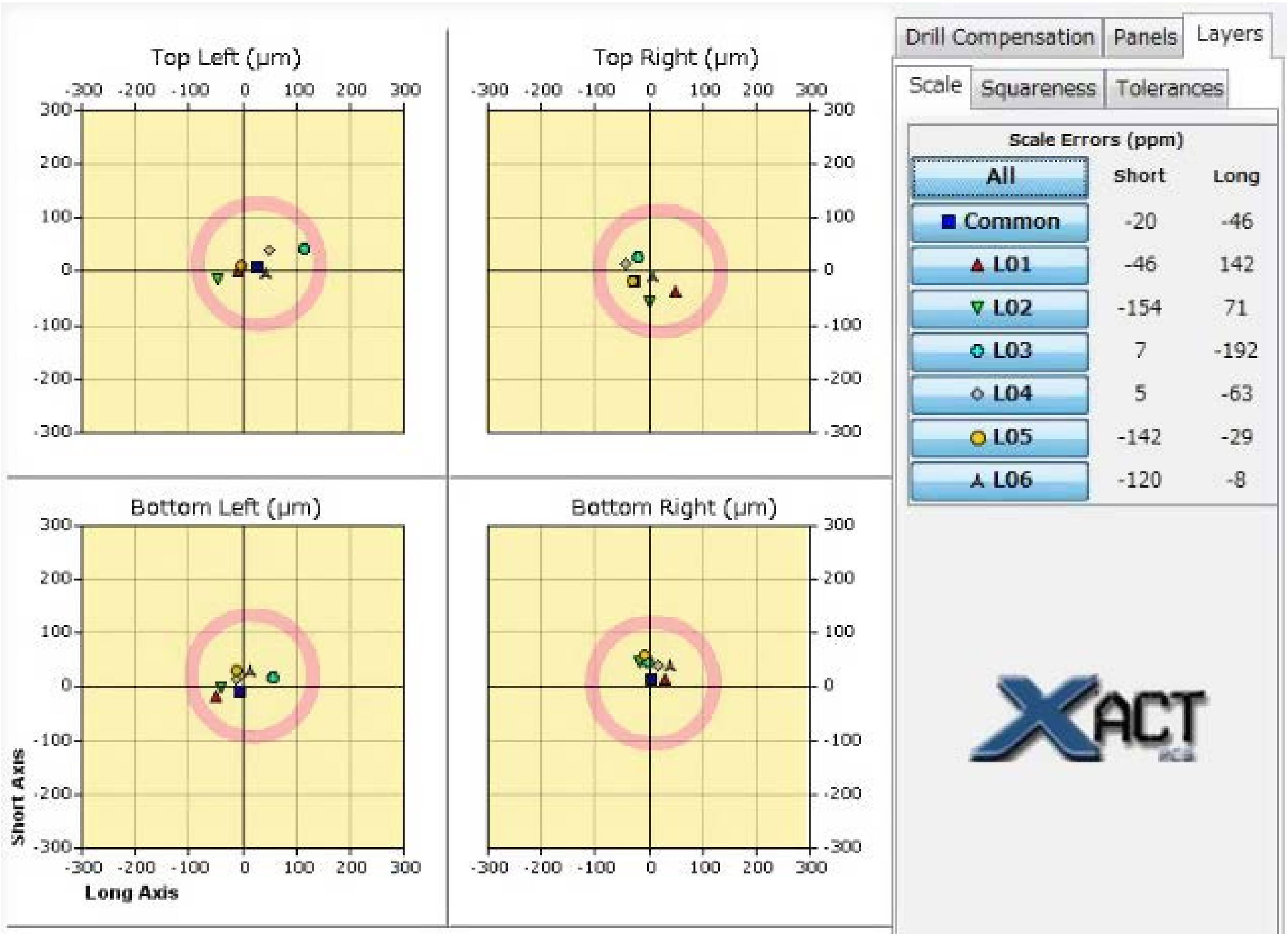

Figure 16: The relative position in between all the layers of one of the panel from the group of panels that were bonded internal and external of the panels (group A).

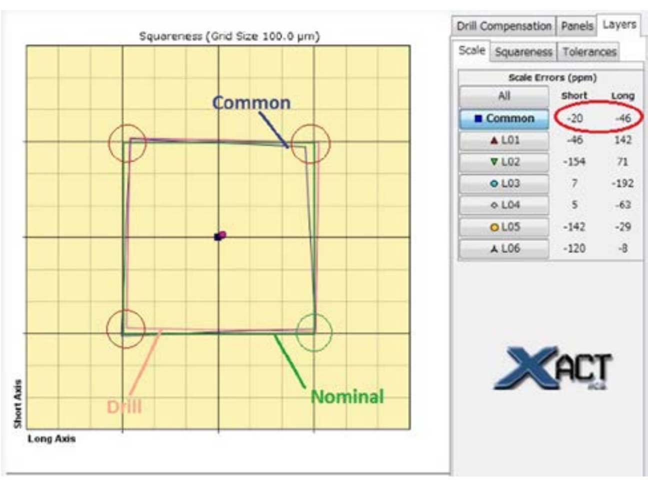

Figure 17: The squareness of the common, the nominal and the drilling compensation (group A).

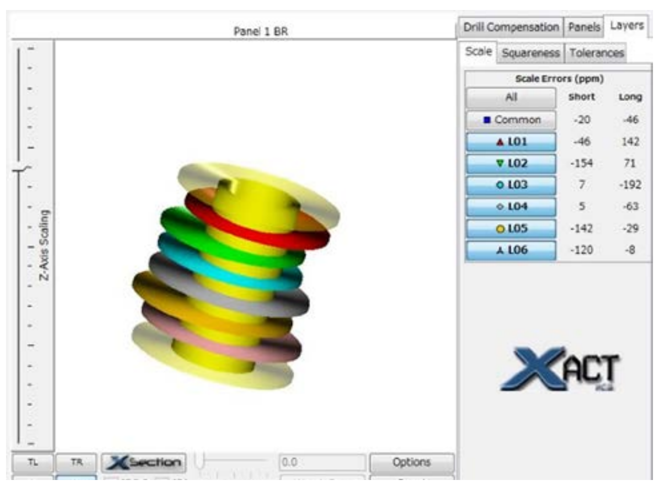

Figure 18: 3D representation of one of the measured targets with its best drill position (group A).

Process Stage	Traditional Pin Lamination	InduBond®RFX Pin Less Lamination
Material Preparation	All layers, prepreg sheets, outer copper foils, and release films need to be punched or drilled in all desired locations for each internal/external pin (expensive).	All layers, prepreg sheets, and outer copper foil need only four oblong punched holes for the registration process.
Registration	Layers need to be punched to be registered over the tooling pins and all holes made with image compensation system to get the holes of each layer in the same relative position. Holes are usually round.	The layers are accurately post-etch punched with four oblong holes with image compensation system (fast process).
Lay-up	Because there are many holes and pins, the laying up process is very slow and difficult due to the complexity of the insertion of thin cores in many pins, at the same time, without damaging the layer holes.	Robust and simple process because the lay up is made on four oblong and short pins, limiting the risk of damaging holes (faster process).
Tooling	Pins needed during the lamination process are numerous (many accurate tooling plates and pins, usually 1-1/2" (expensive).	Pins are not needed for lamination process, only one tooling pin (short pin) is needed just for registration purposes.
Bonding Process	Pin lamination does not need the bonding process because layers are laminated with the registration pins.	Bonding process is required prior to lamination process.
Lamination	Numerous pins during the lamination process requires many separator plates tooled and for different panel sizes.	No pins during lamination means far fewer separator plates, and most of them are suitable for different panel sizes.
Depinning	A depinning process is required after lamination to remove the pins.	No depinning process is required (no pins in the panels).
Tooling Maintenance	Tooling maintenance is crucial to keep all of the pins, bushings, and plates clean and in best shape possible in order to not add errors to the registration from the stress of lamination and depinning.	No maintenace is needed; the tooling plate, pins and bushings have long life expectancy because the tooling plate is not suffering the lamination stress. Separator plates are not soiled by resin flow because they do not have holes.

Figure 19: Pros and cons of traditional vs. InduBond® RFX process.

Conclusions

From the test results, it can be seen that this innovative method and process is capable of creating a clear constraint to the shrinkage phenomenon of the materials while the registration stays stable or even improved in between the layers. This is just what is needed in the high-end, rigid-flex boards due to the local tight registration required in some locations of the board that are usually affected by big flexible layers' random movements. After Eltek used this new process in its Tel Aviv facility for one year, the company experienced a nice percentage of yield increase, particularly on high-end rigid-flex, and a faster process time.

It can also be said that the pinless lamination is less expensive to produce, and faster and easier to manufacture. This new piece of equipment, using inductive currents to bond the layers, successfully improves the manufacturing of rigid-flexes. **PCB**

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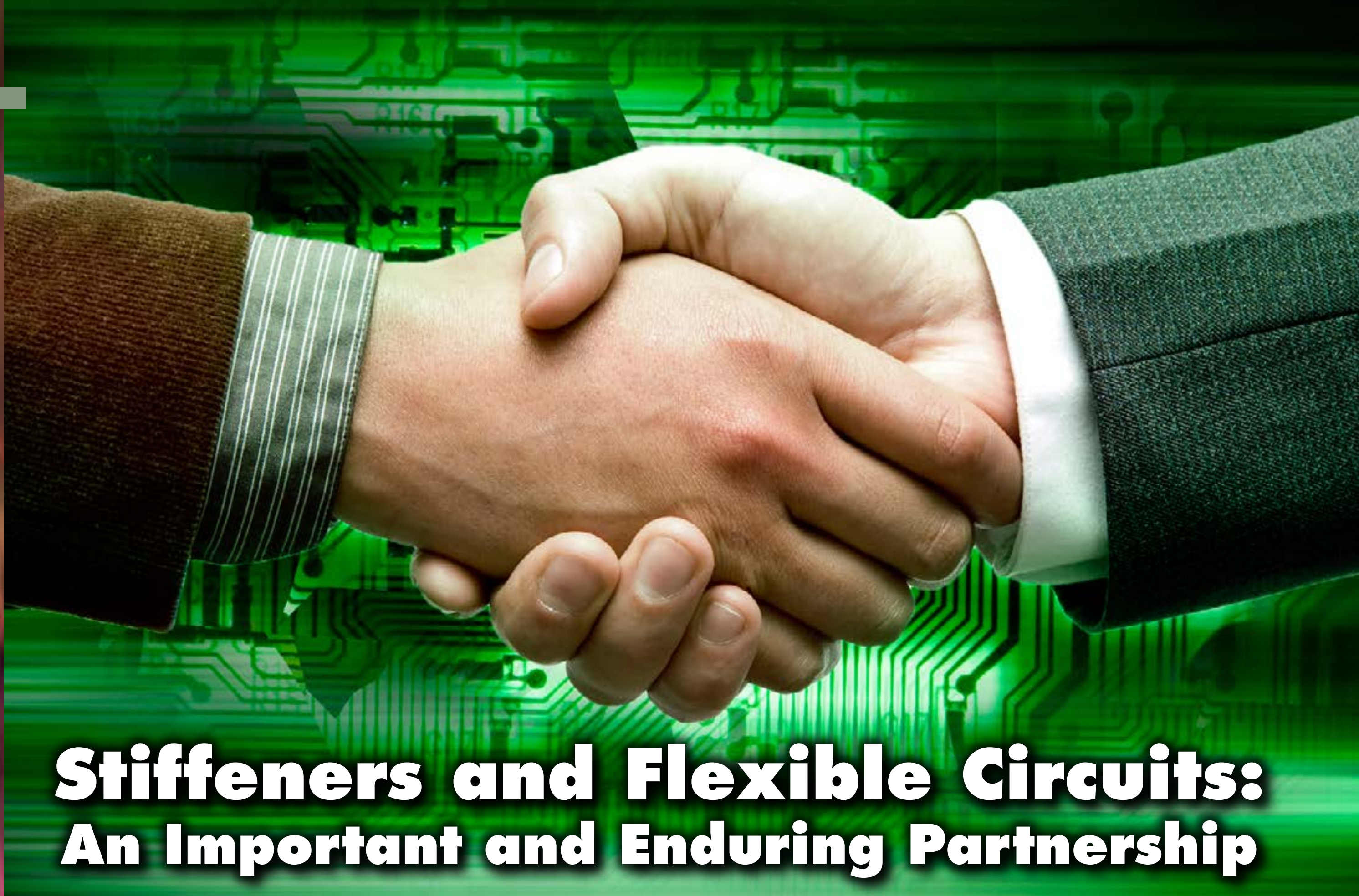
Roberto Tulman is vice president of technologies and CTO at Eltek. Contact Tulman at tulman@eltek.co.il.



Stiffeners and Flexible Circuits: An Important and Enduring Partnership

By Joe Fjelstad
VERDANT ELECTRONICS

SUMMARY: Flexibility is the stock and trade of flexible circuit technology; however, rigidity has its place and stiffeners help to supply that important attribute when and where needed. There are many possible avenues leading to your destination.

Introduction

Flexible circuits are well suited to the needs of a wide range of electronic products and have thus become a go-to solution for product designers around the globe. While flexibility is an obvious attraction, a flexible circuit is inevitably integrated in some manner to one or more rigid elements somewhere in the design. Most often, these rigid elements are used to support other electronic components which run the gamut from discrete devices and integrated circuits to connectors of varying types.

Where needed, stiffeners or reinforcements are most commonly used to support components on flex circuits, though they are also found in areas where the tail of the flex circuit is designed for edge connection to a mating connector. These important add-ons can be fabricated from a wide range of different materials depending on design need. The choice of material is predicated on what design objectives are sought and those objectives can be surprisingly varied. In one application, an objective might be to support components while keeping the weight down. In another application, the thermal conductivity of the stiffener might be a consideration if the components mounted thereto generate significant heat. In yet another application, it might be an objective for the underlying stiffener to serve as resilient bridge in areas that will return to a specific location following bending.

Stiffener Material Choices

Accordingly over the course of flexible circuit technology's history, a wide range of materials have been employed. Following is a review of some of the materials which have been used as stiffeners in the past.

Composite laminates composed of organic resin and glass (either woven or nonwoven) have been a mainstay choice owing to their

ubiquity in the printed circuit industry. While normally used without copper cladding, the copper foil surface option is available for appropriate technical requirements such as shielding.

Because stiffness increases as a cube of thickness, even low modulus materials such as the polymer films commonly used as coverlayers can be and have been used with success in the past. It is important to keep in mind that if polyimide is chosen, the cost will be higher than a material such as FR-4.

Thermoplastics, either filled or unfilled and in either sheet or molded form, are another viable option of record in flex circuit manufacture. In fact, a molded stiffener offers some interesting possibilities where the flex circuit can be made to conform to the contours of a predetermined molded shape. In this regard, it is possible to insert mold a flexible circuit into an injection mold cavity and it has in fact been done in some applications.

Metals and metal alloys, stainless steel, spring steel, beryllium copper alloys and various aluminum alloys can also be stiffener options. Metals are great thermal conductors that may benefit some applications; however, one should bear in mind that they can make soldering more challenging. In the case of aluminum, it is worth remembering that the metal can be anodized, by converting the metal surface to nonconductive Al_2O_3. With that thought in mind, ceramics and glasses can also be used to advantage in certain applications.

Beyond these choices, it is worth remembering that the package or box into which the circuit is to be placed can also be used as the stiffener if the design allows. In this case, beyond simple component support, the technique could allow for the package or the box itself to be used for other purposes such as heat dissipation or assembly complexity reduction. This latter case, while a potentially attractive solution for a number of applications, could present significant difficult if rework or repair is required as removal of the circuit would likely damage the flex circuit.

Adhesives for Bonding of Stiffeners

Obviously, the attachment of a flexible circuit to a rigid base will require an adhesive. Conveniently, all of the bonding adhesives used in the manufacture of flexible circuit laminates are candidates for attaching a flex circuit to a stiffener; however, the list of options is actually not limited just to them. In practice, the choice of which adhesive to use is a function of performance requirements of the end assembly. Following are examples of some of the families of adhesive which have and can be used.

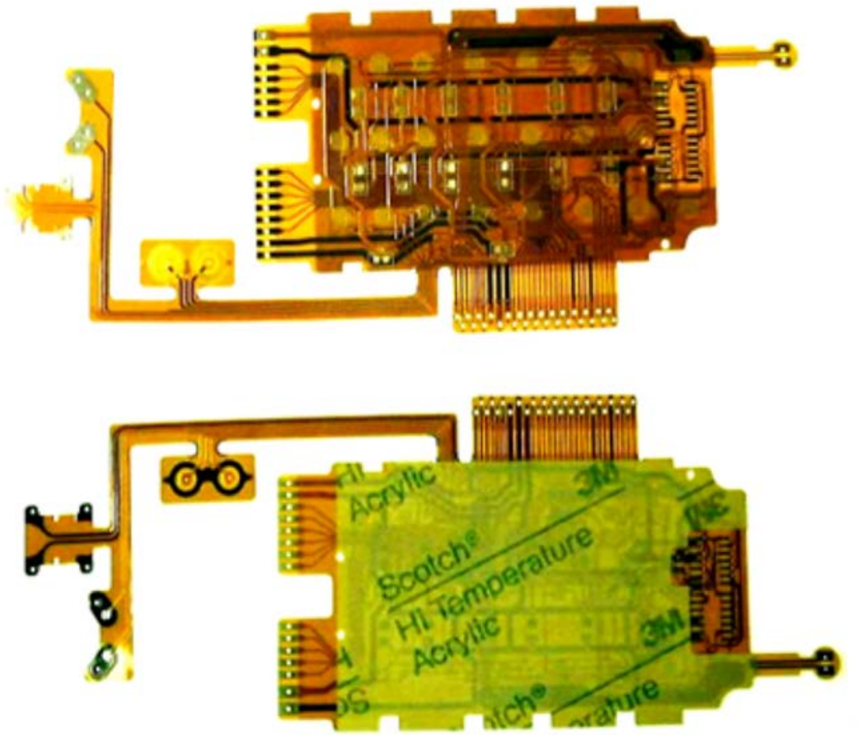


Figure 1: Shown above are the front and back of a flexible circuit with a pressure sensitive adhesive pre-applied to the side opposite the active side allowing it to be bonded directly into an assembly. (In this case an apparent flip phone application.) Note that the adhesive required pre-machining to establish some of the adhesive pattern before being applied to the back. When punched out, the external outline defined the rest of the adhesive pattern.

Pressure sensitive adhesives (PSA) are very commonly used to attach stiffeners. They are perhaps the most versatile and easiest to use from a manufacturer's perspective and thus are likely to be the most cost-effective solution. PSAs exhibit very good bond strength, which in some cases actually improves with age. These adhesives are not generally designed for extended use at high temperatures, but for the most part limited to enduring only short excursions at high temperatures (e.g., soldering temperatures). Because of the challenges of high-temperature lead-free solder, there is need to verify the capabilities of the candidate adhesive before committing to wholesale use. One particular advantage PSAs offer over other adhesive choices is that, when applied directly to the flex circuit, they allow for the flex circuit to be bonded to virtually any surface, thus effectively making anything in the package a potential stiffener (Figure 1).

Thermosetting adhesive bonding films (e.g., the cast acrylic, epoxy and polyimide films and/or flex circuit bond plies which are used in flexible circuit manufacturing) can also be used to bond flex circuits to stiffeners, but they require the time and expense of an additional lamination step. However, thermosetting film adhesives can offer the benefit higher bond strength of the flex to the stiffener.

In addition to thermosetting adhesives, thermoplastic based adhesive films for bonding flex circuits to stiffeners can be employed. Thermoplastic films have some unique advantages among adhesives in that they are typically relatively low stress, fully polymerized polymer resins that require no cure. With properties that include acceptable adhesion to a wide variety of surfaces and materials, and the reported ability to be reworked easily (though rework is most desirably by controlling the process), these adhesives can be a good option.

Another choice for bonding flex to rigid is liquid one- or two-part epoxy type adhesives, which have also seen occasional use in bonding stiffeners to flex circuits. They can be difficult to apply uniformly and thus they do not enjoy wide popularity. However, such adhesive materials are well suited for the creation of strain relief at the transition edge of the flex and stiffener by creating a bead of epoxy along the entire edge of the transition; this can prove an important feature in some flex circuit designs (Figure 2).

Finally, there are ultraviolet (UV) curable adhesives. UV adhesives have been used in a number of different industrial and consumer product applications over the years and are another potential adhesive choice for stiffener attachment. With some screen printable formulations, the UV "activates" the polymer creating a tacky adhesive with PSA qualities. In addition, because they can be rapidly cured, they are also a potentially attractive choice for strain relieving the flex circuit at the transition point from rigid to flex.

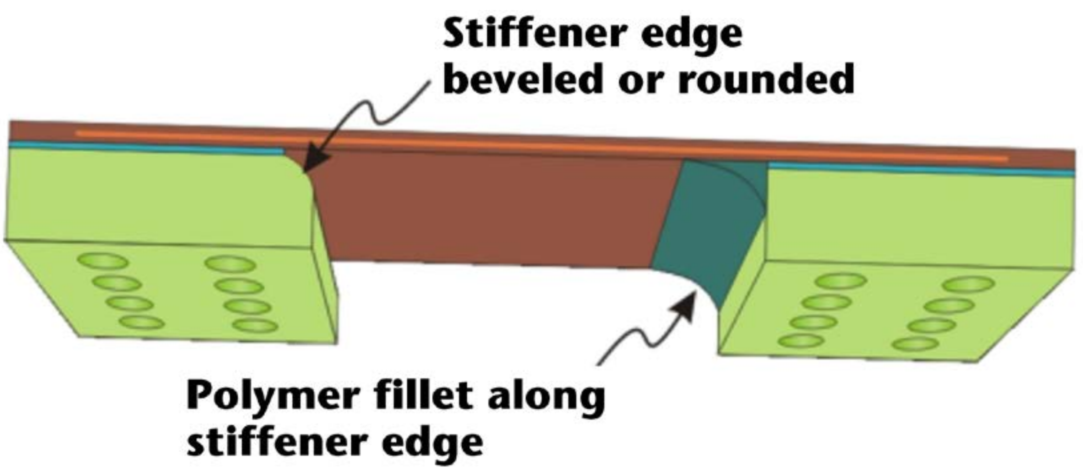


Figure 2: Strain relief at the flex to rigid transition helps minimize potential for focus stress.

Other Benefits of Stiffeners

Beyond just providing component support in a product, with a bit of forethought, stiffeners can aid in the manufacturing process, especially when it comes to assembly. Following are some examples of flexible circuit stiffeners serving to help in the handing and movement of flexible circuit designs through the assembly process.

Route and retain methods are used in the manufacture of traditional PCBs to facilitate component assembly, and the method can be applied usefully stiffeners for flexible circuits; as well though, some additional steps are often required. In one representative example, flexible circuits are bonded to a stiffener using an appropriate adhesive and then the combined assembly is partially NC routed or cut to shape and held in place by tabs at predetermined locations. When preparing the parts, routers are pervasively used in circuit manufacturing; however, lasers and water jet cutters are also viable manufacturing choices for both pre-cutting and post stiffeners.

The adhesive is necessarily prepared so as to limit its application only in areas where the stiffener and flex are desirably permanently joined, which would normally include the periphery of the panel. Following assembly, the parts can be broken apart into individual circuits (Figure 3).

When the flex circuit and stiffener are bonded together, the resulting flex circuit panel can be processed much like a rigid board (the adhesive is applied oversized and cut to dimension during the routing step). While Figure 1 shows the adhesive on the rigid portion, it can alternatively be applied strategically to the flexible circuit, as was shown in Figure 1.

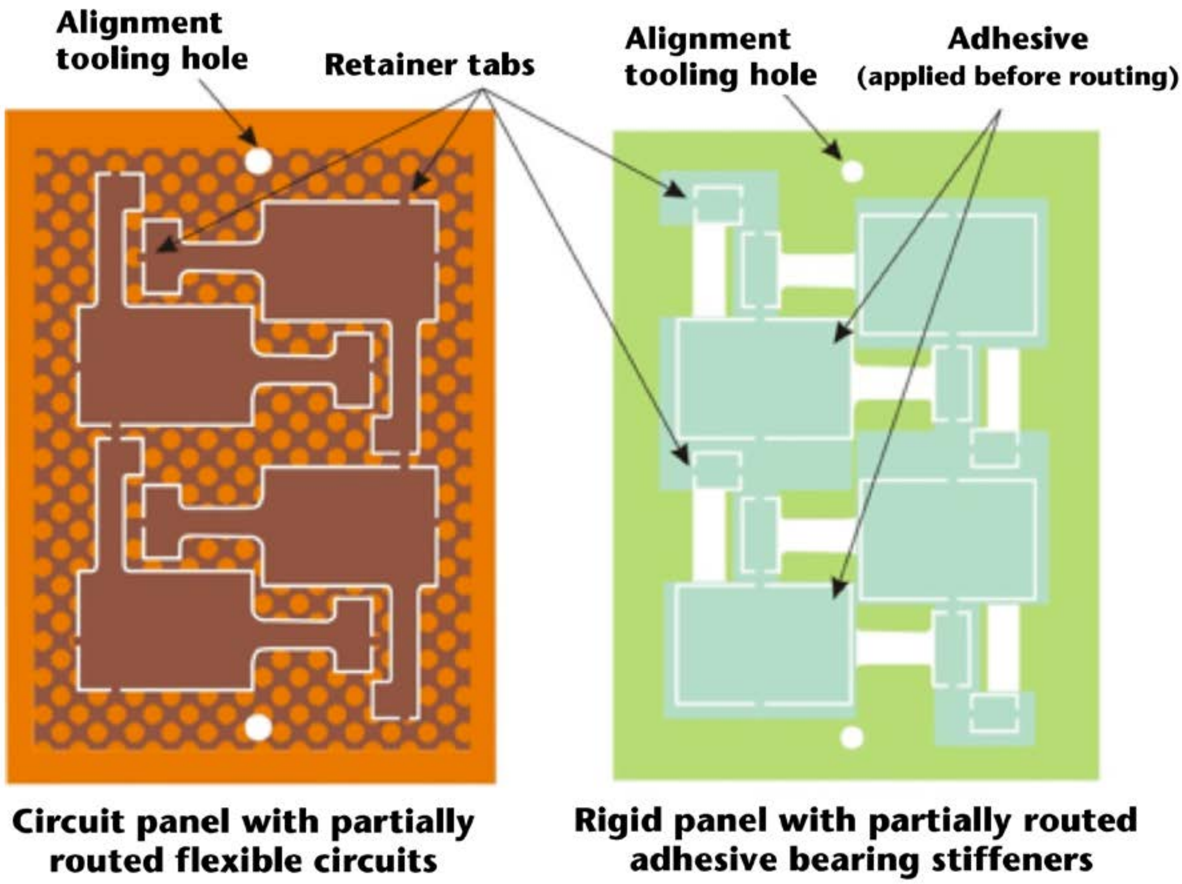


Figure 3: Beyond supporting the components in a final product application, stiffeners can, with some forethought, also serve an important secondary role, streamlining the assembly process by allowing for the mass application of stiffeners to the flex circuits while both are still in panelized form.

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Another option for preparing the stiffener is a method called "return to web punching" (also referred to as "punch out, punch in"). This method requires special punch tooling wherein the rigid material is first punched out of the panel and then is immediately pushed back into it original position in the panel using an "interference fit." The method has been used in the manufacture of inexpensive rigid boards in the past and allows mass assembly with relatively simple assembly fixture requirements.

Depending on the nature of the flex circuit design and its layout, scoring and dicing solutions commonly used in many rigid circuit designs could prove useful. Since scoring and dicing are fundamentally performed using linear and orthogonal cuts, the features of the flex circuit should conform to this need. In the scoring process, the circuit and/or the stiffener is cut partially through using special tools cut a controlled depth straight path through the rigid material alone or through both flex circuit and rigid base. After assembly the circuits can then be snapped apart along the score lines, though if the method is chosen, the bending to snap should be performed into rather than away from the flex circuit to avoid potential damage to the flex circuit.

Other Stiffener Design Issues

As discussed earlier, the edge of a stiffener supported flex circuit transitions from rigid to flex is an important place to consider because these transitions represent locations where stress risers are possible and where damage to the flex circuit because of strain is a real possibility. For this reason, flex circuit designers often call out for the application of a bead of resin be applied to the transition to help protect the area from damage. It is an extra step that may not be required in all cases but it is a practice with a long history and one that is favored by military designers to help make their products more robust. Refer again to Figure 2.

Stiffeners are often provided with holes for both mounting of the assembly and through-leaded components, which are still common for connectors even though surface mount technology dominates electronic design these days. Perhaps not surprisingly, the diameter and relative sizing of mounting holes for components and those for final flex circuit assembly mounting have different purposes and often somewhat oppositional requirements. The result is that the design rules can vary considerably depending on the application.

For example, holes in the stiffener provided to accept through-hole mounted electronic components, such as dual in-line packages (DIP) and various connectors designed for through-hole mounting, should be 250 µm–375 µm (0.010"–0.015") larger than the through-holes in the flex circuit which, in turn, are by design rule, 250 µm (0.010") larger than the lead. This

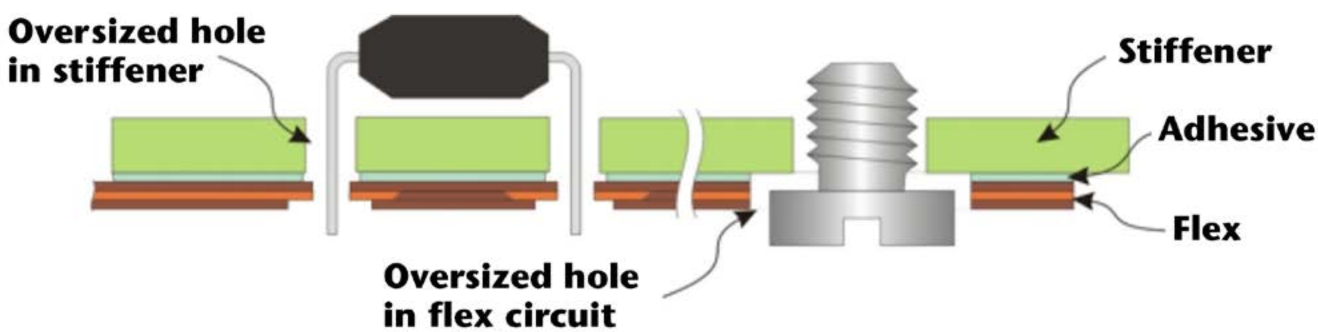

Figure 4: The relation of the relative hole sizes for component mounting and assembly mounting are desirably different due to their differing roles as illustrated and described in the text. While predrilling of the stiffener is a common practice, it is not out of the realm of possibility to drill holes for stiffened single-sided flex circuit assemblies after lamination rather than before, which is the more common practice and one required for through-hole circuits (rigid-flex circuit constructions obviously excepted).

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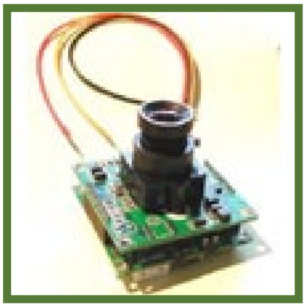

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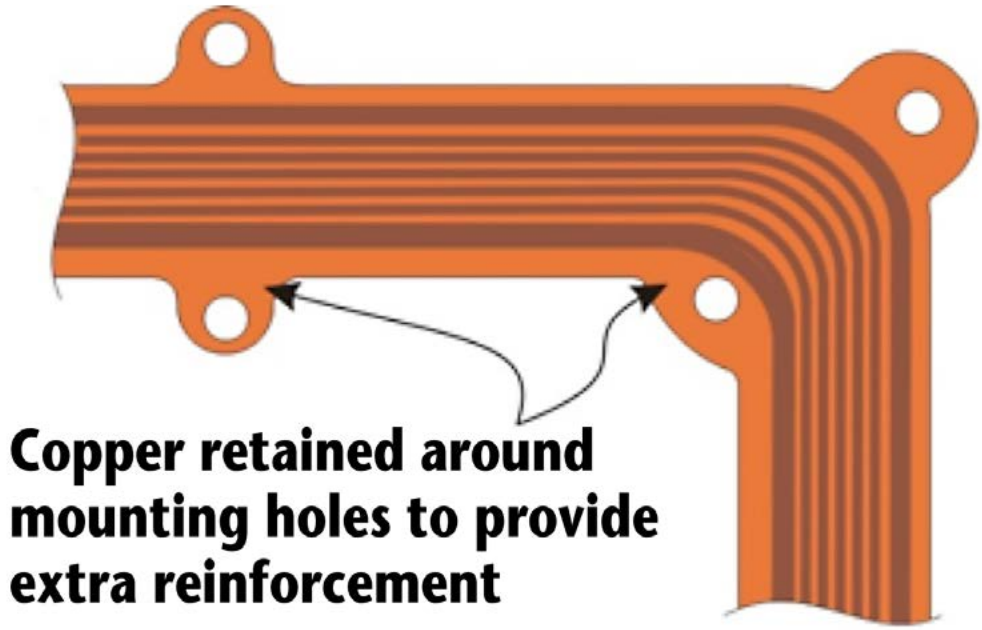

Figure 5: Mounting holes should retain copper when flex circuit is to be mounted without mechanical support. This is a more robust solution than unsupported polymer.

is to allow for any movement and misregistration between the flex and the stiffener that might occur during the stiffener lamination or bonding process. This technique also helps to assure the greatest opportunity for accessing the through-hole with the component lead without interference from the stiffener. In contrast, assembly mounting holes should be equal to or slightly smaller in diameter than the holes in the flex. This assures that the stresses are placed on the rigid portion of the assembly and not on the flex circuit. Figure 4 illustrates the concepts.

The prescription of a stiffener is not always a universal one, as it is possible to mount the flex circuit directly onto a carrier without a stiffener, using common mounting hardware if required by the design. Such holes are referred to as unsupported mounting holes. When the designer opts for this approach, the circuit should be designed to maintain copper around the hole for added strength as illustrated in Figure 5. This practice is of value with regular mounting holes as well if the design will permit. Such features are also a convenient means of making a solid connection to ground on the circuit if the design allows.

Summary

Flexibility is the stock and trade of flexible circuit technology; however, rigidity has its place and stiffeners help to supply that important attribute when and where needed. As has been shown there are many possible avenues to getting to your destination. It is suggested that the designer discuss options with their flex circuit vendor for their recommendations as their experiences are likely to provide good directions to getting you where you need to be. **PCB**

Note: *Flexible Circuit Technology,* 4th Edition is available to the reader as a free download at: www.flexiblecircuittechnology.com.

Verdant Electronics Founder and President Joseph (Joe) Fjelstad is a four-decade veteran of the electronics industry and an international authority and innovator in the field of electronic interconnection and packaging technologies. Fjelstad has more than 250 U.S. and international patents issued or pending, and he is the author of Flexible Circuit Technology, 4th Ed., available as a free download.

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Figure 1: Polyonics flexible substrate, with high-resolution clear printable top coat and printed electronics circuit.

Printed Electronics from a Flexible Substrate Supplier's Viewpoint

by Dave Genest
POLYONICS

SUMMARY: The printed electronics industry continues to make great strides towards commercial success. One of the key determining factors is the availability of durable, printable substrates that combine unique high-performance characteristics with affordability.

The Promise of Printed Electronics

Printed electronics is a sure bet that has yet to pay out, at least on the scale experts predicted a decade ago. It makes so much sense that everyone involved with the technology comes up short when asked why it hasn't taken the world by storm. The best reason is the classic, "The technology hasn't matured enough to drive prices down to where it's an economically attractive alternative to traditional PCBs."

We've seen some encouraging interest in flexible substrates primarily from the printed display and flexible circuit industries, but the real deal—consumer electronics—continues to circle around the potential. For many years, we've been at the tipping point where the materials and technology advancements are improving, but the big guys haven't taken the plunge, which of course would then lower the cost to an acceptable level for the rest of us.

Printed electronics uses traditional, low-cost printing methods (flexo, laser, thermal transfer, dot matrix, inkjet, offset, gravure, etc.) to create electrical devices on ultra-thin, flexible substrates. This is done by depositing conductive or semi-conductive inks on flexible substrates to create functional electronic and/or optical circuits consisting of active and passive devices. These include thin film transistors, resistors, capacitors, light emitting diodes, etc.

Clearly the benefit of printing electronics is derived from its promise of low-cost fabrication. One area that has enjoyed some level of success is RFID systems. These devices enable contactless identification in trade, transport and tracking such as book inventories in libraries. Printing on flexible substrates also allows electronics to be placed on complex, curved surfaces freeing the designer to use more modern shapes in their designs. Examples are printed displays on automotive instrument panels and solar cells on vehicle roofs.

However, the big opportunity for printed electronics lies in the consumer electronics market where conventional semiconductors, even with their higher costs, are more than justified due to their higher performance compared to even the most technologically advanced printed alternatives. But the bets are placed on print-

ed electronics displacing traditional electronics in the very near future.

The two major elements required for these bets to pay off are flexible substrates and conductive inks.

Flexible Substrates

Printed electronics requires a unique blend of high performance and low-cost substrates used to print the circuits on. The substrates need to be thin, flexible, durable and electrically insulative materials that, most importantly, need to not only be printable, but able to accept super fine, high resolution conductive ink patterns.

Paper substrates have enjoyed some initial success due to their low cost, but this has been primarily limited to low-tech products due to the paper's high roughness, low resistance to temperature, flammability and absorbency.

Polyester (PET) has been a more common choice, due to its low cost and high temperature stability. But it too suffers from being highly flammable, having a limited temperature range and weak chemical resistance.

Polyethylene-naphthalate (PEN) is another high-performance film that is particularly applicable to printed electronics. Compared to PET, PEN offers a higher temperature range, better chemical resistance, clear films and higher prices.

Polyimide (PI) is perhaps the most uniquely suited for printed electronics. Compared to the other films mentioned, PI provides higher (and lower) operating temperatures, strong resistance to the majority of chemicals used in PCB manufacturing and superior dimensional stability. In addition, PI offers exceptional mechanical and electrical properties including high tensile strength and dielectric breakdown. It's available in a wide variety of super thin models, is orange/yellow in color and is a halogen-free UL94 flame retardant.

> *"Paper substrates have enjoyed some initial success due to their low cost, but this has been primarily limited to low-tech products due to the paper's high roughness, low resistance to temperature, flammability and absorbency."*

Conductive Inks

The second key element of the printed electronics equation is conductive ink. These unique inks sit atop the flexible substrate and supply the multiple layers of interconnects that power the printed circuits and devices. Although a simple layer, the market for conductive inks is large and growing with silver flake inks serving the largest and most mature markets. New, more exotic and higher performance ink formulations are also being introduced to the market that include silver and copper nanostructures along with graphene and carbon nanotubes that offer higher conductivity, inkjet printability, flexibility, and/or enhanced surface smoothness.

Polyimide Flexible Substrates

Printing directly on PI has always been a challenge due primarily to its poor ink wetting and adhesion properties. Corona treating is sometimes utilized on PI, but produces little in the way of success due to being highly variable and having any performance improvements tending to diminish with time. This is where polyimide films enter the equation.

Polyimide-based substrates take full advantage of PI's unique mechanical and electrical characteristics. These include ultra smooth surfaces for top coat adhesion and print resolution, dimensional stability over a wide range of temperatures, chemical resistance, high dielectric breakdown and high tensile strength. The substrates include a variety of printable top coats that allow conductive and semi conductive inks to be applied via flexo and screen printing techniques. Cross-linking the polymer top coats allows for greater long-term durability. In addition, PI substrates offer high performance-to-cost ratios and the combination of PI and a properly designed topcoat, allows the substrates to be REACH- and RoHS-compliant, halogen-free and UL94 flame-retardant.

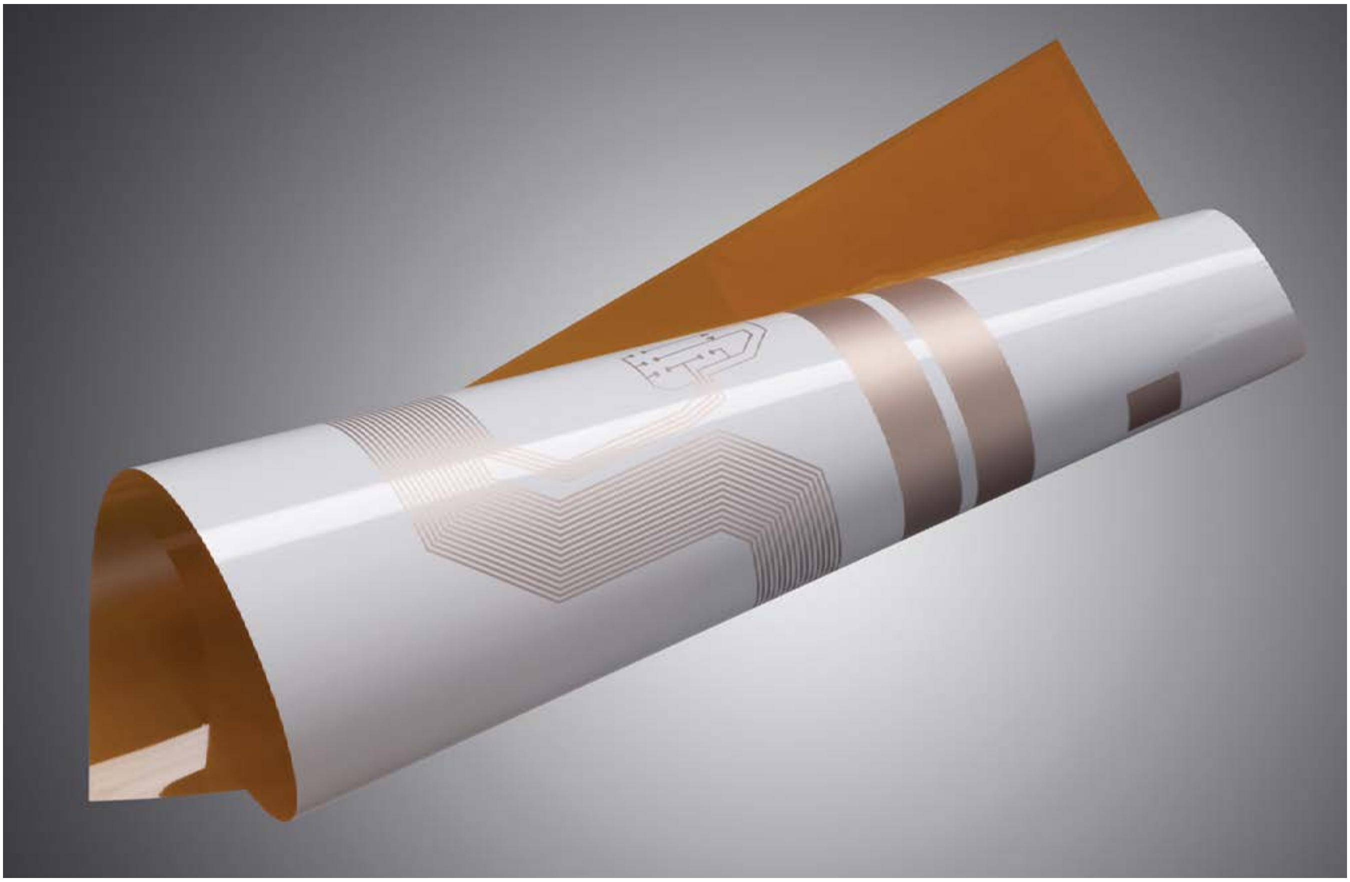

Figure 2: Polyonics flexible substrate, with high-gloss, high-resolution white top coat and printed electronics circuit.

Typical substrate applications include, among others:

- Electrical circuits
- Portable devices
- Antenna arrays
- Smart bandages
- Flex circuits
- Temperature sensors
- Flexible heaters
- Printed batteries

A wide variety of polyimide substrates is available, including 13, 25, 50 and 125 µm (0.5, 1, 2 and 5 mil) thick films with 3-4 µm (7-10 mils) white, clear, matte black or clear anti-static top coats. Harder top coats are also available that address the particular needs of high temperature laminations found in flex-circuit applications.

The Future

The world of printed electronics is moving fast and promises to transform nearly every type of electronic device into a modern ultra-thin, highly flexible and low-cost marvel in the near future. Much has already been done to pave the way for this exciting technology to change our lives. Still, more has to fall in place though to make the promise a reality with substrate technology continuing to play a major role in the ultimate success. **PCB**

Dave Genest is product manager at Polyonics, in New Hampshire. He may be contacted at tape.expert@polyonics.com, or 603-903-6327.

Selecting a Flexible Circuit Supplier

by Dave Becker
ALL FLEX FLEXIBLE CIRCUITS AND HEATERS

The selection of a flexible circuit supplier is a multidimensional decision. An Internet search produces a long list of suppliers capable of building a wide range of products. If you can believe what you read on the Internet, there are very few suppliers unable to support any technology (single-sided to 30+ layer rigid-flex) and volume (prototype to serial production). And if you believe everything you read on the Internet, call me directly, as my uncle in Nigeria has some money that he needs help transferring to a U.S. bank account.

Since all flex circuits are custom designed and manufactured, a more thorough review of a supplier's capabilities and specialties is critical for the specifics of an individual design. Everyone is not good at everything. Significant characteristics that help distinguish from among the myriad of flex circuit suppliers include the following.

Volume Capabilities

Most suppliers claim a wide range of volume capabilities, but what does "high volume" mean in this manufacturing world? Flex circuit suppliers build product using either a panel process or a continuous reel process. Reel-to-reel processing is used extensively to manufacture high volumes of cell phone, camera, and automotive applications. Most of these suppliers are located in Asia, but Multek Flexible Circuits remains a U.S.-based, high-volume supplier capable of competing with the cost pressures of these markets. Extensive reel-to-reel processing provides parts with little direct labor cost and the ability to produce in quantities exceeding millions of parts. Other flex circuit suppliers provide high-volume parts by acting as brokers (i.e., working with an overseas fabricator and

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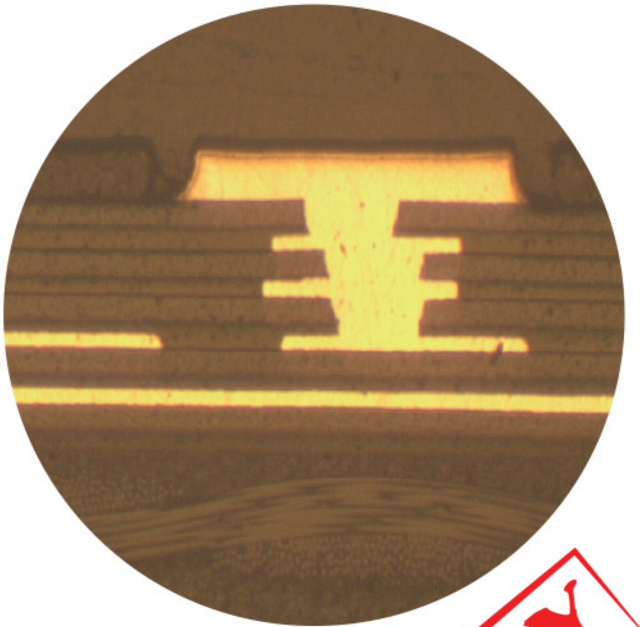

CASE STUDY

PWB REPORT: 5-n-5 Daisy Chain with 3mil Stacked Microvias Survives 1,000 IST Cycles

A printed circuit board with 5 layers of Zeta® glass-free dielectrics, built up on a core by Streamline Circuits, was cross-sectioned for IST testing at PWB lab - "Coupons very robust and no material degradation in capacitance measurements. Results were excellent. . ."

Zeta® films are 3-part dielectrics, including c-stage polyimide cast onto low profile copper with a proprietary high flow b-stage bonding film making it ideal for ultra thin HDI buildup technology. These dielectrics enable thicknesses down to only 12 microns.

Tom Doslak, Streamline's Director of Sales & Marketing, "Zeta's low Dk allows us to meet our same impedance requirements with thinner glass-free dielectrics. This thinness allows for smaller vias that are easier to drill, plate and stack due to Zeta's low 19ppm CTE. These benefits, as evidenced by this IST test, translate into very reliable structures that our customers need."

Streamline has been re-investing into their business by buying the latest state-of-the-art equipment to deliver the most cutting edge next generation HDI technology.

"Zeta is a great material that helps us get there," Doslak added.

To view the full PWB Report, go to integral-hdi.com or scan this Quick Response (QR) Code:

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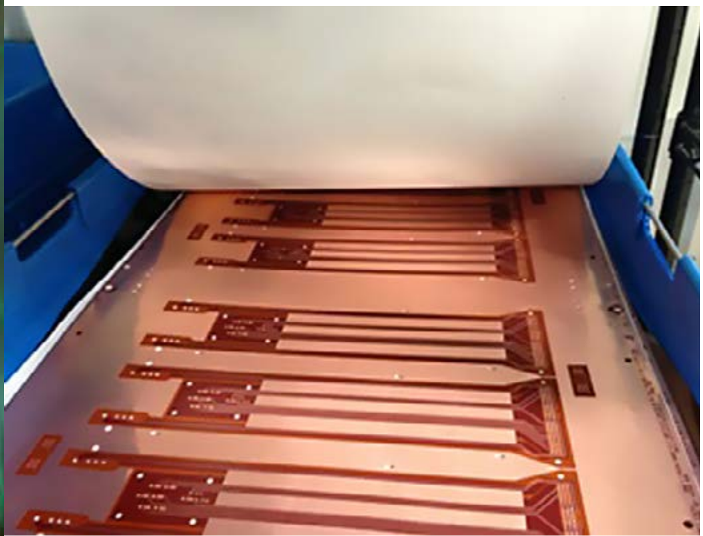


Figure 1: Flexible circuits in panel form, in process before coverlay.

acting as the middleman in the supply chain). As independent agents, these companies often take responsibility for product logistics, transit, quality, and provide domestic applications engineering support.

Panel processing is generally a lower-volume option; however, it does mimic the processing used by high-volume rigid PCB suppliers. Unit volume capacity is highly dependent on circuit size so capacity expressed in quantity of units can be misleading. A more meaningful measure is number of panels processed per day/week/month. Circuit board panel fabrication generally follows a sequential flow through multiple pieces of process equipment. Complex part numbers may require 40+ process steps as panel processes include chemical cleaning, imaging, developing, copper plating, etching, automated optical inspection, platen pressing, plasma cleaning and surface treatment finish, to mention a few. Actual capacity within a given factory is mostly driven by the number of panels possible through a piece of bottleneck equipment, so many shops manage their factory flow with a "theory of constraints" manufacturing philosophy.

Figure 2: Flexible circuits in panel form during automated optical inspection.

Vertical Integration

Building a flexible circuit is usually not the extent of a customer's requirements. Design and assembly services may also be required, and these are often provided by the flex circuit supplier. Under the umbrella of "design" is a wide range of services. Many flex circuit suppliers are able to provide a completed design (CAD files and drawing) if they are provided with a schematic or netlist and the mechanical outline. Reverse engineering a circuit from a sample part or photograph is also possible. One big advantage of having a design created by the fabrication shop is that DFM is an obvious upfront consideration. The opportunity to minimize and eliminate costs can be carefully considered when the design is embryonic. Fabrication yield is always a significant cost driver, so many suppliers “flexize” the artwork patterns to incorporate manufacturability and reliability features such as optimized line widths, enlarged copper via pads, filleted intersections between traces and pads, and rounded traces through curved circuit features. At a minimum, getting early input from a fabrication shop is highly recommended.

Many circuit shops have further integrated vertically by providing assembly services. Most flex circuit applications require some added value ranging from wire assembly and through-hole connector soldering to multiple components attached with automated SMT equipment. Most flex circuit suppliers offer some level of value-added assembly as their customer base continues to express a desire for a shorter supply chain. As products move into higher volumes and/or require more sophisticated assembly, contract manufacturers with these specialized capabilities look increasingly tempting.

HDI

With the constant pressure for miniaturization of electronic products, conductor traces and plated through-holes have become extremely small, with tight manufacturing tolerances. Conductor widths are often reduced to .003” or smaller, and .001” microvias formed with lasers are becoming more common. Specialized high-resolution imaging equipment and microvia formation capability are needed to produce these features. Equally important is process control over the multiple pieces of equipment (developing, etching, resist stripping, and plating) also used to build fine-featured circuits at a high yield.

Suppliers that build these products will generally require additional engineering support and more sophisticated equipment. In the U.S., these companies often support development projects for products that are eventually sourced overseas as volumes ramp. Another example of parts produced with this technology is hearing aid circuits, where pricing based on square inches of area is meaningless.

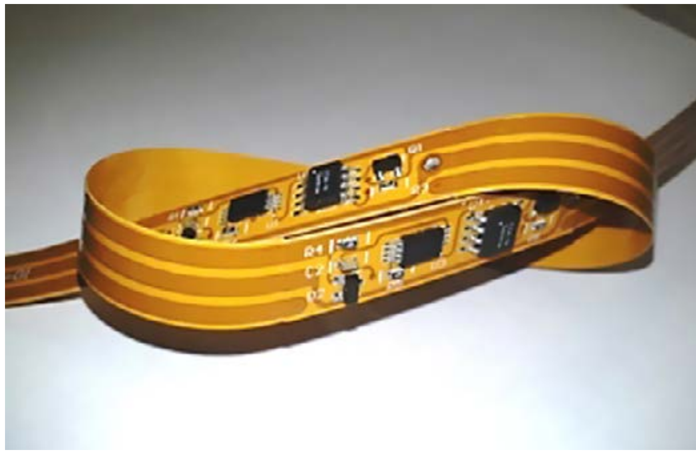


Figure 3: Many flex circuit shops integrate product miniaturization along with through-hole and SMT assembly services.

Quick-Turn Capability

Standard lead times for flex circuits vary considerably among fabricators, with a typical standard delivery offer of a few weeks. This can vary substantially depending on product complexity and may also be paced by the availability of components when assembly is included. Other flex makers specialize in producing parts with highly compressed cycle times and are able to deliver products with lead times of a few days. A portion of this market demand is supported by companies specifically focusing on quick-turn as a manufacturing niche. It is also true that most “standard delivery” suppliers reserve some portion of their capacity for expedited deliveries of low volumes at a premium price. Willingness to support a quick-turn request is often determined by the availability of factory capacity at a given time.

Certifications and Systems

Quality system certifications and registrations are requirements for some applications. The most common of these are:

ITAR

International Traffic in Arms Regulations is a set of U.S. government regulations controlling defense-related products. ITAR requires defense-related information to be controlled by U.S. citizens. Customers and suppliers can face fines if they provide non-U.S. citizens with access to information protected under an ITAR contract. A flex circuit supplier's registration with the U.S. Defense Trade Controls Compliance Division is required.

ISO 9001

The ISO 9000 family of standards is intended to ensure a certified quality management system is in place, and it is designed to help organizations ensure they meet the needs of customers and regulatory requirements related to their product. ISO 9000 deals with the fundamentals of quality management systems and details certification requirements. Third-party certification bodies provide independent confirmation companies are meeting ISO 9001 requirements.

AS 9100

AS9100 is another standardized quality management system, and in this case, specifically designed for the requirements of the aerospace industry. Aerospace manufacturers and suppliers worldwide require compliance and/or registration to AS9100 as a condition of doing business.

Mil-P-50884, MIL-PRF-31032, and IPC-6013

These quality assurance requirement documents are frequently specified by the government for military applications. The two military specifications require building coupons of generic product samples that are submitted to an independent lab for test and product qualification. This certifies that a supplier is eligible to bid on programs requiring these specifications. In addition, end-product quality requirements are defined with frequencies specified for some in-process tests. In an attempt to combine military and commercial program requirements, government and industry representatives have written and widely adopted IPC-6013. Many applications now specify the IPC document as a quality standard, with IPC Class 3 products defining quality requirements intended for high-reliability applications.

Summary

The products and capabilities offered by flex circuit suppliers vary considerably. Fortunately for the U.S. electronics industry, there is a good selection of domestic suppliers available…no need to schedule work in an Asian time zone or learn Mandarin. These criteria should help determine some of the questions to be asked when considering sourcing a new part number. The Internet can help as an initial filter, but you should then spend some time talking to applications engineers with a couple of potential suppliers. It does take a little due diligence, but matching the proper source with a new application will save headaches in the future. **PCB**

Dave Becker is vice president of sales and marketing at All Flex Flexible Circuits and Heaters.

Key Surface Properties of Complex Oxide Films

Better batteries, catalysts, electronic information storage and processing devices are among the benefits of a discovery made by Oak Ridge National Laboratory scientists.

The findings, published in Nanoscale, showed that key surface properties of complex oxide films are unaffected by reduced levels of oxygen during fabrication—with implications for the design of functional complex oxides used in a variety of consumer products, said Zheng Gai, a member of DOE's Center for Nanoscale Materials Sciences at ORNL.

"With these materials being a promising alternative to silicon or graphene in electronic devices, the ever-decreasing size of such components makes their surface properties increasingly important to understand and control," Gai said.

Electroless Copper and D-Sep

by Michael Carano
OMG ELECTRONIC CHEMICALS

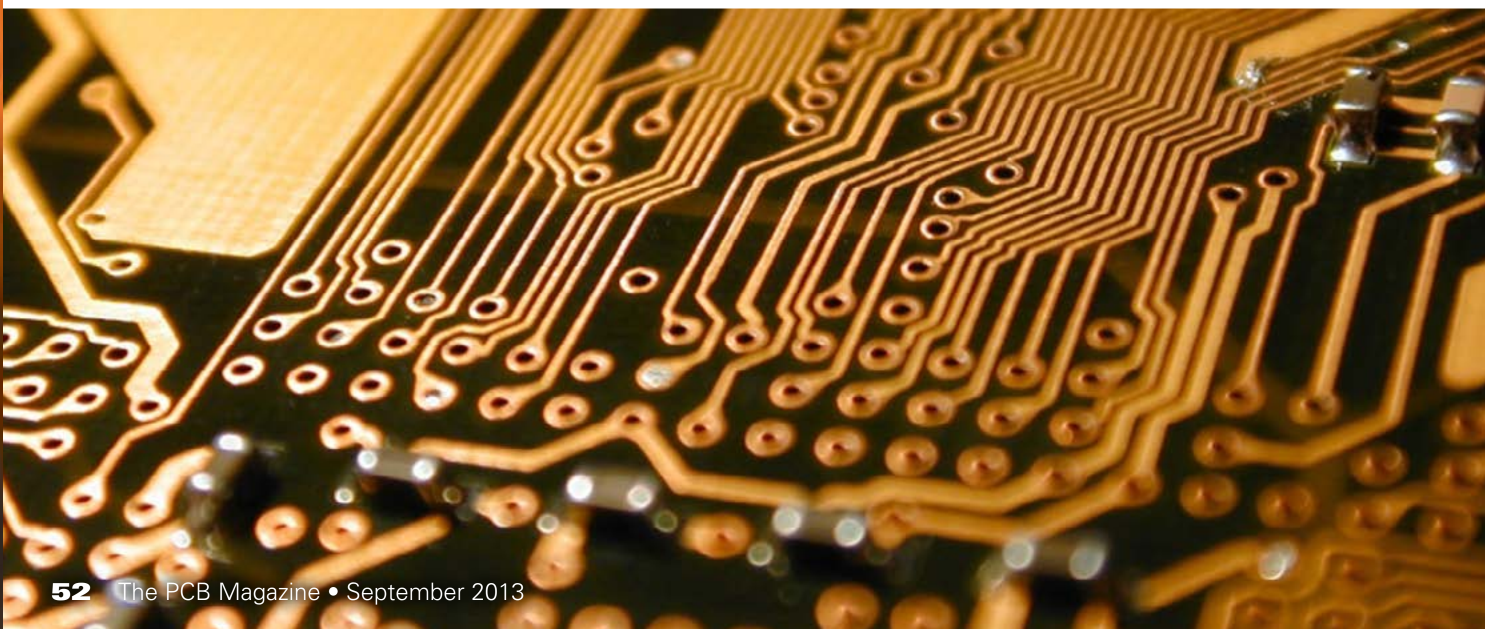
In past columns, I presented information about the different types of ICD interconnect defect and its root causes. One key defect that was not discussed was the infamous D-sep. What exactly is D-sep? We will explore this issue and provide several suggestions for process improvement so that you don't experience D-sep on your expensive, high-reliability printed circuit boards.

Description of the Defect

First, D-sep (Figure 1) is a separation of the electroless copper deposit from the post interconnect. Okay, you say! But isn't that a definition of an ICD? In a way, yes. However, D-sep occurs without a thermal excursion. Let's list a few other considerations when discussing D-sep:

Figure 1: Example of D-sep.

- An interconnect separation without any thermal stress
- Stress in the electroless causes it to separate from the interconnect forming a D shape
- Separation can cover the width of the interlayer or it can cover only a small part of it
- Occurs most on 1 oz. layers
- Occurs more often in center of hole
- Generally occurs more in center of the plating rack (basket)
- If all other factors are kept constant in the desmear and electroless line, panels with positive etch back may have D-sep when normal desmear will not



D-Sep: What are the Causes?

There are a number of factors that can lead to D-sep. The major factors relate to the electroless copper plating solution itself. Generally, these issues arise due to the lack of proper control and vigilance of the process. So the causes are related to an interruption or delay in the electroless deposition, with the following major factors contributing:

Major factors

- low caustic level (depleting the caustic stops the plating reaction)
- high specific gravity (by-product components are produced that have an inhibiting effect on the chemical plating, most notably, sodium sulfate and sodium formate)
- vibration
  - vibration removes air bubbles that may be trapped in the hole as it enters the tank
  - hydrogen gas is produced during the reaction and needs to be removed from the holes
- temperature of electroless (higher temperature increases the plating rate; if solution is not transferred fast enough, the reaction stops)

There are always concerns about the actual deposition rate of the copper plating process. The more active the electroless copper plating solution, the faster the overall deposition rate. My own studies have shown that faster dep rates tend to lead toward highly stressed copper deposits. The end result: The copper deposit tries to pull away from the surface, whether the surface is the copper interconnect or the hole wall. Figure 3 below shows a process effects diagram of the relationship between the operating temperature and the caustic (NaOH) content in the electroless copper plating solution. The colder colors (blue and light blue) indicate that at those process parameters there is little to no tendency for D-sep. Again, these results were confirmed with countless design of experiments and actual practice in the operating PCB manufacturing environment.

Figure 2: Partial D-sep.

One may ask what influence the caustic concentration has on the issue of D-sep. Again, internal studies have provided insight to the influence of the caustic soda (sodium hydroxide) and the deposit stress of the plated copper. Now, while this is an oversimplification (as other factors such as stabilizers and rate-controlling additives play a role), the NaOH with all other factors held constant does indeed influence the occurrence of the D-sep defect.

Figure 4 shows the relationship between the sodium hydroxide content and operating temperature on the deposition rate of the copper. It should be easy to correlate the results in Figures 3 and 4 to discern the relationship of these parameters and the influence on the D-sep defect.

There are several minor factors that contribute to D-sep and these are listed below.

Minor factors

- rack agitation
- solution movement
- hole size and board thickness
- desmear, etch back
- rinses (cleanliness of the rinses; pH of the rinse prior to electroless copper; temperature of the rinse)
- micro-etch

Let's discuss the importance of the micro-etch. There is a correlation between the quality of the etch topography on the interconnect and

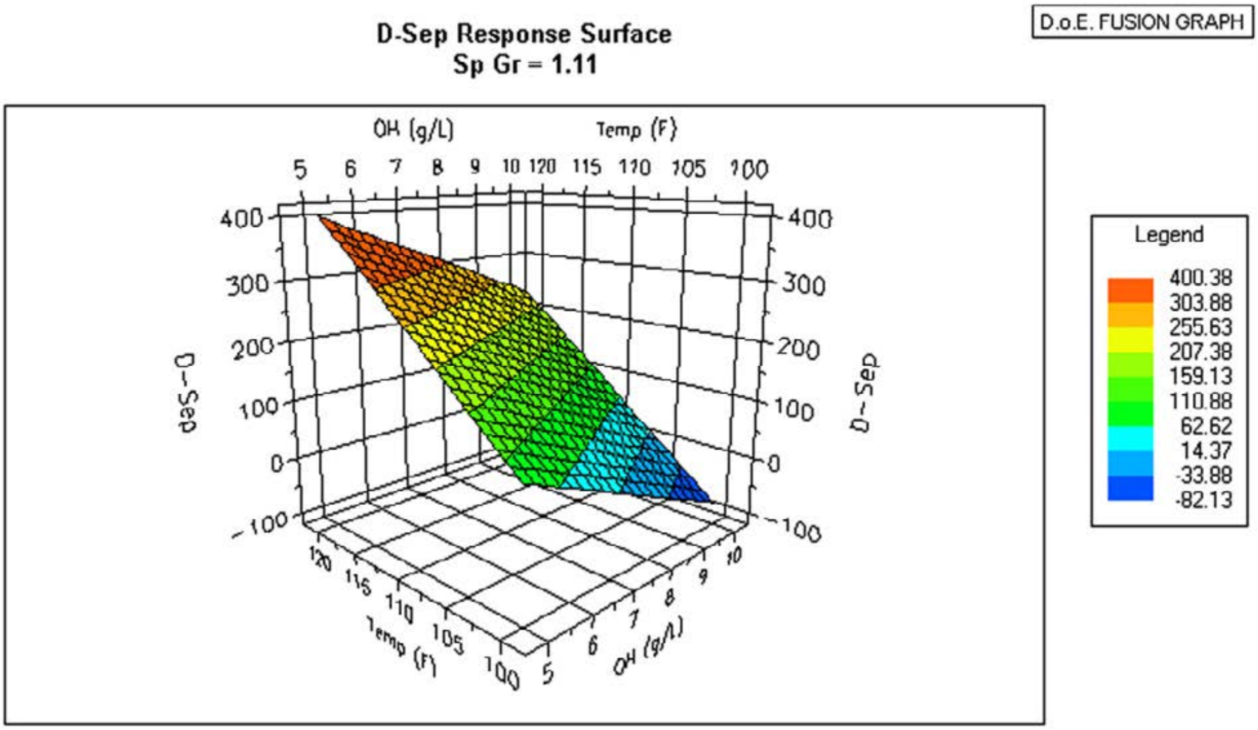


Figure 3: D-sep response curves relationship between caustic content and the operating temperature of the electroless copper solution (note: blue and light blue areas denote more desirable outcomes).

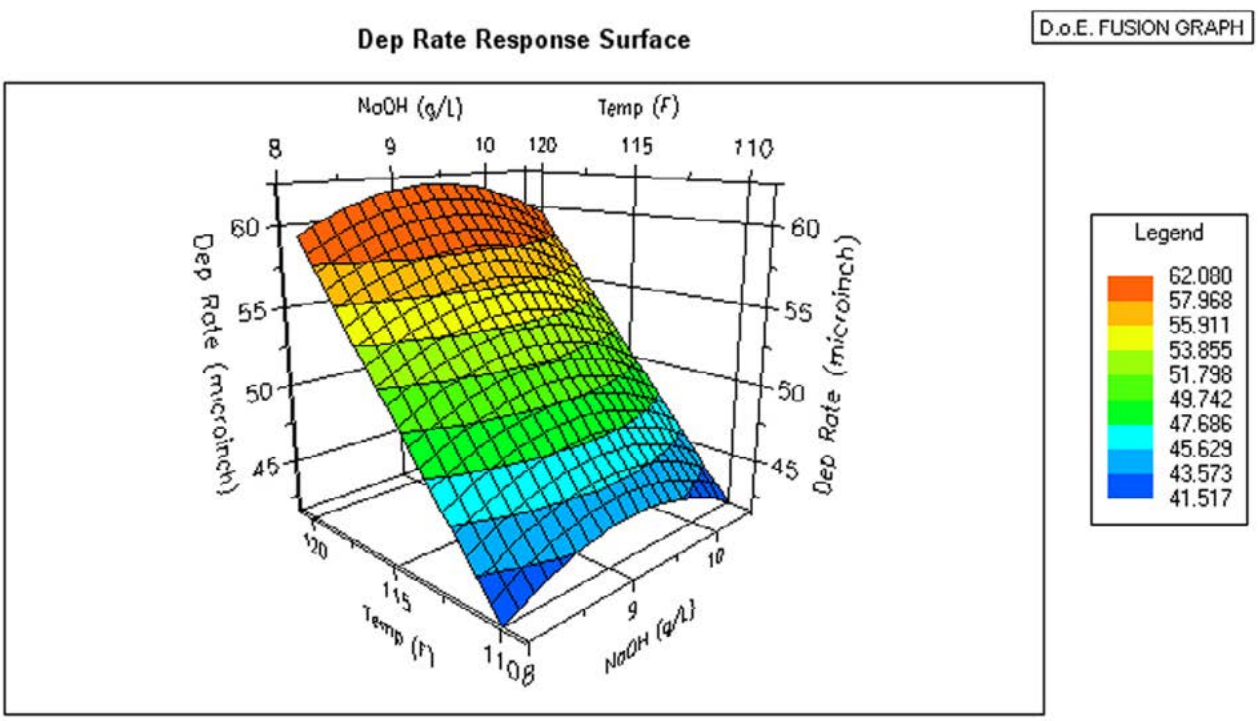


Figure 4: Effect of caustic and temperature on deposition rate (note: blue and light blue areas denote more desirable outcomes).

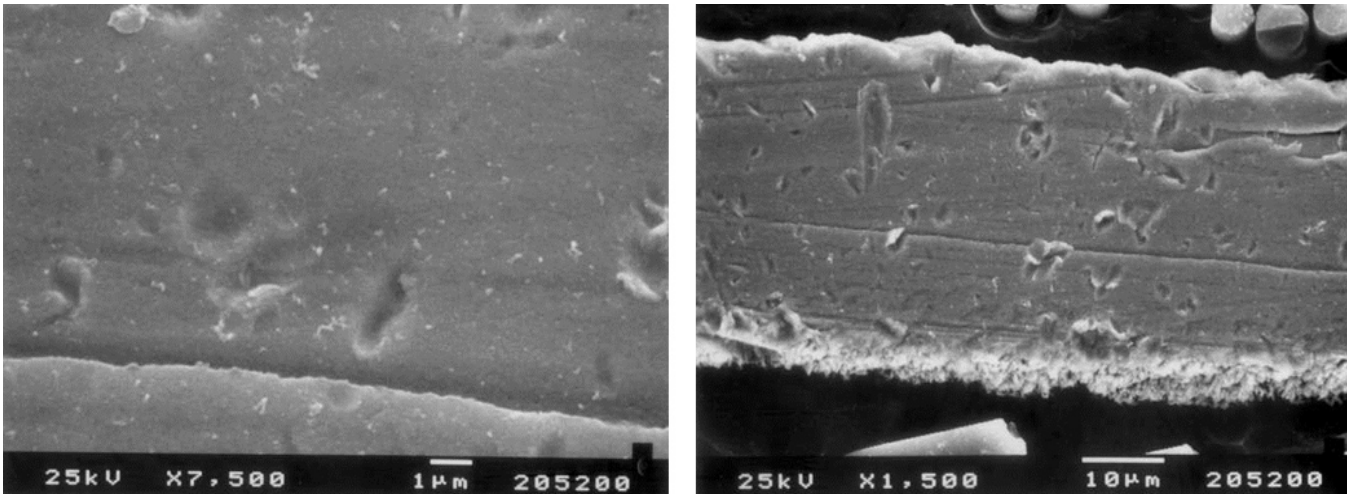


Figure 5: View of copper interconnect after mild micro-etch. Note the somewhat smooth topography.

the ability to resist D-sep. A close look at Figures 5 and 6 tell the tale of this author's recommendation.

D-Sep: How to Prevent it?

- If D-sep occurs raise the caustic level to 9.5 g/L
- Lower the temperature if possible
- Reduce the specific gravity of the bath
- Increase the ability of solution to flow through the holes
  - – increase vibration
  - – increase solution movement
  - – ensure proper rack agitation
  - – open up spacing between boards
- Other options that will help
  - – increase rinsing to clean the holes
  - – raise temperature of the rinse water
  - – increase the pH of the rinse before the electroless
  - – ensure that desmear is giving a clean hole and not dragging any chemistry down the line

Again, there is no shortcut to a good solid understanding of the process fundamentals. This includes mechanical as well as chemical parameters. **PCB**

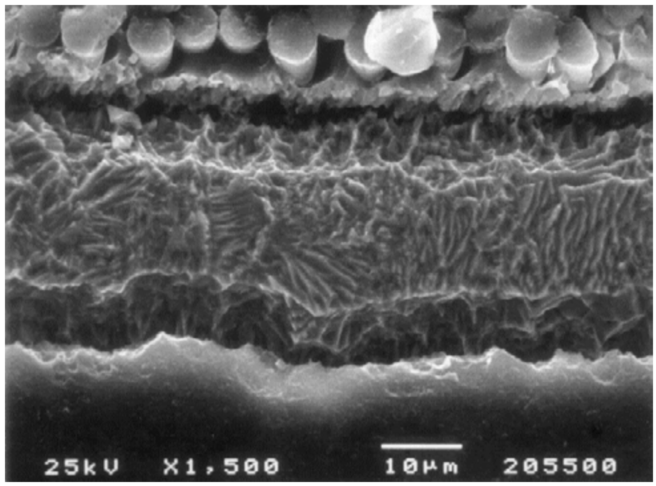
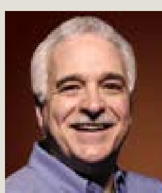


Figure 6: Properly etched interconnect. Note rough topography that will enhance the adhesion of the electroless copper to the post and minimize D-sep.



Michael Carano is with OMG Electronic Chemicals, a developer and provider of processes and materials for the electronics industry supply chain. To read past columns, or to contact the author, click here.

2013 MEPTEC MEDICAL TECHNOLOGY CONFERENCE

Global Momentum in the Medical Industry – Convergence of Electronics, Biology and Health

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MANY FACTORS HAVE contributed to global momentum in the medical electronics industry, with the convergence of electronics technology and biological health sciences playing a major role. Growth in medical electronic applications (yes, there is an App for that!) will parallel Cell Phone and Tablet PC markets, with increases in computing power as well as optical resolution and touch sensor technologies. Current focus for mobile, implantable and large medical systems is on improved personal health, with preventative applications and advanced early diagnostics. Various integrated circuit (IC) technologies, now complemented by MEMS bio-sensor technologies, allowed for significant development in areas such as prosthetics, combining “artificial limbs” with “artificial intelligence”, sensing and reacting to very small electrical impulses from the brain, through direct body contact.

This conference will address the many industry challenges and opportunities including safety, reliability, miniaturization, manufacturing and materials as well as government regulations and political healthcare initiatives. The human body is a convergence of various biological phenomena and sophisticated electrical networks controlled by the brain, with the health sciences and medical electronics technologies converging to meet strong global demand. ◆

OLD MAIN on the ASU Tempe Campus, constructed before Arizona achieved statehood, will host the 8th Annual MEPTEC Medical Electronics Conference.

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- Safety and reliability of medical devices
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- Bonding techniques of new wire alloys for medical electronics
- Wafer Level Packaging and TSV for biomedical applications
- MEMS & Sensors for Medical Applications
- Security and psychological issues in medical devices
- Miniaturized electronic packaging for wearable health monitors
- Wireless communication/solid state batteries in miniature implantable medical devices
- Designing more reliable medical products
- “Fantastic Voyage” meets medical device design

KEYNOTES

Sam Bierstock, M.D.

Day One Keynote

MEMS Technology and the Healthcare Industry: The Convergence of Timelines and the Perfect Storm

Sam Bierstock, M.D., BSEE
Physician, Electrical Engineer, Medical Informaticist, Founder of Champions in Healthcare

Dr. Bierstock is a nationally recognized authority on healthcare and healthcare information technology. He is the Recipient of the George Washington Honor Medal, Freedoms Foundation for his work on behalf of our nation’s veterans. ◆

Karthik Vasanth, Ph.D.

Day Two Keynote

Creating Solutions for Health Through Technology Innovation

Karthik Vasanth, Ph.D.
General Manager, Medical and High Reliability Business Unit
Texas Instruments

Karthik Vasanth received his Ph.D degree in Electrical Engineering from Princeton University in 1995. He joined the Silicon Technology Development group at Texas Instruments in 1995. In 2010 he became the General Manager of the Medical and High Reliability Business Unit at TI. ◆

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PCB007 Market News Highlights

Global Smart Grid Technology to Grow $220B by 2020

With the smart grid core and enabled technology market expected to grow to $220 B by 2020, it's no secret that the smart grid is seen by many utilities around the globe as the ticket to addressing the escalating demand for reliable power, renewable energy integration, and greater energy-efficiency.

Global Mobile Phone Market Up 6% in Q2

The worldwide mobile phone market grew 6.0% YoY in 2Q13. According to the International Data Corporation (IDC) Worldwide Quarterly Mobile Phone Tracker, vendors shipped a total of 432.1 million mobile phones in 2Q13 compared to 407.7 million units in 2Q12.

Global Semiconductor Industry to Reach $394 Billion In 2017

The recently released Global Semiconductor Industry 2012-2017: Trend, Profit, and Forecast Analysis report states that global macroeconomic developments and technological advances, personal computers, and memory markets are expected to drive demand over the forecast period.

Market & Technology Drivers to Bring 3D-IC to Production

With semiconductor technology moving toward systematic integration of stacked heterogeneous chips and 3D-IC, the latest developments will be featured at 3D-IC & Substrate Pavilion and Advanced Packaging Technology Symposium at SEMICON Taiwan 2013 and the SiP Global Summit 2013.

3D Scanning Market to Reach $4.08 Billion by 2018

The global 3D scanning market is forecast to grow from an estimated $2.06 billion in 2013 to $4.08 billion by 2018, at an estimated CAGR of 14.6% from 2013–2018. Recent industry trends show the technology is continually improving—right along with demand.

Tablets Shipments Soar in Q2; Up 43% YoY

More than 34 million tablets shipped in Q213, a 43% year-on-year increase. Tablets now account for 31% of worldwide PC shipments. But Apple's performance faltered. Its tablet shipments declined 14% on Q212 and its market share dropped to 43%.

Key Raw Material Demand to Double as LED Market Booms

Global demand for precursor, a material used in manufacturing of light-emitting diodes (LEDs), is set to more than double from 2012–2016, as the market for LED lighting booms, according to a new report entitled "Precursor for LED MOCVD–Market and Industry Analysis," from Displaybank.

Global Semiconductor Revenue to Rise 6.9% in 2013

The SAF also forecasts that semiconductor revenues will grow 2.9% YoY in 2014 to $329 billion and log a CAGR of 4.2% from 2012–2017, reaching $366 billion in 2017.

U.S. to Witness Uptick in Economy in 2014

The U.S. economy is in for another year of sluggish growth in 2013, but a rebound in the housing market is expected to lead to stronger gains next year, according to The Conference Board of Canada's U.S. Outlook, Summer 2013.

Small Cells Market: To Rise 125% in 2014

In ABI Research's latest forecast, overall enterprise and consumer Femtocell shipments will reach 5.7 million units in 2014 compared to 3.8 million units in 2013. While 3G indoor small cells will continue to represent the vast majority of shipments, it is LTE indoor small cells which are expected to ramp up significantly this year.

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Look to Rogers Corporation not only for PCB materials with high-ε_r values, but for circuit materials with the widest range of ε_r values in the industry. Rogers' PCB materials provide circuit designers with true flexibility, not just for the electrical performance they seek, but to achieve it in the smallest-sized circuits possible.

Product	ε_r	Df @ 2.5GHz
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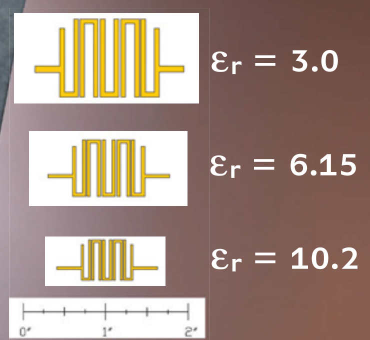
RO3006™	6.15	0.0018
RO3010™	10.2	0.0020

If it's a circuit that has to be smaller, make sure it is also better, with Rogers!



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Temporary Process Change

by Steve Williams

Change is Good

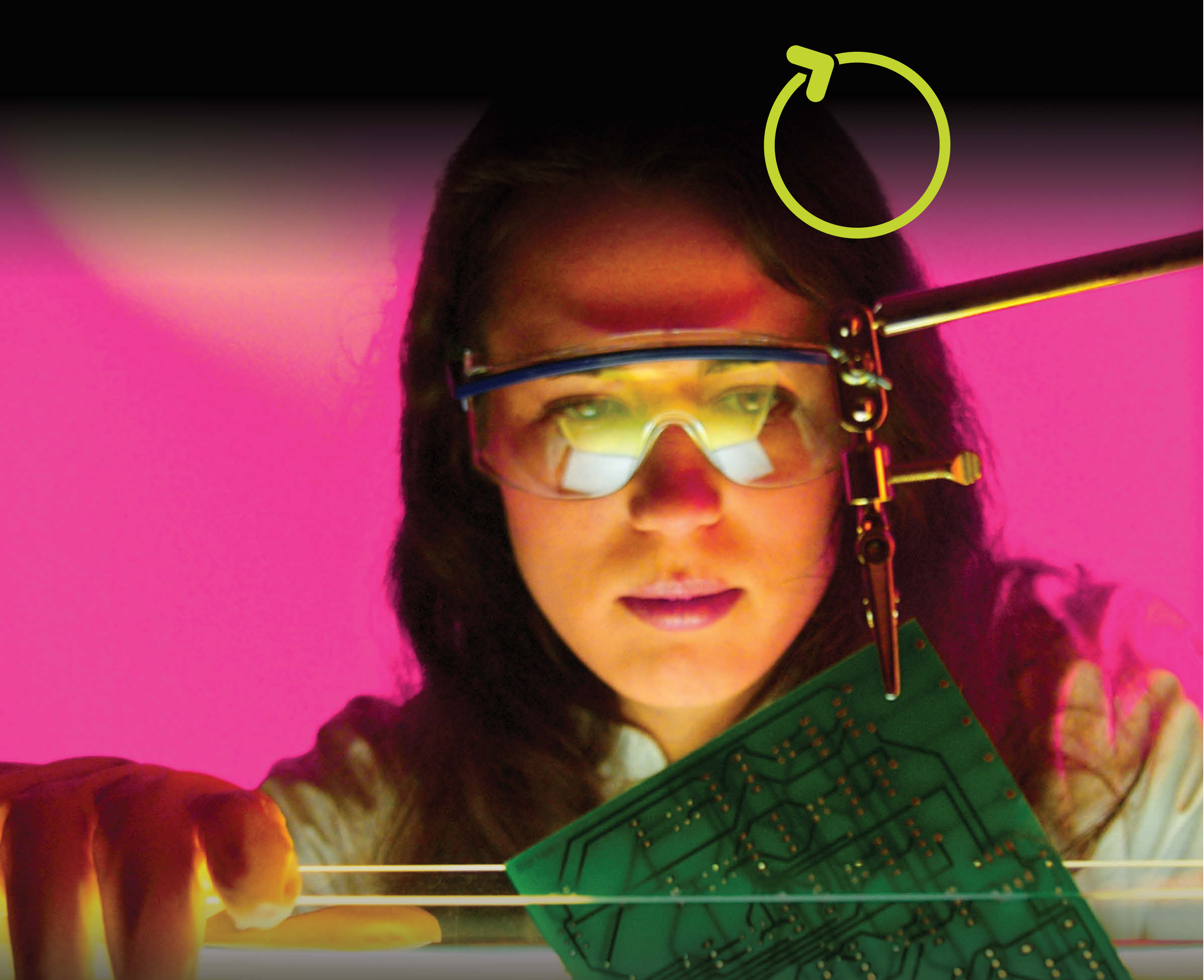
Change is a given. While this adage may be quite true and normally a good thing, it can cause havoc in the documentation system of a printed circuit operation. To be successful, there must be a formal methodology to handle process change.

Without change, improvement stagnates and complacency sets in. Change is good, but the operative word is controlled change relative to the complex processes involved in producing a PCB. Many companies implement change on the fly, without any formal evaluation or approval process in place. This tends to not only be ineffective, but also to guarantee a finding with any customer or ISO auditor. The key to successfully navigating procedural change is to develop a robust temporary process change (TPC) program.

Process Overview

When crafting the program, the first thing to flesh out is the function that will serve as the watchdog of the system, which is the first mission-critical aspect of a TPC program. Creativity must certainly be fostered, while at the same time guarding against changes that could have a detrimental effect on the process. Redundant TPCs must also be avoided as there is no need to expend resources on a method that has been proven unsuccessful in the past. I would make a strong argument for process engineering to manage the system, but each shop is different; however, my only caveat would be to have a single entity overseeing the process. I would also highly recommend making this a standalone procedure/work instruction.

There are three main components of a solid system, the TPC form, the TPC log, and the



quality assessment phase. My position affords me the unique opportunity to evaluate the best and brightest in the manufacturing world, but on the other hand I also get to observe the opposite end of the evolutionary scale: the worst of the worst. It continues to amaze me, ISO notwithstanding, how many times I run across controlled procedures that have items crossed

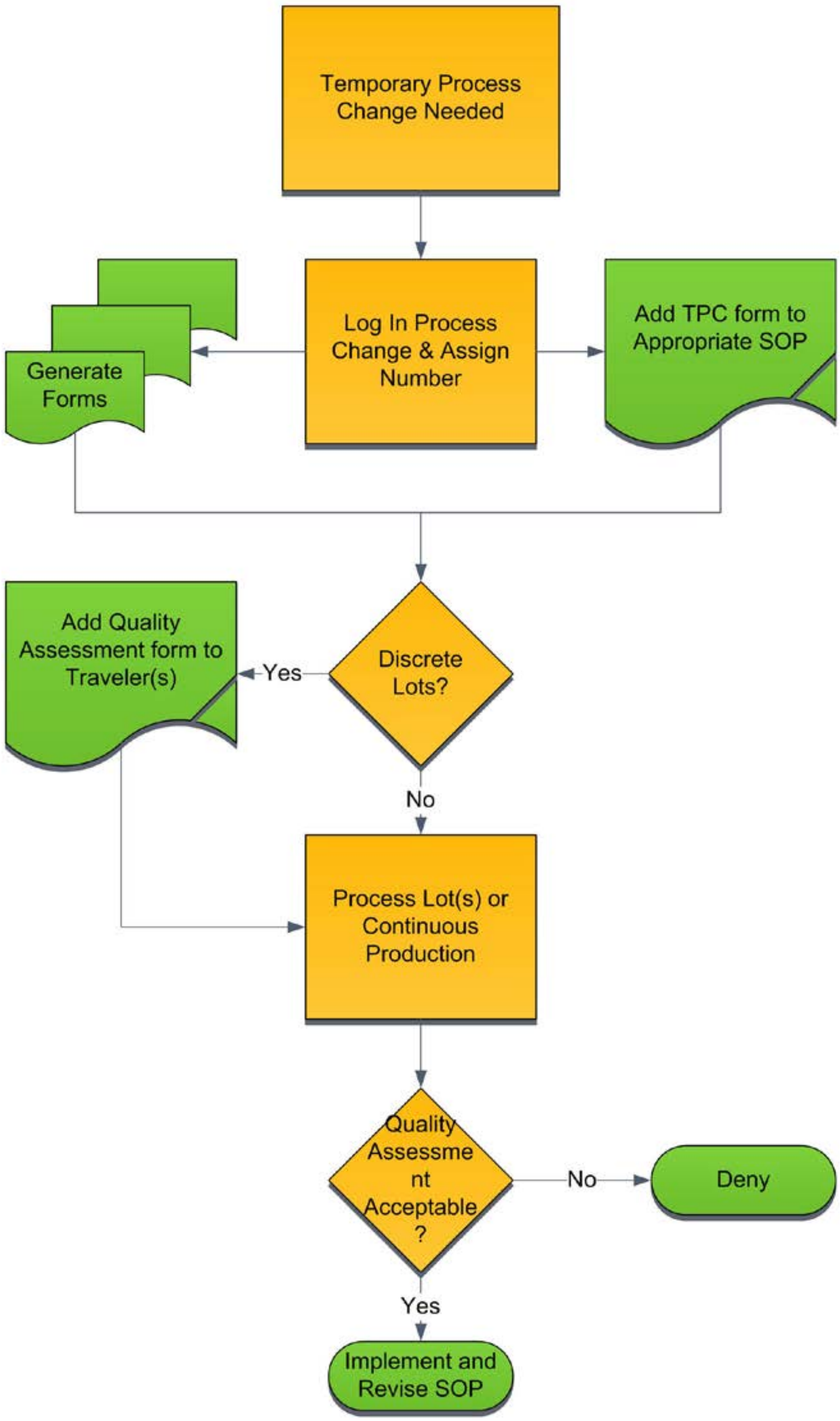


Figure 1: Flow for a TPC flow program.

off and handwritten changes. A few companies have even accounted for this by including in their document control procedure that handwritten changes are allowed! Although this loophole may satisfy a first-year ISO auditor, this violation would banish a company to the "not ready for prime-time" file in my book. Figure 1 details the process flow for a TPC program.

TPC Form

A simple electronic or paper form should be developed that provides the basic information needed to implement and track the change. It should include sections that describe the change, any chemical changes, the reason for the change, and the results ("implemented" or "denied"). A TPC can be defined as any process change that deviates from a standard operating procedure (SOP) for a short period of time. The change could be related to procedures, raw material, or suppliers/brands, and the "short period of time" must be defined. Anyone should be allowed to submit a TPC for review and approval; however, utilizing the organization's various improvement teams for this activity increases buy-in and can be an effective screen for unworthy ideas. If the change is global for the process, it should be attached to the appropriate procedure (either paper or electronic). If the change is limited to a specific lot(s), it should be attached to the appropriate process traveler(s). In either case, all appropriate operators should be notified of the change, again improvement teams are a perfect media for this communication.

TPC Log

A method for managing the TPCs needs to be developed, and a simple spreadsheet log is the most effective (also a controlled document). Building a level of intelligence into the TPC numbering system (such as embedding the procedure or department number) will allow historical analysis of successful and unsuccessful TPCs for any process.

Quality Assessment Phase

The second mission-critical aspect of a TPC program is the quality assessment phase, where a decision will be made to either permanently incorporate the change into the process or deny it. This decision needs to have the cross-functional approval from the department/improvement team, engineering and quality, at a minimum. This decision needs to be documented (form) and as data-driven as possible (i.e., yield & rework, material/labor cost reductions, etc.) over the TPC period. If a discrete lot(s) is being evaluated, the quality assessment form can be attached to the process traveler(s) to gather the appropriate data as mentioned above. Global TPCs affecting continuous production will require a systemic tracking method over the course of the time period.

Closure

This should be easily accomplished, but getting to the decision point is where many often stumble. As mentioned earlier, setting a defined time frame for the TPC evaluation is critical. In most cases, 30, 60, or 90 days are sufficient to execute a meaningful evaluation of a process change. It is a strongly recommended practice to close out as many of the open TPCs as possible prior to a major customer or ISO surveillance audit. Closure also means revising the appropriate SOP to include any successful TPCs. Don't be concerned with having a history of frequent TPCs, if the quality system is operating correctly this activity should be encouraged. In the quest for continuous improvement, change is good.

I'll end this column with a quote about change that seems appropriate in the volatile world of PCB manufacturing. I borrowed it for the title of my first book from my good friend and quality guru, W. Edwards Deming: "It is not necessary to change. Survival is not mandatory." **PCB**

Steven Williams is the commodity manager for a large global EMS provider, and author of the book [Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean](). To read past columns, or to contact the Williams, [click here]().

NEWS

Mil/Aero007 News Highlights

PCB Sales to Mil/Aero Market Remains Positive

Despite cutbacks in the U.S. military budget, cumulative rigid PCB sales to the military market from January through May this year were up 3.4% compared to the same period in 2012, while rigid PCB sales to other markets were down 9.1% year-to-date.

IPC DVD Helps Industry Understand Conflict Minerals Regs

"The proceedings DVD gives those who could not attend the summer conflict minerals conference the opportunity to benefit from the knowledge shared by industry experts and the experiences of those in the trenches…" said Fern Abrams, director of government relations and environmental policy.

Endicott Interconnect Secures Re-certifications

Endicott Interconnect Technologies, Inc. recently announced the completion and passing of several critical re-certifications including AS/EN/JISQ9100:2009—Revision C, ISO 9001:2008, and ISO 13485:2003.

Micropack Achieves AS9100 ANAB Accreditation

"Micropack Limited has always focused on meeting the stringent challenges of the industry and AS9100 certification is a major step in our endeavor to achieve excellence and to meet the exacting demands of the aerospace and defence industries. Nadcap certification is next in our road map," said CEO Sreekar Reedy.

Invotec Develops PCBs for European Comm Satellite

Invotec Group took a keen interest in the launch of Inmarsat's latest satellite, Alphasat, in July. The most sophisticated commercial communications satellite ever launched, Alphasat features an advanced digital integrated processor system built by Astrium in the UK and incorporating PCBs manufactured by Invotec Group.

SOMACIS Earns Nadcap Merit Status for Electronics

The company has been awarded Nadcap Merit status for Electronics at its Italian facilities, covering rigid and HDI PCBs. The very first European PCB manufacturer to achieve the Nadcap accreditation, SOMACIS has held the accreditation since 2005.

Multilayer Technology Earns AS9100C Re-certification

The company has announced completion of and passing the AS9100C re-certification audits. The re-certification consisted of three full days of intense auditing of all departments by a registrar. This audit marks the three-year anniversary that the company has achieved and maintained this certification.

Park Electrochemical Unveils Very Low-Loss RF Material

Park Electrochemical's NL9000 RF/microwave electronics materials products feature very low-loss, high-frequency transmission and exceptional antenna gain and directivity performance.

HEI Q2 Sales Up 35%

"Our Victoria operation continues to grow with the large contracts relating to the military radio systems and other customer demand. We are also seeing operational improvements in the Victoria and Tempe plants with better flow and improving yields," said HEI CEO, Mark B. Thomas.

Rogers Introduces Improved Antenna Grade Laminates

The company's Advanced Circuit Materials Division introduced improved high-frequency materials to address several market needs. The RO4700JXR Series antenna-grade laminates were designed for use in base station, RFID, and other antenna designs and combine low-loss dielectric with low-profile copper foil for reduced passive intermodulation (PIM) and low insertion loss.

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The 5 Whys: It's a DAM problem!

by Gray McQuarrie
Grayrock & Associates

What we observe is not nature itself, but nature exposed to our method of questioning.
—Werner Heisenberg

This month, we'll focus on "what" based questions: how they reveal solutions to problems faster and better than "why" based questions.

The 5 whys are a tool that has been adopted by Six Sigma and Lean, and comes from Taiichi Ohno, the pioneer of the Toyota Production System. Even though this technique is highly regarded, it's a tool I rarely see used in practice, and for me, it just doesn't work as promised. What the 5 whys are supposed to do is find the root cause to any problem quickly. The example Ohno uses goes like this:

Q1: Why did the robot stop?
A1: The circuit was overloaded, causing a fuse to blow.

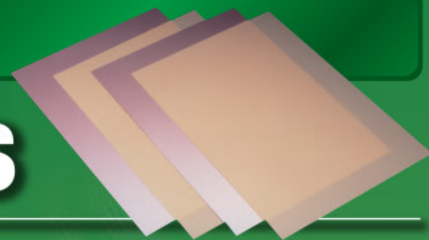
Q2: Why is the circuit overloaded?
A2: There was insufficient lubrication on the bearings, so they locked up.

Q3: Why was there insufficient lubrication of the bearings?
A3: The oil pump on the robot is not circulating sufficient oil.

Q4: Why is the pump not circulating sufficient oil?
A4: The pump intake is clogged with metal shavings.

Q5: Why is the intake clogged with metal shavings?
A5: Because there is no filter on the pump.

In this example, the 5 whys appear to work perfectly. Part of the reason is the person answering these questions has a perfect under-



standing of the robot. If you take a moment and think through this example you will start to see an immediate problem. For example, if you had a perfect understanding of the machine, why wouldn't there be a filter on the pump to begin with? Where did the metal shavings come from? Are the gears and other metal rubbing together inside the robot and wearing themselves out unexpectedly because of a poor design? Does this mean that in a matter of months all of these robots will require a very expensive overhaul? Are we kidding ourselves that the small filter will solve our problem when there are much more serious issues with the robots and their design to consider?

What if we have a very limited understanding of our problem? Will the 5 whys help? For example, let's say you have too much wicking in a drilled hole. Here is how the 5 whys might play out:

Q1: Why is the wicking excessive?

A1(a): Because the glass bundles have been damaged so much that there are microscopic pathways for plating chemistries to be absorbed through capillary action.

A1(b): Because there was poor impregnation of the resin system to the glass creating microscopic canals that were never filled with resin. This provides a wicking path for plating chemistries.

A1(c): Because the material was left too long in the plating tank, where chemical materials absorbed to their maximum within the material.

And so it goes with multiple answers. Are any of these answers right?

Let me put this multiple answer scenario in mathematical terms. Let's say for each why question (e.g., "why did this happen?") there are at least four possible answers. Therefore, for each of these four answers there would be the second round of why questions (or second level) that would each generate four possible answers. This would mean there are 16 questions to ask for the third why (third level), producing 64 answers. By the time we reach the 5th level the expectation is we will unearth the true root cause. What we wind up with instead is 256 questions and 1,024 possible answers! This type of geometric progression, discussed in What is the DAM Problem with Scheduling? (The PCB Magazine, July 2013), is why these types of problems are called NP Hard or Complex problems. The reality is, the less we know about what happened, the more the 5 whys will make finding a solution within our lifetime hopeless. It seems in order for these why questions to work, we have to start off with a pretty good understanding of our problem.

> ***"The reality is, the less we know about what happened, the more the 5 whys will make finding a solution within our lifetime hopeless. It seems in order for these why questions to work, we have to start off with a pretty good understanding of our problem."***

There is something even worse to consider with the 5 whys. What is the probability of being right if there is only one right answer at each level? If you are just guessing, then the probability of being right at the first level is 25%. The probability of being right at the second level is 6.3%. The probability of being right at the third level is 1.5%. The probability of being right at the fourth level is 0.4%. And for the fifth level the probability of being right is 0.097%. In order to compute the probability of being right at all five levels so that you find the one true root cause you must multiply all of these probabilities together, resulting in a 0.00000009165% chance of being right!

Some of you may object to the whole way I went about this argument, and you insist on using the 5 whys anyway. Consider the following video in which Nobel Prize winning physicist Richard Feynman is asked, "Why do two magnets held in a particular way repel each other?" He answers that a "why" question is predetermined by our existing understanding of nature and our bias of how we think things work. For example, how would you respond to an alien who asks, "Why can't you pass your hand through a rock?" As absurd as this question appears, it is a fact that matter is mostly pure empty space, as explained quickly and efficiently in this short video.

You see, only if you have a really solid understanding of the theory of quantum mechanics and electrical forces can you have any hope of explaining your answer. Does not knowing why we can't pass our hand through a rock cause any problems for us? Would knowing why help us? Perhaps understanding why isn't as important as we think. And the reality, for even the simplest things such as being able to pick up a rock that is 99.99% empty space and throw it and watch it fall, we don't understand why. What is amazing is that if you ask why this is so, 99% of people will not admit that they don't know why? Why is that?

There is a psychological side to asking why. For example, you come home from work and your significant other isn't happy. Fresh from your Six Sigma or Lean training you decide to try the 5 whys in order to discover the true root cause to your partners unhappiness so you can fix it: "Honey, why are you so annoyed?" There are several possible answers you would likely receive back such as: "Why are you such a pompous jerk?" The problem with a why question is it puts us on psychological defense, because we feel instinctively attacked or cornered. We either attack back or subvert the line of inquiry so that it comes to a halt. And when we feel attacked, our brain is no longer thinking. Our fight-or-flight emotions kick into overdrive.

"The problem with a why question is it puts us on psychological defense, because we feel instinctively attacked or cornered. We either attack back or subvert the line of inquiry so that it comes to a halt. And when we feel attacked, our brain is no longer thinking."

Where Do We Go From Why? What!

What is the alternative to the 5 whys? "What-based" questions that have no hint of prejudicial judgment or bias. For example, when a police officer arrives at an accident scene, he asks, "What happened?" Then he gets his pen out and start listening and writing. What does that activity of taking notes do? It causes us to talk more, because we feel significant and important. We are receiving attention. We aren't being judged. And we feel safe. Could you imagine what would happen if the police officer went up to a driver involved and asked, "Why did you smash into that other car?" Or ask a witness, "Why did this crash happen?" instead of, "What did you see?"

In my column, The Reliability Mindset (*The PCB Magazine,* June 2012), I suggest these four questions when something goes wrong, such as scrap material, a machine breaks down, a loss of a customer, or somebody didn't show up for work.

1) What happened?
2) Did we know this was going to happen?
3) When will it happen again?
4) What are we going to do about it?

Because of the 5 whys, I get a lot of resistance from smart people who think they need to understand why an event happened in order to prevent it from happening in the future. And they are typically insulted about the need to ask what happened, because this implies they didn't understand something. They will say to me, "I know what happened and what the problem is." And yet when I ask five different people what happened, I get five different answers. What does this mean? There is a poor understanding of what happened. How is this fixed? With a very careful investigation by a team.

When a plane crashes, do people ask the 5 whys on the spot and get an answer within minutes? No. They get a team of experts and they spend months carefully answering in minute detail "what happened?" What is their next question? You guessed it, "Did we know this was going to happen?" And they proceed through the four questions above. Why? Because they live in a fault-intolerant industry. They have to be continuously improving. The same event can't ever happen again. In order to achieve this they must change what they do and how they think, because what they were doing and thinking before wasn't good enough. Can you imagine what would happen in your board shop if you started this line of inquiry for any problem you face in a spirit of not having the same problem repeat itself again and again?

Is there any value to the 5 whys? I don't know, what do you think? What has been your experience? What are your ideas about how you could make the 5 whys better? For me, I find that with a little thinking, I can take any why question and turn it into a "what" question. And the new "what" question replaces three or four "why" questions. For example, the mind tools web site considers the problem of people who aren't using a new software system. Instead of asking, "Why aren't you using the new software?" and getting the answer, "because we don't like it," you can ask, "What are the reasons for not using the new software?" and the answers will form a list. Then you can ask, "What are your ideas about fixing the most annoying problems you are faced with?" (By the way, I find when people participate in the solution, all of the problems suddenly go away. Why is that?)

The next time your spouse is upset, start with, "What happened?" instead of "Why are you upset?" Make a note of the difference in the conversation. **PCB**

Gray McQuarrie is president of Grayrock & Associates, a team of experts dedicated to building collaborative team environments that make companies maximally effective. To read past columns, or to contact McQuarrie, click here.

VIDEO INTERVIEW

Lightweight Drilling with Interdyne Solutions

by Real Time with...IPC APEX EXPO 2013

Mike is presenting a linear drive drilling system that started from scratch to redefine drilling in the industry. The drives are all three axes and the cage, or "wing" as they call it, is made of super strong aircraft-type metals to minimize weight. All in all, a very exiting product!

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PCB007 Supplier/New Product News Highlights

Collaboration to Form Rogers Innovation Center

Rogers Corporation and Northeastern University have announced plans to establish the Rogers Innovation Center at Northeastern's George J. Kostas Research Institute for Homeland Security in Burlington, Massachusetts.

Enthone Unveils New Electroless Nickel Process

The ENPLATE Onyx mid-phos electroless nickel process is a cadmium-free and lead-free process that is engineered to provide an optimum black appearance on today's advanced designs and complex-part geometries.

Two Viasystems Facilities Earn Integral's Zeta Certification

The Viasystems facilities in Anaheim and Milpitas are the most recent PCB fabricators certified to use Integral Technology's revolutionary Zeta glass-free laminate and film solutions for rigid PCB applications.

KYOCERA to Acquire NEC Toppan Circuit Solutions

Kyocera Corporation has concluded a share transfer agreement with Toppan Printing Co., Ltd. and NEC Corporation to acquire all shares of the PCB manufacturing company NEC Toppan Circuit Solutions, Inc. to further strengthen and expand the Kyocera Group's organic substrate business.

Stevenage Converts to Taiyo Flexible Inkjet Legend Ink

Stevenage Circuits has selected Taiyo's IJR-4000 FW100 for use with their new Orbotech Sprint 120 inkjet printer. The ink is designed specifically for use with this equipment and specifically for flexible circuits.

Amphenol Reports 7% Sales Growth in Q2

Amphenol President and CEO, R. Adam Norwitt, stated, "We are pleased to report strong second quarter sales up 7% over the comparable 2012 quarter and 5% sequentially. The sales growth over last year was driven by increases in nearly all of our served markets led by the commercial aerospace, automotive, mobile networks and broadband markets."

Isola Unveils Breakthrough Low-loss Dk Product

Isola Group S.a.r.l., a market leader in copper-clad laminates and dielectric prepreg materials used to fabricate advanced multilayer PCBs, has announced Astra, the company's breakthrough very low-loss dielectric constant (Dk) product for millimeter wave frequencies and beyond.

DuPont, IQLP to Co-develop High-Speed Circuit Technology

"DuPont has been developing and expanding its product line for high-speed, high-frequency applications," said Michael Hennessy, global technology director. "We anticipate that our collaboration with IQLP will lead to opportunities to broaden our existing range of advanced materials for high-speed, high-frequency applications…"

Isola: Low-loss, Low-skew Materials for PCB Fabrication

Isola Group has announced its new low loss, low skew, high-speed material, GigaSync. This product has been engineered to eliminate skew issues in high-speed designs that use differential pairs to create a balanced transmission system able to carry differential (equal and opposite) signals across a PCB.

Taiyo America Realigns with Eyes on the Future

Taiyo America announces that Bob MacRae will now be the sales manager for the Eastern Region of the United States, as well as Eastern Canada and South America. Steve Campisi will also be supporting the same territories as technical service representative.

Final Finish Specifications Review: IPC Plating Sub-Committee 4-14

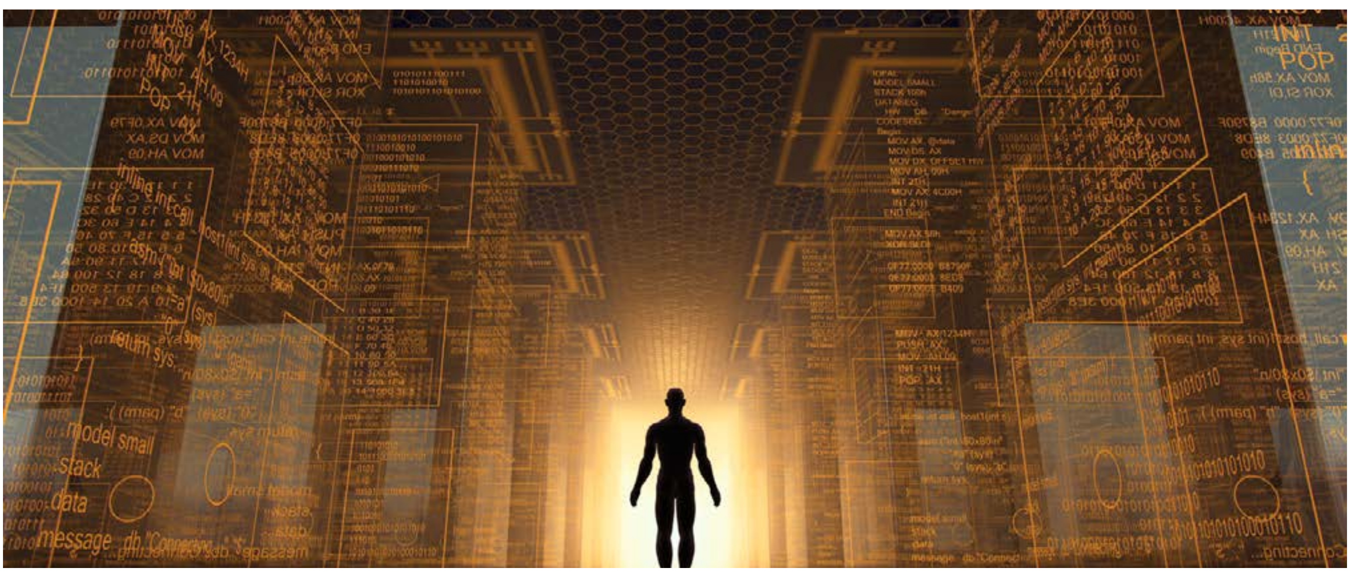
by George Milad
UYEMURA INTERNATIONAL CORP.

Specifications are consensus documents that are agreed upon by a panel of interested industry participants composed of suppliers, manufacturers, assembly houses and end users. The IPC Plating Sub-committee 4-14 is no exception. If there is consensus then the committee documents it in a specification. In cases where no consensus is readily arrived at, the committee undergoes its own testing in what is commonly referred to as a round robin (RR) study.

In an RR study, an agreed-upon test vehicle (TV) is designed and manufactured. The TVs are then sent to the different suppliers who deposit the agreed-upon thicknesses to be investigated. The TVs are collected and the deposit thicknesses are verified and documented. The TVs are then coded. The coding is done to conceal the identity of the specific supplier, to keep the evaluation objective and to ensure it is not a comparative study between different suppliers. This is followed by again sending the TVs to the different testing sites that test for the desired attribute like soldering, contacting and wire bonding capabilities of the different finish thicknesses. The data is then collected sorted out and documented. At this point a new attempt at consensus is made and upon arrival, the thickness specification is set.

Specifications are reference documents called out by designers and OEMs. Designers may take exception to one or more items in the specification to ensure that the product meets the requirements of its intended use. The term "AAUBUS," as agreed upon between user and supplier, is part of any specification.

The IPC Plating Sub-committee 4-14, chaired by Gerard O'Brien and me, has been active since 2001, with Tom Newton as the IPC liaison. The committee operates through bi-weekly, one-hour conference calls, and boasts an extensive member list. All decisions are made by those in attendance on these calls. The call minutes are documented and sent out to the entire membership, who acts as checkers to ensure that the committee is on track to meet its objectives. To date, all committee activities have been voluntary and acknowledgement is in order, for the members, and equally important to the man-



Designers: when you choose a fabricator, what guarantee do you have that they won't deliver scrap?

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How we qualify PCB manufacturers

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agement of their companies that believe in the need for industry specification and allow for the voluntary time invested by their employees.

Since its inception, the IPC Plating Subcommittee 4-14 has issued the following:

IPC-4552 ENIG Specification 2002
IPC-4553 Immersion Silver Specification 2005
IPC-4554 Immersion Tin Specification 2007
IPC-4553A Revised Immersion Silver Specification 2009
IPC-4552 Amended ENIG Specification 2011
IPC-4554 Amended Tin Specification 2011
IPC-4556 ENEPIG Specification 2013

IPC-4552 ENIG Specification (2002)

The ENIG IPC-4552 Specification was issued in 2002; at that time the idea of lead-free (LF) had not taken hold in the industry, and tin/lead was the dominant assembly solder in use.

For thickness, IPC-4552 stated:

- The electroless nickel thickness shall be 3–6 μm [118.1 to 236.2 μin]
- The minimum immersion gold thickness shall be 0.05 [1.97 μin] at four sigma (standard deviation) below the mean; the typical range is 0.075–0.125 μm [2.955– 4.925 μin]

To arrive at these numbers the committee conducted a series of test in a round robin study that included suppliers, PCB manufacturers, EMS providers and OEMs. The data are summarized in the appendix of the specification.

As the price of gold soared, there was pressure on the committee to revise the lower limits for ENIG. The ENIG specification was amended and the lower limit for thickness was reduced from 0.05 μm to 0.04 μm (1.6 μin); however, some restrictions were added, such as ability to measure, and limited time from manufacturing to assembly as well as demonstrating the consistency and reproducibility of the plating process.

“As the price of gold soared, there was pressure on the committee to revise the lower limits for ENIG.”

Presently, the IPC-4552 A, ENIG Specification revision is in progress. The purpose is to reduce the lower limit of thickness as per the amendment and to determine if the restriction imposed earlier could be lifted. This entails a RR study and a full investigation to ensure that the lower limit will not create problems for the industry. In addition, all testing will include LF solder and LF stressing conditions; both were not available when the initial IPC-4552 was issued.

IPC-4553 Immersion Silver specification (2005)

The specification for immersion silver was issued in 2005. At that time there were two distinct types of immersion silver that were commercialized. One type could only produce a thin deposit of silver and the other produced a thicker deposit. As both had market penetration the committee had to specify the two types. The initial 4553 specification stated the following for thickness of deposit:

- Thin silver: 0.05 μm (2 μ”) minimum at -2σ from process mean as measured on a pad of area 2.25^2 μm (3600^2 mils). Typical value 0.07 μm (3 μ”) to 0.12 μm (5 μ”)
- Thick silver: 0.12 μm (5 μ”) minimum at -4σ from process mean as measured on a pad of area 2.25^2 μm (3600^2 mils). Typical value of 0.2 μm (8 μ”) to 0.3 μm (12 μ”).

The IPC 4553 Silver specification was unique:

- Two thicknesses were specified
- No upper limit in the specification
- The pad size for measuring thickness was defined

IPC-4553 A Immersion Silver specification (2009)

Over the next couple of years, the supply of the thin silver dwindled and was replaced by the thick version. It was necessary for the commit-

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Bangalore, India

September 10–12, 2013
IPC Conference on Component Technology: Closing the Gap in the Chip to PCB Process
Sponsored by Amkor Technology, Inc.
Chandler, AZ

September 24–26, 2013
IPC Technology Market Research Conference & Management Meetings
Chicago, IL

October 12–17, 2013
IPC Fall Standards Development Committee Meetings
Co-located with SMTA International
Fort Worth, TX

October 16, 2013
IPC Conference on Assembly and Reliability
Bangkok, Thailand

October 23
Conflict Minerals Conference: What an EU Company Needs to Know
Brussels, Belgium

November 12–13, 2013
7th International Symposium on Tin Whiskers
Hosted by IPC and CALCE; Sponsored by Lockheed Martin
Costa Mesa, CA

November 13–14, 2013
IPC Conference on Solder and Reliability: Materials, Processes and Test
Costa Mesa, CA

December 4–6, 2013
HKPCA International Printed Circuit and IPC APEX South China Fair
Shenzhen, China

More Information
www.ipc.org/events

SAVE THE DATE

IPC Technology Market Research Conference & IPC Management Meetings

September 24–26, 2013 • Allerton Hotel • Chicago, IL

The Next Generation:

Creating the Electronics Industry of the Future

The IPC Technology Market Research Conference (TMRC) & IPC Management Meetings are the only events of their kind in the electronics industry that provide a high-level perspective on technology, market trends and management issues for senior-level decision-makers. Geared for the executive, these events will give you a unique view of the industry so you can take action. It's the one venue where you can:

- Discover how key technology drivers will impact your industry segment.
- Get a preview of emerging market trends … and what they will mean for your business.
- Hear from leading technologists on new advancements and their impact on industry needs.
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- Network with potential customers and suppliers who can provide the answers you need.

No other event will provide you with this type of information or allow you such access to other industry executives.

Management Meetings — September 24
TMRC — September 25–26

For more information, visit www.ipc.org/tmrc-mm or contact Susan Filz, IPC director of industry programs.

Questions? Contact IPC registration staff at +1 847-597-2861 or registration@ipc.org.

tee to revise the specification. Rev A contained two important revisions. The first eliminated the terms "thin" and "thick" and specified a single thickness. The second set an upper limit for immersion silver thickness.

The thickness specification of immersion silver IPC-4553 A states:

- 0.12 μm (5 μin) minimum to 0.4 μm (16 μin) maximum at ± 4σ from process mean as measured on a pad of area 2.25 mm^2 or 1.5 mm X 1.5 mm (approximately 0.0036 in^2 or 0.060 in x 0.060 in); typical value between 0.2 μm (8 μin) to 0.3 μm (12 μin).

"After more than one year of struggling with the specification nothing was issued. There was no consensus arrived at."

IPC-4554 Immersion Tin Specification 2007

For immersion tin, the committee specified a lower limit for thickness. The relatively thick value of 1 micron was chosen to ensure that enough virgin tin would be available at the surface for soldering after storage. It is well understood that tin forms an intermetallic (IMC) layer with the underlying copper, and that this layer continues to grow in thickness over time.

The immersion tin thickness will be:

- μm (40 μ") minimum at -4σ from process mean as measured on a pad of area 2.25^2 μm (3600^2 mils). Typical value of 1.15 μm (46 μ") to 1.3 μm (52 μ")

Immersion Tin Specification IPC-4554 was amended in 2011. The amendment addressed solderability testing and specified the allowed stress testing conditions for the deposit and the type of fluxes to be used for both tin/lead and LF testing.

IPC-4556 ENEPIG Specification 2013

This is the last specification issued by the committee. The document produced is very comprehensive and includes a wealth of information from the RR studies that were conducted. The Appendix contains a documentation of these studies; each is authored by the principle who conducted the testing. It also includes a section on the proper methods of equipment setup for a reliable measurement of very thin layers of metal deposits.

The thickness specification for ENEPIG states:

- Nickel: 3–6 μm (118.1 to 236.2 μin) at ± 4 sigma (standard deviations) from the mean
- Palladium: 0.05–0.15 μm [2–12 μin) at ± 4 sigma (standard deviations) from the mean.
- Gold: 0.025 μm (1.2 μin) at -4 sigma (standard deviations) below the mean

All measurements to be taken on a nominal pad size of 1.5 mm x 1.5 mm [0.060 in x 0.060 in] or equivalent area.

It is noteworthy that the committee had spent considerable time working an organic solderability preservative (OSP) specification that was designated IPC-4555. After more than one year of struggling with the specification nothing was issued. There was no consensus arrived at. Mostly this was due to the wide assortment of organic products that were used for solderability preservation for the various applications, each with its own thickness recommended values.

Conference calls are held every other Wednesday at 11:00 a.m., EST, and anyone may participate. **PCB**

George Milad is the national accounts manager for technology at Uyemura International Corporation. Milad is the recipient of the IPC 2009 President's award, current chair of the IPC Plating Committee and a permanent member of the Technical Activities Executive Committee of the IPC. Contact Milad at gmilad@uyemura.com.

TOP TEN

PCB007 News Highlights This Month

1 Omni Circuit Boards Develops Aluminium Trace Circuit Board

Omni Circuit Boards has announced the successful development of an aluminium, monometal wire-bonded circuit board. The prototype, designed and manufactured for use in a D-Wave systems quantum supercomputer, allows for superconductivity and operation in low temperatures just above absolute zero.

2 IPC, JPCA: New Design Guidelines for Printed Electronics

"IPC will continue its work on the design guidelines, in collaboration with JPCA, to secure additional companies' experiences. We encourage companies with expertise in this area to help by participating in the continuing international consensus-building committee process," said IPC Director of Technology Transfer Marc Carter.

3 The PCB List Celebrates Anniversary

"The participation of fabricators in claiming and populating their listing is directly proportionate to how beneficial The PCB List is. It's simple and only takes a few minutes to get your company up and searchable to an expansive list of registered buyers," noted Patty Goldman, sales director for The PCB List.

4 MFLEX Reports 20% Q3 Decline in Net Sales

"We believe our third quarter results will serve as an inflection point as we anticipate a meaningful sequential improvement in revenue in the fourth quarter, with continued momentum into fiscal 2014. As a result, we expect to return to profitability in the first quarter of fiscal 2014, as well as on a full year basis in fiscal 2014," said Reza Meshgin, CEO.

5 IPC N.A. PCB Industry Study Forecasts Growth by Year End

North American PCB production should see a return to modest growth by the end of 2013. The growth is expected to continue through 2016, not just for North America, but also for world PCB production as a whole. Recently released by IPC, the annual survey-based study provides a comprehensive overview of the market and business of PCB manufacturing.

6 German PCB Market Continues Growth in May

Despite May 2013 having only 19 working days, total turnover for the month was still 5.6% higher from April, and 3.3% higher from the same period last year.

7 Viasystems in Line with Expectations; Q2 Sales Nearly Flat

Net sales and operating income in the company's PCB segment for 2Q13 were $240.7 million and $4.7 million, respectively, compared with PCB segment net sales and operating income of $240.4 million and $15.1 million, respectively, for 2Q12.

8 IPC Trims PCB Sales Forecast; June Bookings Down 6%

"Until this June, monthly PCB orders outpaced sales every month since January, which has produced positive book-to-bill ratios for the past six months," said Sharon Starr, director of market research.

9 TTM Technologies Q2 Net Sales Up 4%

"Overall results for the second quarter were in line with our guidance," said Kent Alder, CEO. "During the quarter, we experienced broad-based strength in our networking and communications end market in both Asia Pacific and North America…"

10 AT&S Begins FY 2013/14 on Positive Note

"Despite the challenging market environment, both mobile devices and automotive and industrial segments reported significant year-on-year improvements in revenue and capacity utilisation. We have good reason to be satisfied with how the financial year 2013/14 has started, and have laid a solid foundation for the year to come," explained CEO Andreas Gerstenmayer.

EVENTS

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar of Events, click here.

For a complete listing, check out *The PCB Magazine's* full events calendar.

NEXTGEN AHEAD
September 9–11, 2013
Washington, D.C., USA

International Test Conference 2013
September 10–12, 2013
Anaheim, California, USA

Capital Expo & Tech Forum
September 10, 2013
Laurel, Maryland, USA

2013 MEPTEC
September 17–18, 2013
Tempe, Arizona, USA

Failure Analysis of Electronics Short Course
September 17–20, 2013
University of Maryland, Maryland, USA

Electronics Operating in Harsh Environments Workshop
September 17, 2013
Cork, Ireland

IESF 2013: Integrated Electrical Solutions Forum
September 19, 2013
Dearborn, Michigan, USA

MRO EUROPE 2013
September 24–26, 2013
London, UK

PCB West 2013
September 24–26, 2013
Santa Clara, California USA

ID WORLD Rio de Janeiro 2013
September 26–27, 2013
Rio de Janeiro, Brazil

SAE 2013 Counterfeit Parts Avoidance Symposium
September 27, 2013
Montreal, Quebec, Canada

2013 SMART Group European Conference
October 2–3, 2013
Oxfordshire, UK

RFID in High-Tech
October 2–3, 2013
Santa Clara, California, USA

Long Island SMTA Expo and Technical Forum
October 9, 2013
Islandia, New York, USA

IEEE SMC 2013
October 13–16, 2013
Manchester, UK

electronicAsia
October 13–16, 2013
Hong Kong, China

SMTA International
October 13–17, 2013
Fort Worth, Texas, USA

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ADVERTISER INDEX

Next Month in *The PCB Magazine:*

Automotive & Transportation

The automobile industry continues to advance from the mechanical world into the ICT and electronics world. The global demand for OEM automotive electronics is forecast to exceed $174B by 2014, with major growth in safety and security and powertrain applications. What will be the effect on the PCB industry? What is holding back the predicted green revolution in electromobility? When will there be a breakthrough in battery technology? These questions and more will be addressed in the October issue of *The PCB Magazine.*