

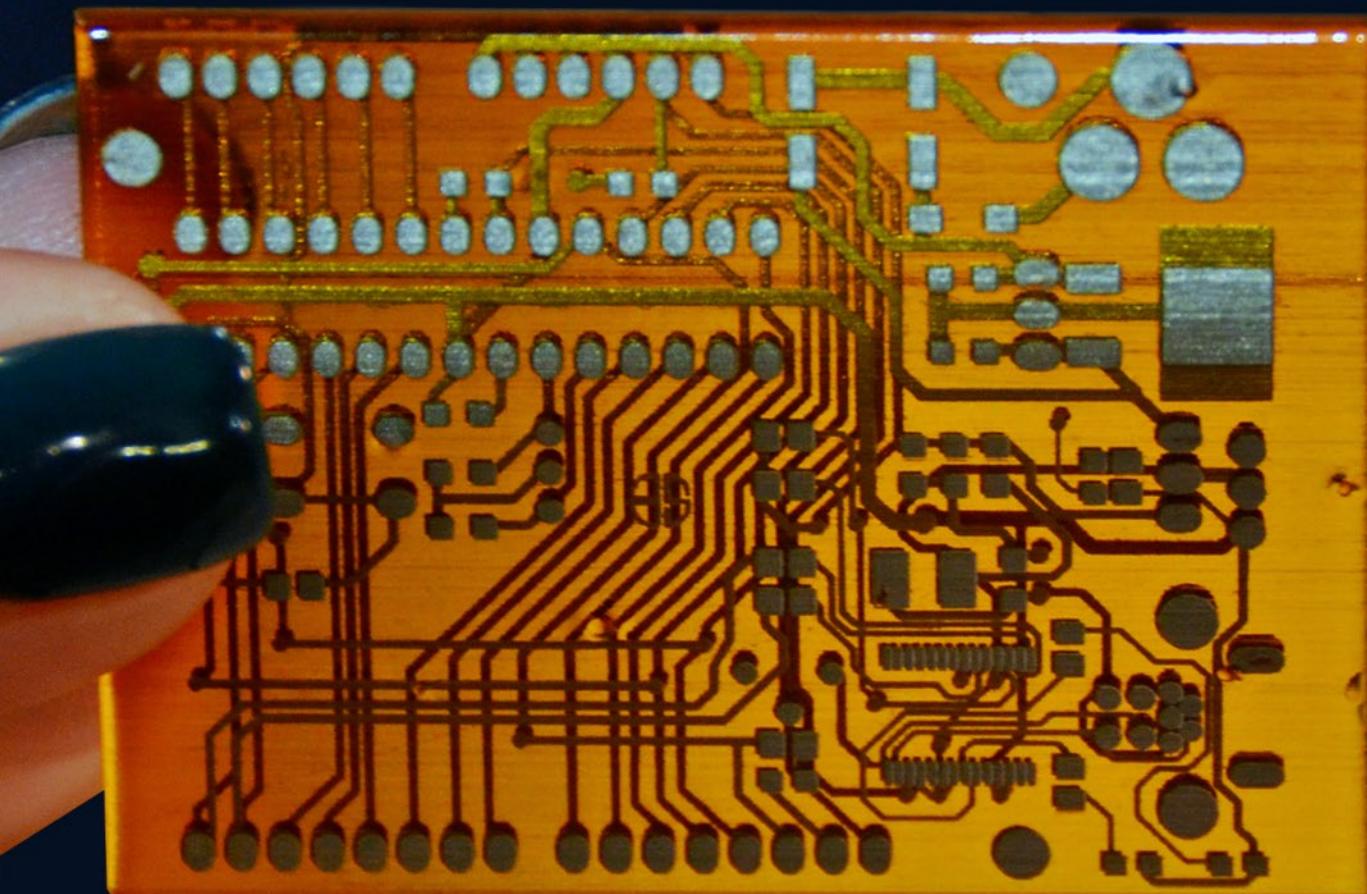
February 2016

# *the* pcb magazine

**What's New  
in PCB Fabrication?**

- ▶ 12 New Material and Process Solutions for the Electronics Interconnection Industry
- ▶ 32 Copper Via-Fill Technology in Development
- ▶ 36 Camtek Takes Injet Technology into the Future

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*An Interview with Simon Fried,  
Nano Dimension, pg. 24*

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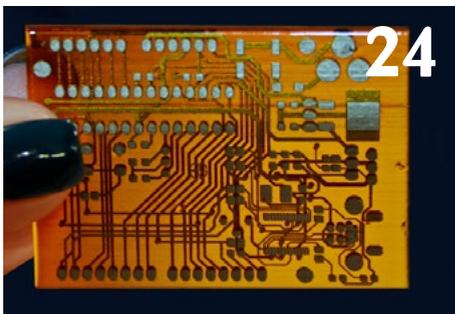
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## What's New in PCB Fabrication

We've covered it from top to bottom this month—what's brand new in the world of PCB fabrication *and* what's on the horizon for our industry. Feature articles, interviews and columns reach into material and process solutions, 3D printing, surface finishing, and more!



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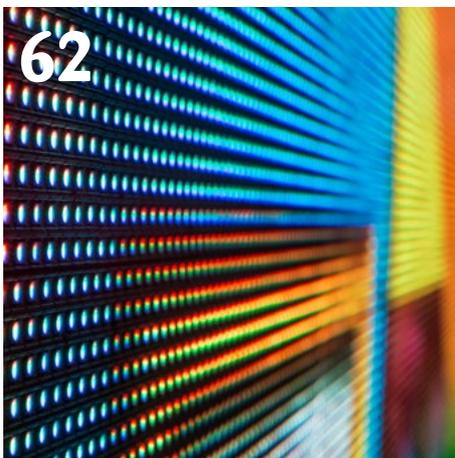
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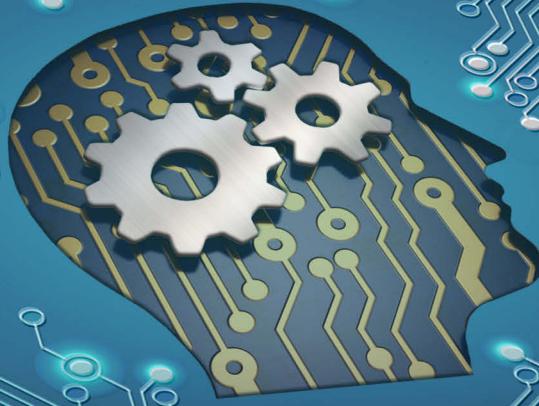
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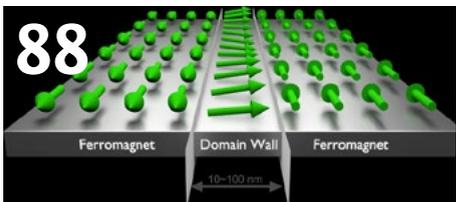
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Df @ 10 GHz	0.0030	0.0017	0.0031	0.0028 - 0.0036
CTE Z-axis (50 to 260°C)	2.90%	2.90%	2.80%	2.90%
T-260 & T-288	>60	>60	>60	>60
Halogen free	Yes	No	No	No
VLP-2 (2 micron Rz copper)	Standard	Standard	Available	Available
Stable Dk and Df over the temperature range	-55°C to +125°C	-40°C to +140°C	-55°C to +125°C	-55°C to +125°C
Optimized Global constructions for Pb-Free Assembly	Yes	Yes	Yes	Yes
Compatible with other Isola products for hybrid designs	Yes	Yes	Yes	For use in double-sided applications
Low PIM < -155 dBc	Yes	Yes	Yes	Yes

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# So... What *is* New in PCB Fabrication?

by **Patty Goldman**

I-CONNECT007

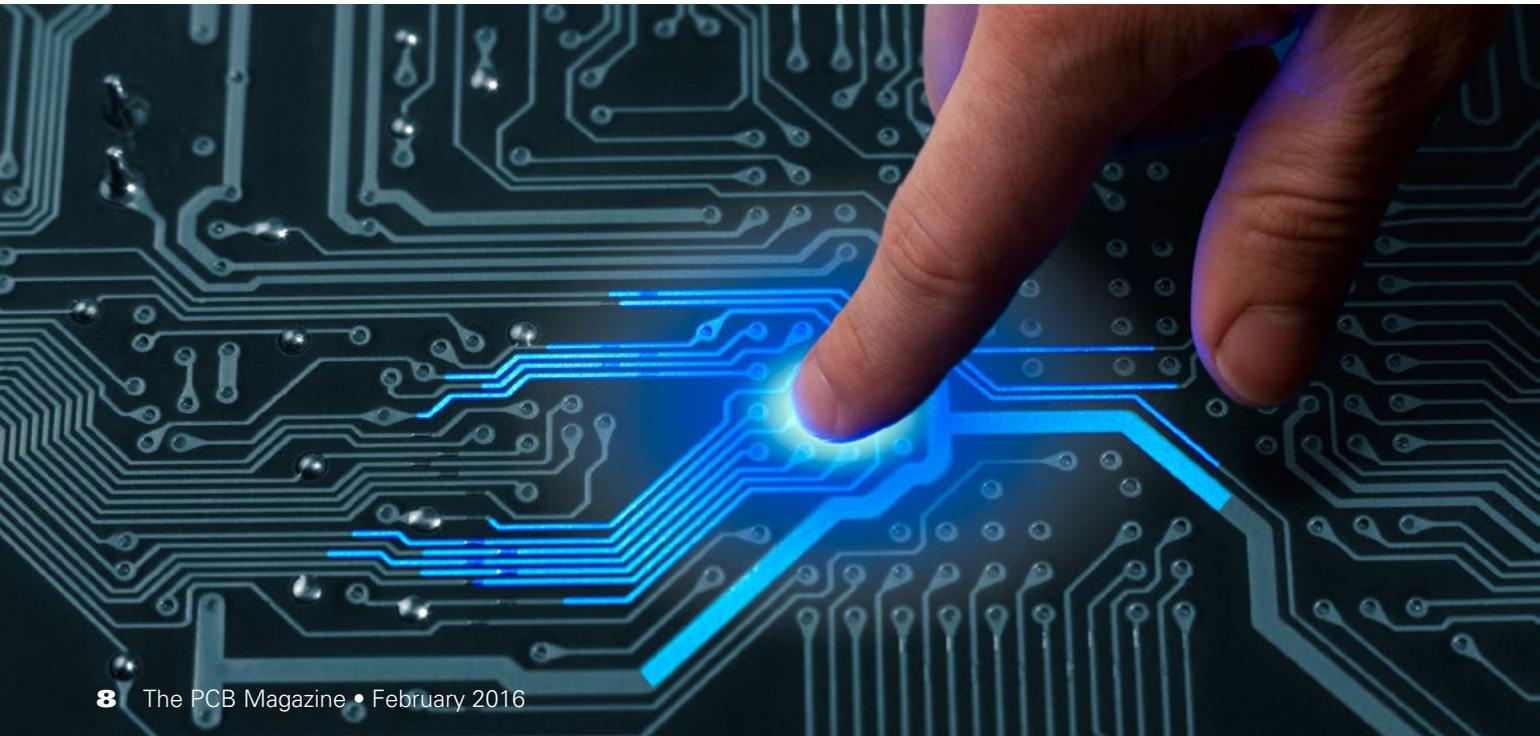
There's a lot that's new. It's not just new equipment and materials to build the PCBs we've been making forever; there are also new ways to build a whole different type of PCB. You've probably heard lots of buzz about printing—not just inkjetting circuit patterns, but building entire PCBs, from layer 1 to layer n. Is it a reality? Will it take the industry by storm? Or will we continue making our boards the traditional way, but with some modifications and with new, improved processes to get us there? Will PCBs as we know (and love) them disappear?

Of course, the jury is out. But my experience is that the old never really disappears. Thirty or so years ago the demise of single-sided boards was widely predicted as multilayer technology matured and came into its own. But I was working with a Chicago facility that made a ton of those “punch-and-crunch” boards by discovering ways to fit the circuitry from two sides onto

one side, eliminating much processing (PTH and electroplating processes) and saving their customers big bucks. And those are still with us in greater volume than ever—when your cat's toy has a circuit in it, you know they are everywhere. So too, I believe, with the technologies we have today. They don't go away but other technologies will grow up beside them, probably cannibalizing some amount of square footage in the process. Considering the seemingly endless applications that arise at an ever-increasing rate these days, I believe there is room for all.

We cover quite a lot of ground in this month's issue, from articles on what is truly new and very different in the way to create a PCB to better processes for building the traditional ones. We also have a couple pieces for you guys out on the floor who need a little how-to info. Let's get going and do it!

Joe Fjelstad of Verdant Electronics starts us off with a dissertation on one of those new ways



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to build a printed board, this time by printing or jet-printing a conductive silver paste to create both the circuit pattern and fill the vias.

We follow this interesting info with an interview with Nano Dimension's Simon Fried, who tells us about technology to print the entire circuit board—yes, dielectric and circuitry, multilayers included—on a 3D printer. This technology appears perfect for making prototypes in a fairly short time span and we can envision every designer wanting one right next to his/her desk. Sounds great for every PCB fabricator, too, to be able to cut their prototype turnaround time to just a few hours rather than the typical 24–48.

Next, Tara Dunn of Omni PCB fills us in (pun intended) on a new via fill technology, this one based on a nano copper ink developed by Intrinsiq. One nice advantage is that the sintering process can be accomplished using equipment already in the PCB facility.

In another interview, Amir Tzchori of Camtek tells us about their inkjet-printed solder mask system, designed for high-mix, low-volume PCB fabricators. He stresses the importance of a total process and supplier responsibility. Very interesting.

But what about making PCBs and multilayers the usual way? Any new processes for that? Something of enduring interest to PCB manufacturers and assemblers alike is the final surface finish on the PCB. Jun Nable of MacDermid writes about a new immersion gold process that has been developed that is cyanide-free. As regulations continue to stiffen, this is certainly of interest to all.

Osamu Sekine of Nano System gives us an interesting discussion on the various types of lasers that can be used in PCB processing to create vias of all sizes and shapes. He then presents versatile equipment that can evolve with one's technology advances and accommodate all these types.

Then, Josh Goldberg of Taiyo presents a very informative primer on developing solder masks for the LED industry, including the challenges of making white truly white and keeping it that way through the various heat cycles experienced by a PCB.

Back to via fill and another technology, this one using your existing plating line. Uyemura's George Milad goes into detail on how to set up the copper electroplating process to successfully and properly plate blind vias. A fine, practical paper for you process engineers out there.

And in another one for engineers, we have Steve Williams of The Right Approach Consulting with a discussion on RCA—root cause analysis. This formal approach to troubleshooting gives a very useful framework to keep you on track in your problem-solving efforts. And of course your customers will more than appreciate the results.

Next month our topic is "Strategies to Increase Profits," and it's not just for managers or CFOs. No, profits are improved by reducing scrap and returns, improving flow through the shop, working more closely with designers and customers, and a myriad of other ways. Tune in then, which is easy when you [subscribe](#) and the magazine pops right up in your mailbox the moment it publishes. **PCB**



**Patricia Goldman** is a 30+ year veteran of the PCB industry, with experience in a variety of areas, including R&D of imaging technologies, wet process engineering, and sales and marketing of PWB chemistry.

She has worked actively with IPC since 1981 and served as TAEC chairman, and is also the co-author of numerous technical papers. To contact Goldman, [click here](#).

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# New Material and Process Solutions for the Electronic Interconnection Industry



by **Joseph Fjelstad**  
VERDANT ELECTRONICS

## Introduction

The manufacture of electronics has, for the last several decades, followed a production script that has changed little over time. The vast majority of printed circuits are still being manufactured and assembled using materials and processes that the pioneers of the early printed circuit industry would easily recognize. The primary reason is that most circuit design practices are deeply rooted and tied to traditional manufacturing methods. However, these methods are not the only ones that can be used to manufacture and assemble printed circuits today. In fact, it is arguable that traditional methods are not as well-suited to the manufacture of today's more challenging product designs. This is a fact that has not been lost on Japanese product engineers. Over the last nearly two decades, they have conceived of and reduced to practice a number of unique methods for making high-density interconnection product. One of

the important keys to making this possible has been the development of materials uniquely designed and structured to filling special needs of these advanced circuit designs.

Though perhaps not a household name, 70-year-old Tatsuta Electric Wire & Cable Co., Ltd. has been at the forefront of the development of such materials for many years. As the name implies, the company was originally focused on providing wire and cabling solutions for the electrical and electronics industries. However, realizing that the scope of their business extended beyond wire harnesses and cables, the company began to develop materials suited to the needs of printed wiring manufacturers and assemblers. This article has been prepared to familiarize the readers of this esteemed electronics publication of some of the new material and process solutions the company has developed and is making available to the industry.

## Solutions for the Printed Circuit Industry

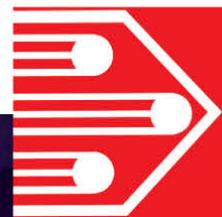
While the company has solutions spanning everything from high power electrical cable to

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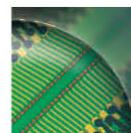
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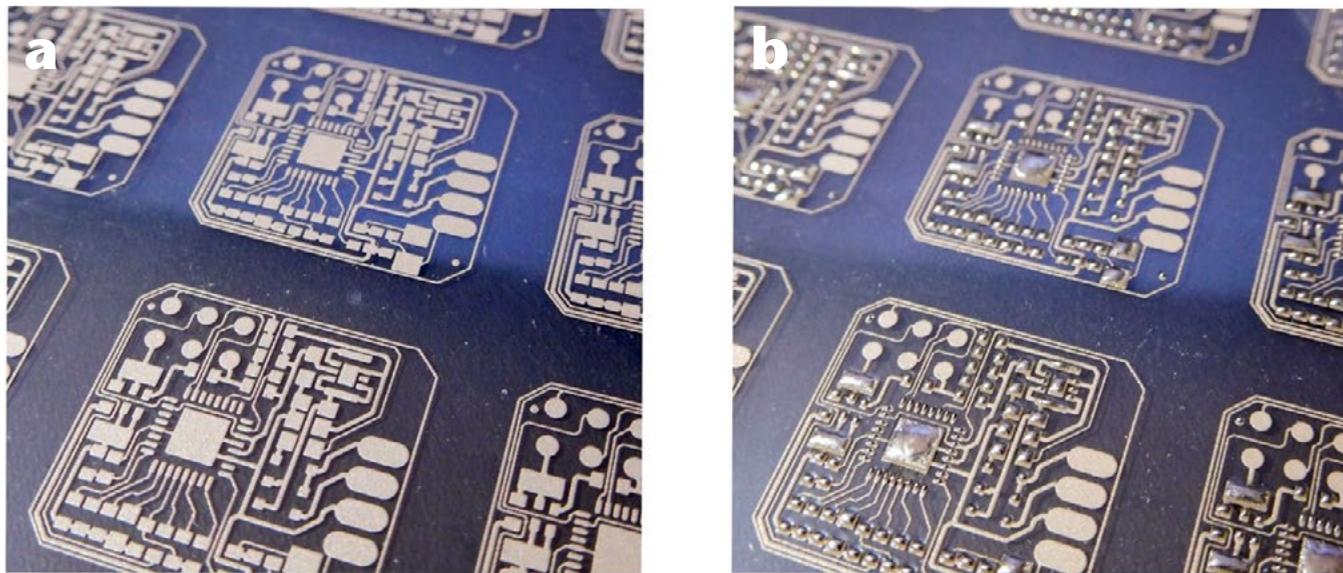


Figure 1: The printed paste is capable of resolving fine circuits features as illustrated in 1a; however, of equal importance, the printed metal is directly solderable as shown on the right, where Sn42Bi58 paste has been reflowed onto selected lands on the polyester base substrate.

high-speed optical fiber cables, and even extending to bonding wire used for making interconnection between chip and package, the focus of this discussion will be on some of the enabling conductive materials the company has for the printed circuit industry. These materials serve a range of needs from circuit production, to alternative layer-to-layer interconnection materials, to thermal via solutions, to EMI protection. Following is a discussion of these different areas of application.

### Circuit Production Materials

Circuits manufactured today are most often produced by a process that involves electroplating copper circuits and plated-through-holes on a piece of copper-clad laminate and then etching the circuit pattern. In contrast, Tatsuta set its sights on developing metal paste which can be screened or possibly jet-printed directly onto an insulating substrate to create the circuit pattern.

The conductive paste is comprised of silver-coated copper particles, produced in a practical range of 3–5  $\mu\text{m}$  size, evenly distributed into an epoxy resin/butyl carbitol base. The final product is 89% metal. The company has demonstrated the ability to print circuit features

down to 100  $\mu\text{m}$  line and space and the cure temperature is a modest 130°C (suitable for use with polyester base materials) resulting in conductors with a volume resistivity in the range of 1.0–2.0  $\times 10^{-4}$   $\Omega$  cm. Finally, and not unimportantly, the finished circuits have shown good solderability with common solder pastes. An example of a printed product is shown in Figure 1a and the same circuit pattern is shown with printed and reflowed solder on its lands in Figure 1b. Further demonstration of the capability of the product is found in Figure 2 where full array solder-coated contacts with pitches of 0.65 mm, 0.5 mm and 0.4 mm are shown. Finally, Figure 3 shows contacts for a peripherally leaded device to further evidence the fine feature printing capability of the conductor paste.

### Via Fill Materials for Many Applications

Metal pastes have and are serving a range of applications in today's high performance electronics. Those familiar with some of Japan's leading high density circuit manufacturing technology will appreciate how metal pastes have been used for interconnection of circuit features between metal layers. The two most common are B2IT solution and ALIVH (Any Layer Interstitial Via Hole) technologies. ALIVH

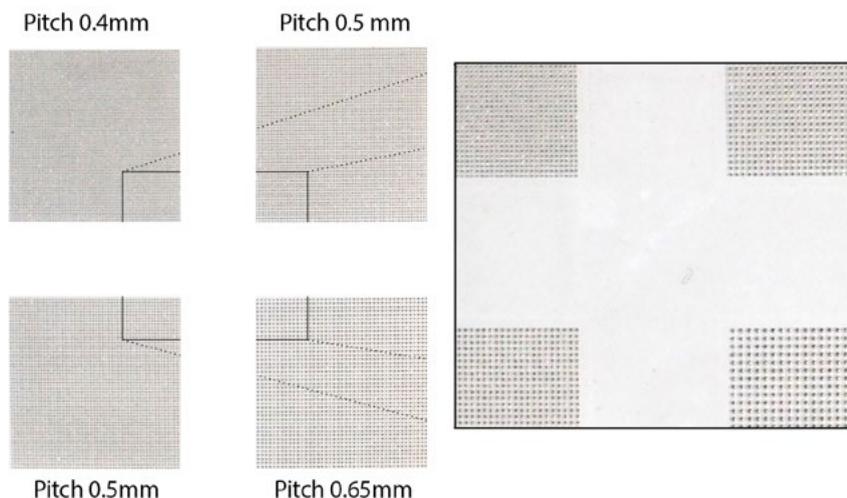


Figure 2: Printed conductors suitable for many of today's highest density circuits can be achieved as shown above. Note that the contacts for the full array lead pitches shown, which range from 0.65 mm down to 0.4 mm, have reflowed solder contacts. It should also be recognized that the base material for this, and the other demonstration circuits shown in this paper, is polyester, a highly economical base material for PCB construction.

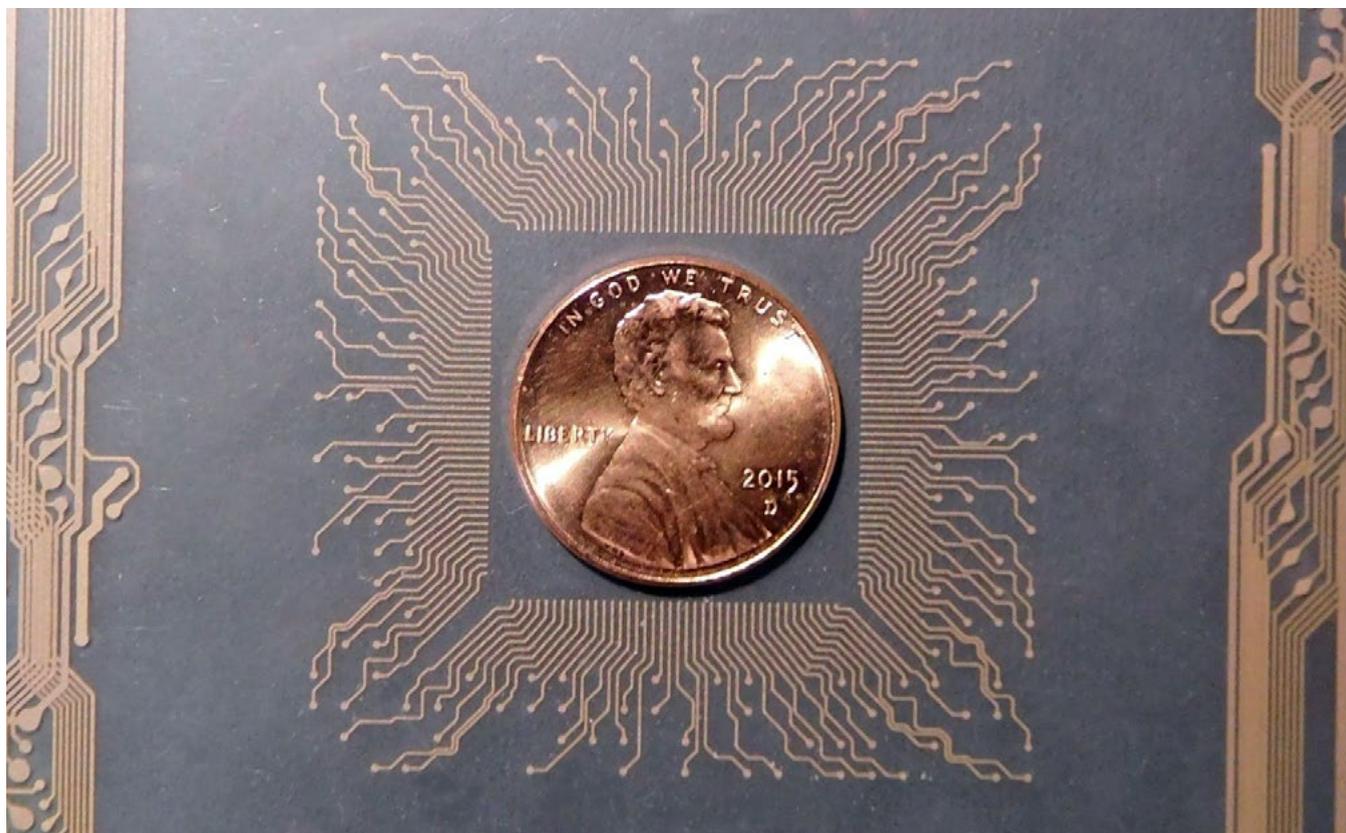


Figure 3: The technology is not only capable of printing fine line features, it is suitable for making circuits having more than one conductive layer as is in evidence in the circuit pattern on both left and right halves of the image.

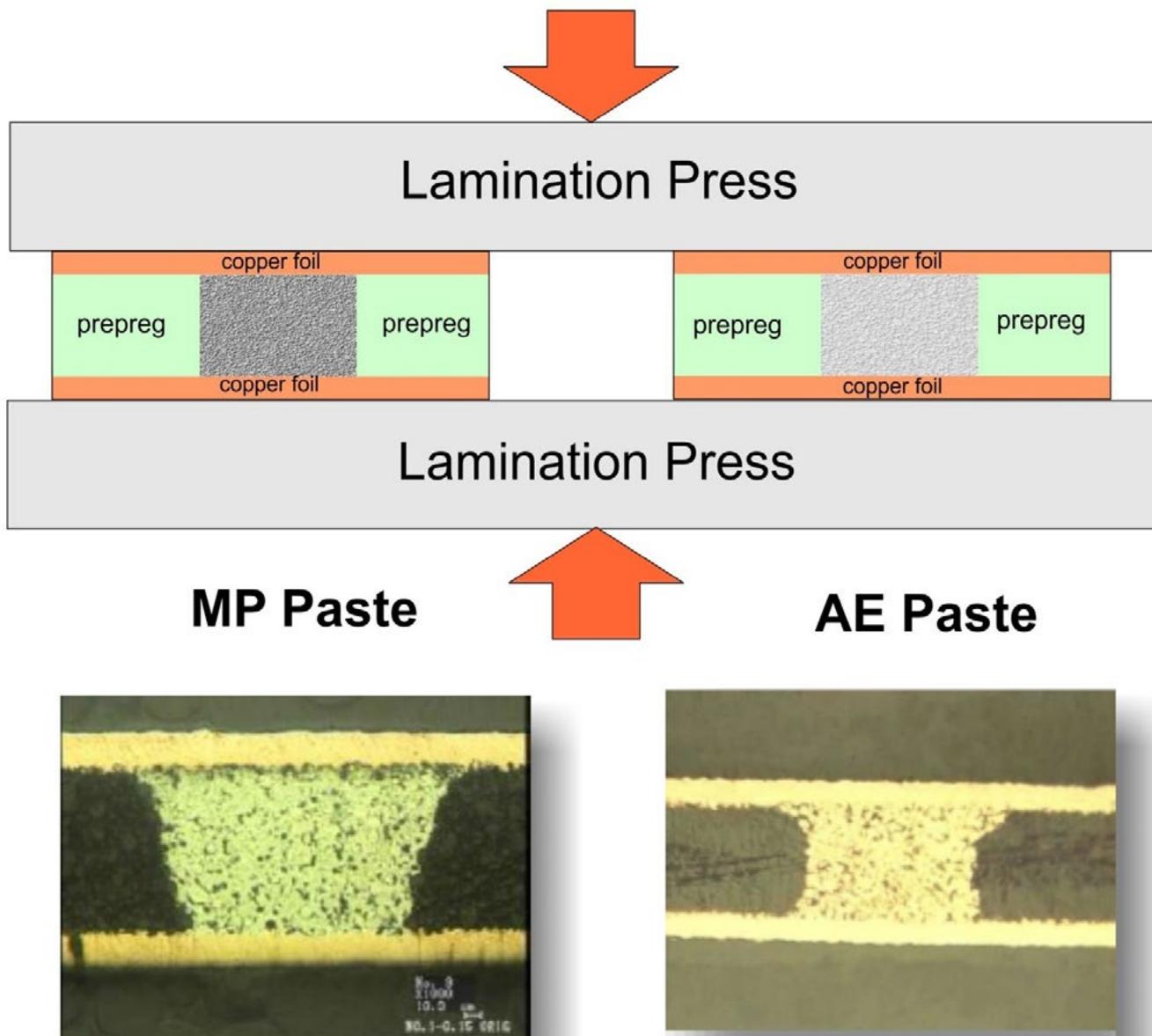


Figure 4: Via paste materials MP series and AE series have differing means of making interconnection between layers. The MP material has a nominal final volume resistivity of  $8.0 \times 10^{-5} \Omega \text{ cm}$  while the AP material is slightly higher, on the order of  $1.0 \times 10^{-4} \Omega \text{ cm}$ .

is arguably the simpler process of the two and it is finding increased use as Tatsuta builds on the 11 patents related to ALIVH technology, which were acquired by and transferred to Tatsuta from Panasonic last year. However, the metal paste's application is not limited and can serve other important functions as well. This will be discussed in more detail after this brief discussion of Tatsuta's conductive mate-

rial applied to layer-to-layer interconnection applications.

Two basic types of paste have been developed for use as conductive materials for vias in printed circuit production. The first is referred to as a metallized paste which is comprised of a mixture of low and high melting point powders in a binder material. In the lamination process the different materials

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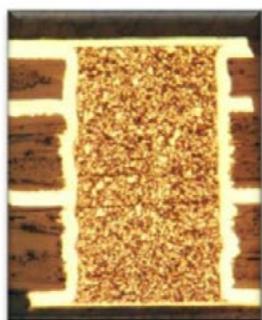
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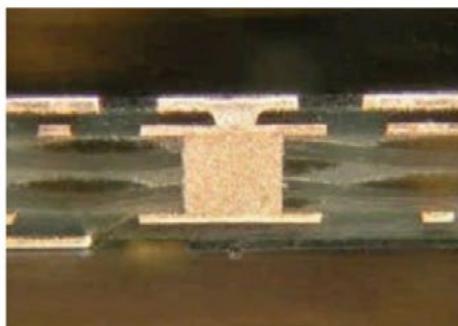


form metallurgical bonds both between themselves and the exposed copper foil. The second type is referred to as a conductive paste and is comprised of silver-coated copper particles in a binder material which shrinks during cure. These materials and their operation are illustrated in Figure 4.

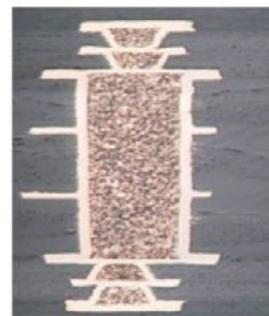
The second area of application of metal pastes for vias is used in concert with plated-through-holes in PCBs. Through-hole vias are vulnerable features when exposed to the high temperatures required for commonly used SAC alloy solders. To protect the vias, via fill materials are often called on to mitigate the strain



Expansion Control Paste  
Non conductive  
(Cu/epoxy)



Thermal Control Paste  
Conductive  
(Ag/Cu epoxy)



Thermal Via Paste  
Conductive  
(Ag/Cu epoxy)

Figure 5: Tatsuta has formulated different types of materials in the via fill space for different applications. The “non-conductive” copper epoxy paste on the right is designed to manage expansion and protect plated-through-holes. While not suitable for electrical purposes it does have a measure of thermal conductivity. The conductive pastes are designed to provide better thermal conduction.

**Test Vehicle Construction Details**

**Thermal Performance Comparison**

Via Diameter: 0.6mm, PCB Thickness: 0.6mm,  
PTH Wall: 20µm, Cap Plating: 15µm Via 35µm,  
Conductive Paste AE 1244: 11.7W/mK

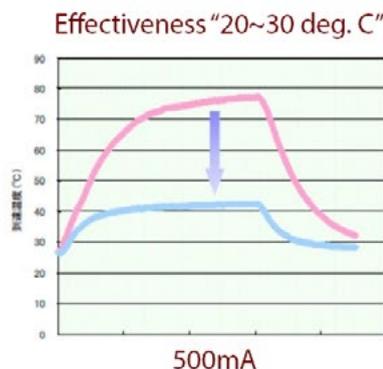
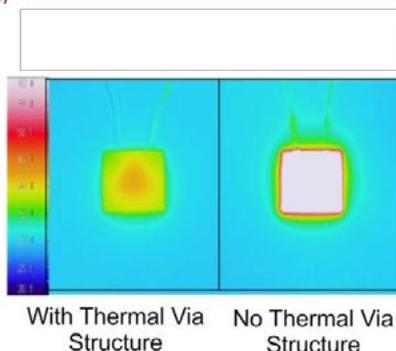
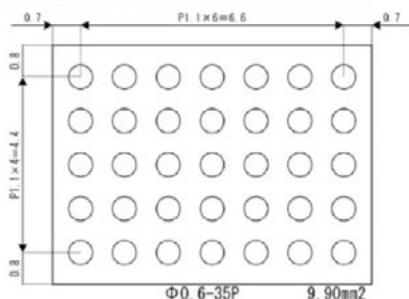


Figure 6: The efficacy of Tatsuta’s conductive paste AE1244 is demonstrated by the test performed. Note that this test was to demonstrate the potential of the material; different designs and components may require a modification to this.



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on the through-holes during the soldering process. However, via filling is not limited to protecting the through-holes; it can also be used to help improve heat transfer from high operating temperature components during operation. Tatsuta has developed a range of pastes both non-conductive and conductive to fill both potential needs. These are shown in Figure 5 and the thermal performance of an AE series material in managing heat generated on a test vehicle is shown in Figure 6.

**ESD/EMI/Controlled Impedance Materials**

In addition to the many materials discussed, there is one more product that is wor-

thy of inclusion in this brief overview of Tatsuta’s material and process offerings to printed circuit manufacturers. Included in this group is a range of materials generally provided in film form specially developed to manage ESD and EMI challenges, as well as some applications where controlled impedance is required. The general product set is laid out in Figure 7. It is simple and descriptive but it belies the nuance capabilities of the many materials available. The range of material includes various conductive, anisotropically conductive and non-conductive films and includes both thermal setting and pressure sensitive application methods.

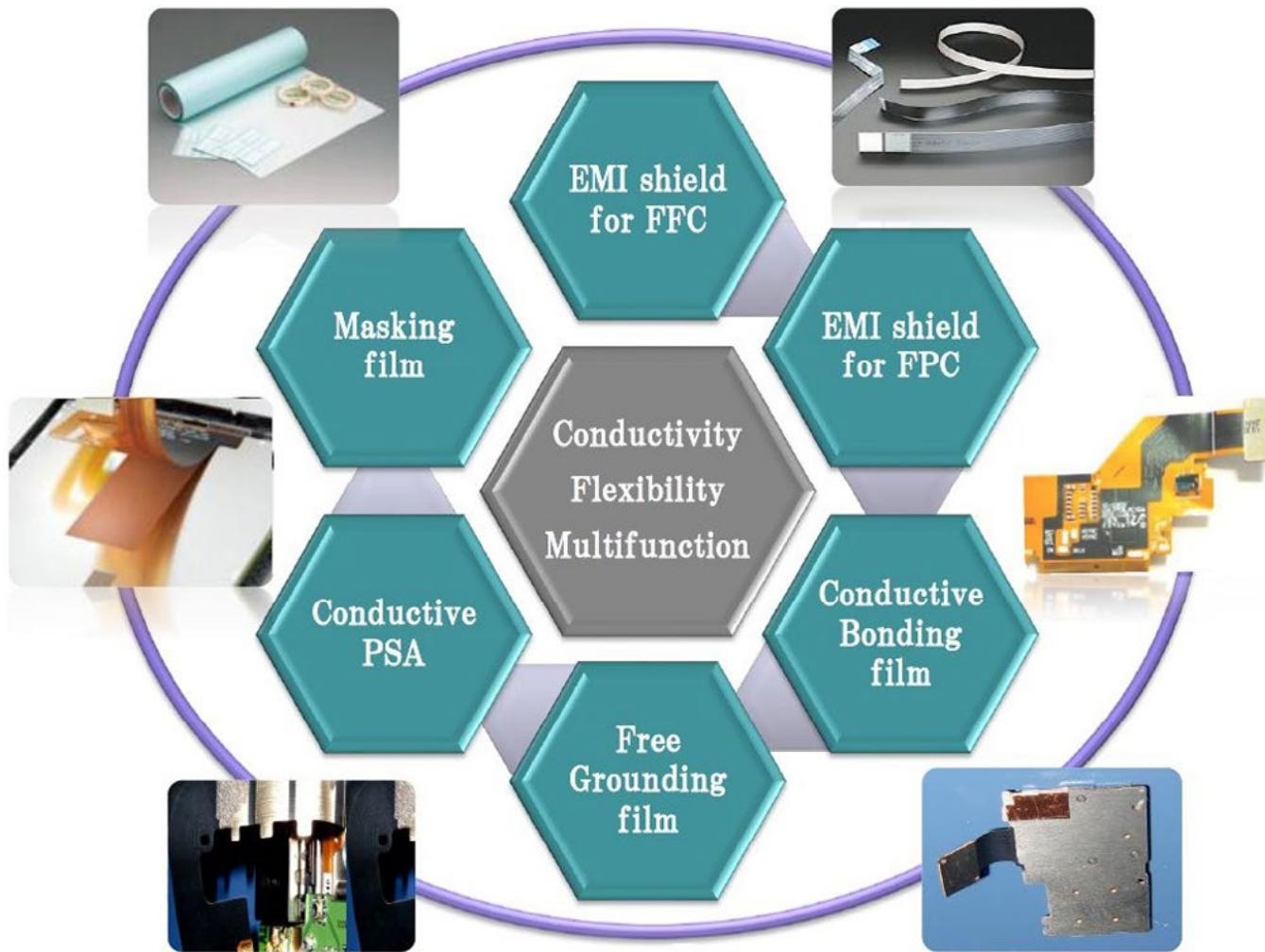
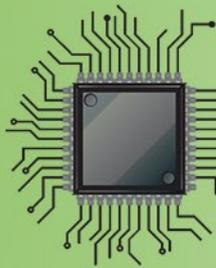


Figure 7: Tatsuta has developed and is making available to designers and producers a wide range of film type products in the areas defined above suitable for both rigid and flexible circuit construction and protection as illustrated.

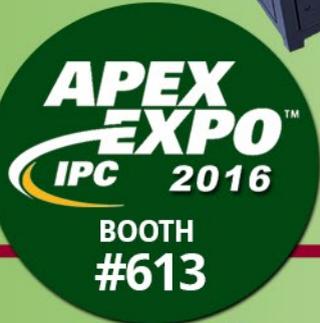


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## Areas of Product Design Presently Being Served

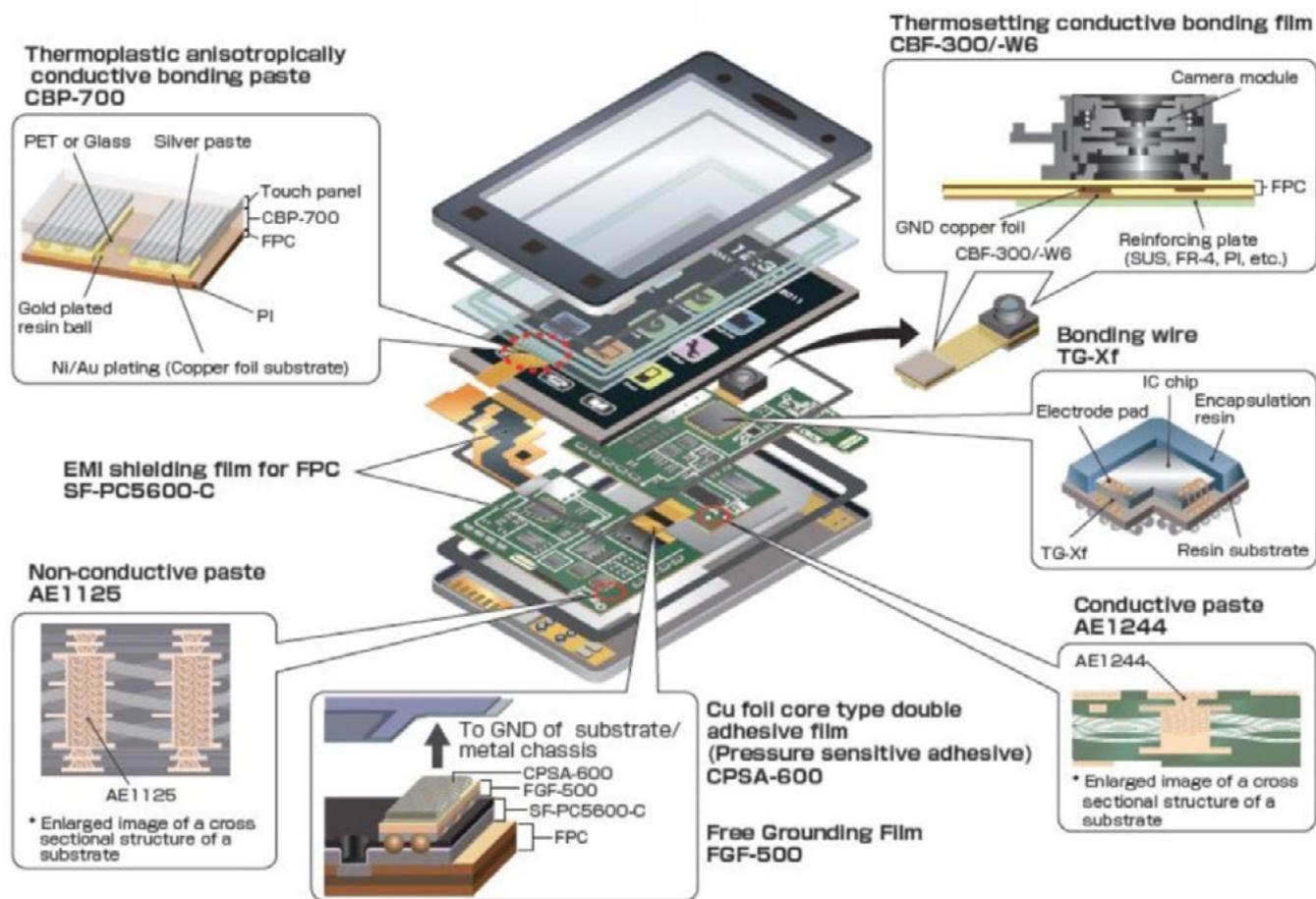


Figure 8: Illustrated are examples of the many important and enabling materials the company has developed. Also shown is how they are presently being used by current customers.

### Summary

The electronics interconnection industry is constantly being challenged by new designs and new design requirements. The set of materials in general use today are still suited for many applications but not all. New materials and processes are going to be required in the coming years. What has been offered to the reader is an opportunity to get a glimpse of some of the many new and enabling materials that are presently available and to appreciate better how they might be applied to present and future circuit design and fabrication challenges. How they might be used in some present design applications is illustrated in Figure 8.

### Acknowledgement

The author would like to acknowledge the assistance of Tatsuta GM Mike Sakaguchi in making available much of the technical content in this article. For more information on Tatsuta, [click here](#). PCB



**Joe Fjelstad** is founder and CEO of Verdant Electronics and is an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 150 U.S. patents issued or pending. To reach Fjelstad, [click here](#).



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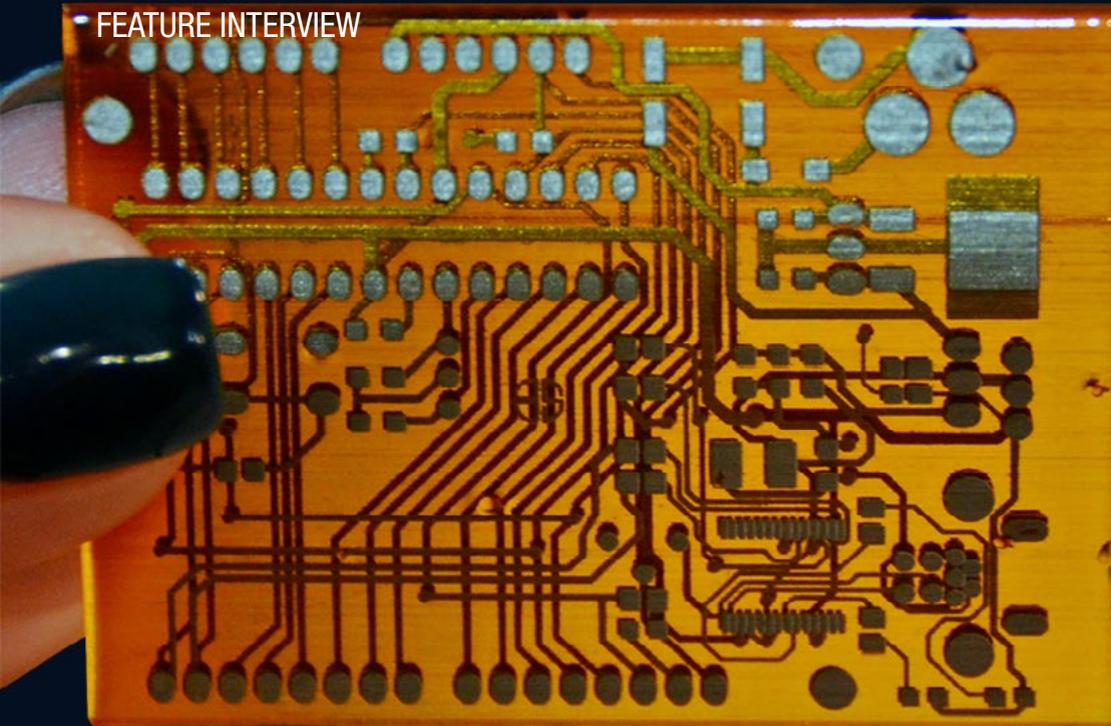
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# Printing PCBs... In Your Office!

*An Interview with Simon Fried by Barry Matties*

The days of producing a PCB prototype with a 3D printer may not be as distant as you think. I spoke with Simon Fried of Nano Dimension about how 3D printing is becoming a reality, and how this disruptive technology will change the way designers produce rapid prototypes.

**Barry Matties:** *Why don't you first tell us a little bit about what Nano Dimension does?*

**Simon Fried:** Nano Dimension is a company that is merging the worlds of printed electronics and 3D printing. It's taking printed electronics, which was a 2D space, putting conductor materials down onto films, and adding that additional material so that you can start building multi-layered circuits. What we've developed is a 3D printer that prints multi-layered PCBs right on your desktop in an overnight process.

**Matties:** *Obviously you're targeting the prototype market—people who just want to produce working prototypes in their office.*

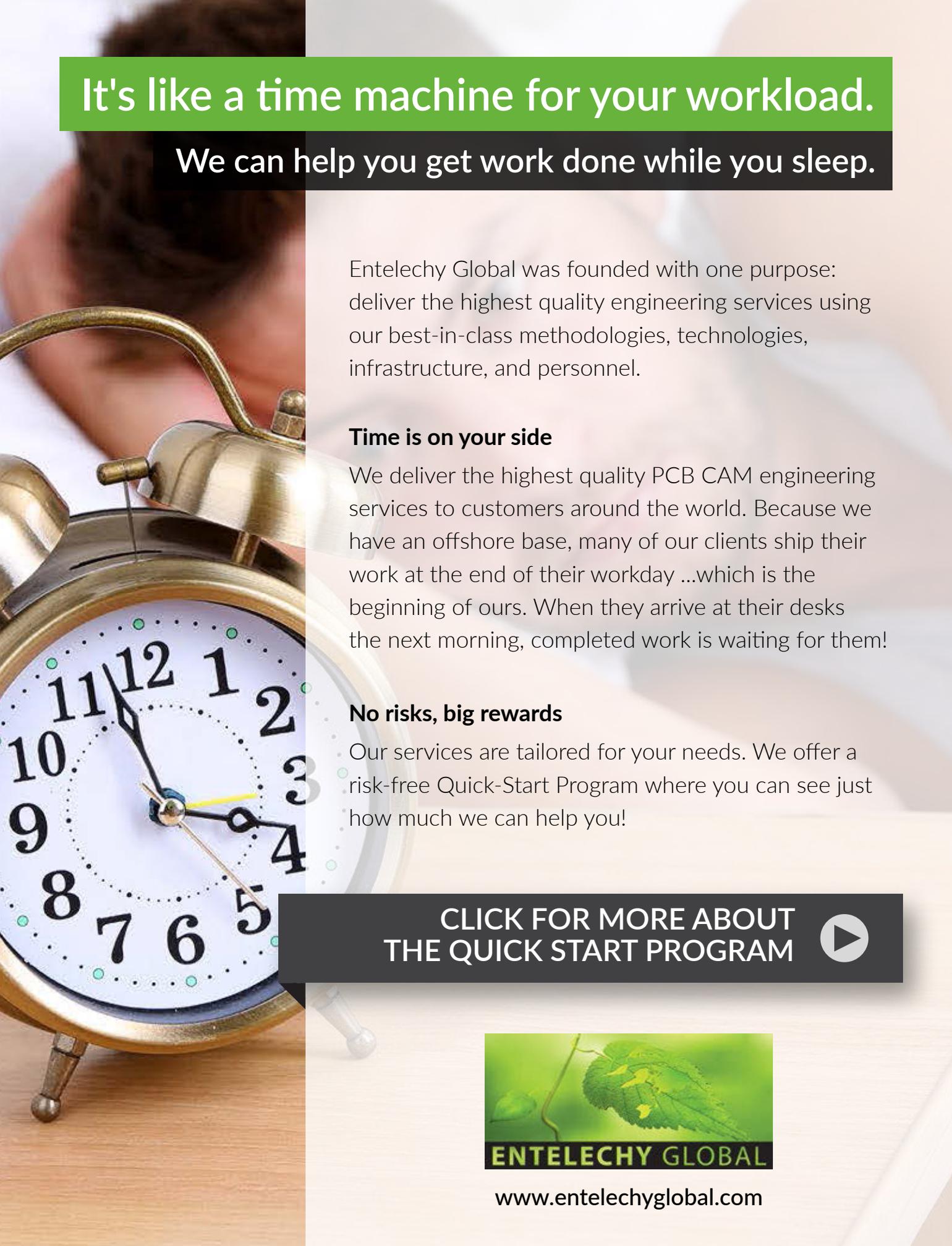
**Fried:** Absolutely. This is for that engineer who's developing a PCB who needs to do rapid devel-

opment, quick iterations, has a broad range of different PCBs, and can adapt on the fly to the developments as the development process progresses. It minimizes the risk of changing the PCB design. It allows you perhaps to be more innovative because you're not going to have to sit around waiting to find out if that great idea you just had is actually going to work.

It saves you time, it'll save you money, but it will also change the way that people work when they're developing PCBs. It'll allow you to do things that you otherwise wouldn't. If you compare that to the way 3D printing affected the prototyping of other objects, like engineering and design, what's happened in those spaces once 3D printing arrived is they did significantly more prototyping. They found that at the end they were getting better products more rapidly because exploration and innovation became that much easier.

**Matties:** *Now, with regard to the inks that you're using, is this proprietary ink?*

**Fried:** Yes, both of the ink materials are proprietary. We found that in order to get the perfor-



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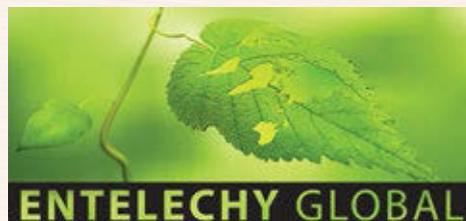
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Simon Fried,  
Nano Dimension.

mance that's required out of the PCB there are so many parameters from chemistry to print process that need to be very finely tuned. As a result we took it upon ourselves to develop the materials, printer, and software, all of which allows us to control every aspect of the process. That allows us to make the product at the end to the specifications required.

**Matties:** *How long have you been in business pursuing this?*

**Fried:** The company was founded in 2012 by a team of people who have extensive experience in the area of printed electronics and inkjet printing as a whole. It was bringing together various cutting-edge technologies in the materials space, but also in the printing space and also in the software area. All of those converged around 2012. Since then we've been bringing them together into this product.

**Matties:** *Is there a specific software requirement where they bring in their Gerber files, or how does that process work?*

**Fried:** We have as a goal to make it as user friendly as possible. We have a print job software that receives the Gerber files, including the drill and the route layer, etc. You can then double check before you send the item for print to make sure the stack is the way you want it. You hit print and that print job is then sent over to the printer. In that process it's actually converted into a 3D printable file, so the Gerber layers are actually turned into very thin slices, which the printer then lays down one at a time, building the PCB from the bottom up.

**Matties:** *Why don't you talk about the base material that you're using and how you build up the layers.*

**Fried:** Sure. The two materials are printed simultaneously. The dielectric material is something that we developed as almost like a liquid FR-4. It contains silica, and it contains polymers that give the strength, the rigidity, the dielectric performance, and also the temperature performance. The end result here is a polymer that can withstand 300°C, which means you can hand solder, you can reflow solder over the printed item at the end of the print.

That's a unique product that we've developed which works hand-in-hand with the silver. The silver ink has to have very strong adhesion to the dielectric, and they also have to behave firmly in the same way so you don't get cracks or splitting as it's exposed to the changes in the environmental temperature. Those two materials are very much married to one another. That allows us to put down the dielectric, and put down the silver material in such a way that you don't have to do any drilling. There's no drilling required. You print the vias and stack the silver all the way through.

**Matties:** *That's my next question: Where are the holes?*

**Fried:** As far as the printer is concerned, complexity doesn't matter. There's no such thing as complexity for the printer; it's just "Where do I put ink one and where do I put ink two?" If I need a vertical stack of silver, each time the print head goes by it puts a bit of silver in that place. If it keeps doing it in the same place repeatedly, it builds a stack. If you want to leave a through-hole you just tell the printer not to put anything there and it'll leave a through-hole. Blind or buried or open, it doesn't matter.

**Matties:** *This obviously is for prototyping, but would you expect this to go into production?*

**Fried:** We would love to see this kind of technology going into the production. It would certainly change everything. It would bring manufacturing back from the Far East and put it right back in the hands of the people actually developing electronics in the U.S., Germany or Japan. But that's something that's going to be a ways down the road.

**Matties:** *What's the greatest challenge?*

**Fried:** The challenge is the materials. We're using silver inks which are far too expensive for mass production. They're very price competitive if you're talking about the prototyping space where there's no set up, there is no waste, and it's on the spot. If you have very small batches of very complex PCBs, you might consider printing them this way. One-offs and prototypes by all means, but if you're talking about tens or twenties then you're already into a space where the traditional manufacturing approach is going to have a significant competitive advantage in terms of cost.

**Matties:** *Would someone need solder mask or some sort of coating for this?*

**Fried:** There's no need for the solder mask for two reasons. One is that when printing with silver, there's no oxidation issue at all, so that issue is removed. The other thing that we do is simply add another layer of the dielectric material on top, leaving the pads open. That's another step that we cut out. The only process that's happening here is depositing the dielectric and the conductive materials. At the end of it you have no drilling, no need for coating, and you have no post processing. It comes out of the printer and it's ready to go.

**Matties:** *What can someone expect to pay for the unit?*

**Fried:** The unit hasn't been publicly priced. We have a price goal of "less than \$200,000." A similar precision regular material enterprise inkjet 3D printer from the big players in the 3D space is normally a six-figure printer.

**Matties:** *If someone was to test the technology, how do they go about doing that?*

**Fried:** In terms of testing the technology, what we're doing is we're working with serious industry partners at the moment who will test them and make sure that for the purposes of a range of industries, whether it's aerospace, defense, telecom, automotive, it meets not only their needs in terms of specification, but also

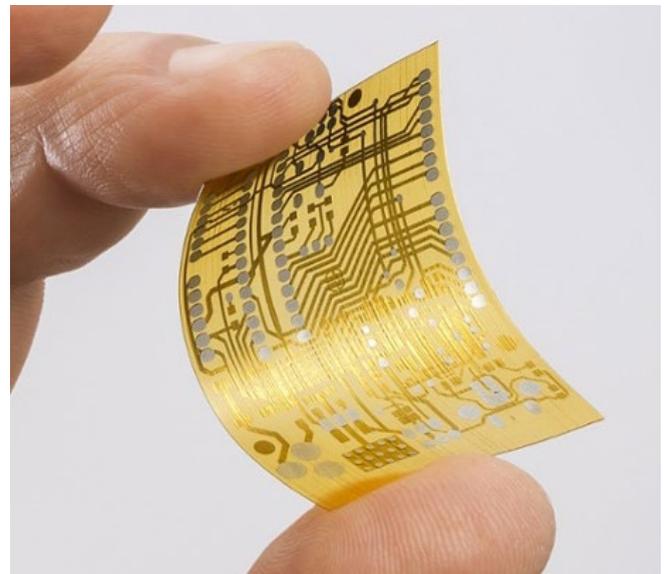
the ways that they work. Does it fit into their routine? Is the software user-friendly and is it comfortable? Is it intuitive, and so on? We must make sure of all those things before we launch the product. We'll be releasing information about case studies as time progresses for those that really want to get a more detailed insight into the end product.

**Matties:** *I think a lot of people would be extremely interested in that.*

**Fried:** Absolutely. It's a very conservative industry and it's a binary world that either works or not. The burden of proof is on us to make sure this thing works and that's precisely what we're doing.

**Matties:** *What's the response been to the technology?*

**Fried:** The response has been phenomenal. I think this is a clear example of a very applicable solution where there's a clear pain point in terms of the designers out there who are sitting around waiting for their PCB to get back so they can get on with testing. With the current pressures in terms of time to market, development cycles and minimizing the risk of making a change to a PCB, this is really a Godsend in terms of changing the way in which you go about innovating and progressing the product that you have in-



3D printed PCB from Nano Dimension.



Nano Dimension Dragonfly 2020 3D printer.

house. It also allows them to start thinking a little bit about the future, where you can start thinking about printing things that you currently can't even make. What if you want to play around with an offset via? Or you want to have a spiral interconnect? 3D printing really opens up a whole new world of opportunities and we're actually in an era now where things have been upside down. The software is lagging behind the hardware, which is not supposed to happen.

As things currently stand, if you look at the CAD systems out there, they don't actually have an answer for 3D design or 3D validation of design. There's an interesting period here where the software needs to catch up.

**Matties:** *Are you partnering with any software developers?*

**Fried:** We're certainly in touch with various software developers. We can't talk about any particular partnerships at the moment, but certainly what we're shining the light on is that there's an opportunity here to start looking at embedded or structural electronics in a way that hasn't really been possible before.

**Matties:** *Do you see traditional circuit board facilities putting this in and offering it as a viable option for their local designers?*

**Fried:** Without a doubt. If we look at the responses that we've had from potential users, we have everything from the R&D labs of the large

organizations that you'd expect, the educational institutions, and designers who want to be able to offer that final mile of actually delivering the PCB to their customers. Actually, one of the first very early pre-orders that we got was from somebody who said, "What I want to do with this is set up a service center." This is for somebody who doesn't want to have to deal with stencils and the interruptions in order to get that prototyping work, because it's an annoyance. The shops don't want to deal with this; they just want the big order at

the end of the day. If you can have a few printers around the shop dealing with those multiple changes in stencils, it takes all of that hassle out of the system and you can focus on dedicating your actual production to those bigger jobs.

**Matties:** *Well this is exciting—congratulations. Is there anything that we haven't talked about that we should share with the industry?*

**Fried:** We're planning to initiate our pre-sales of the system probably early 2016 in Q1 or Q2. There will be a limited number that we're able to produce initially. We're beginning to fill the order books as of January. People that are looking for earlier delivery rather than later delivery should be getting in touch.

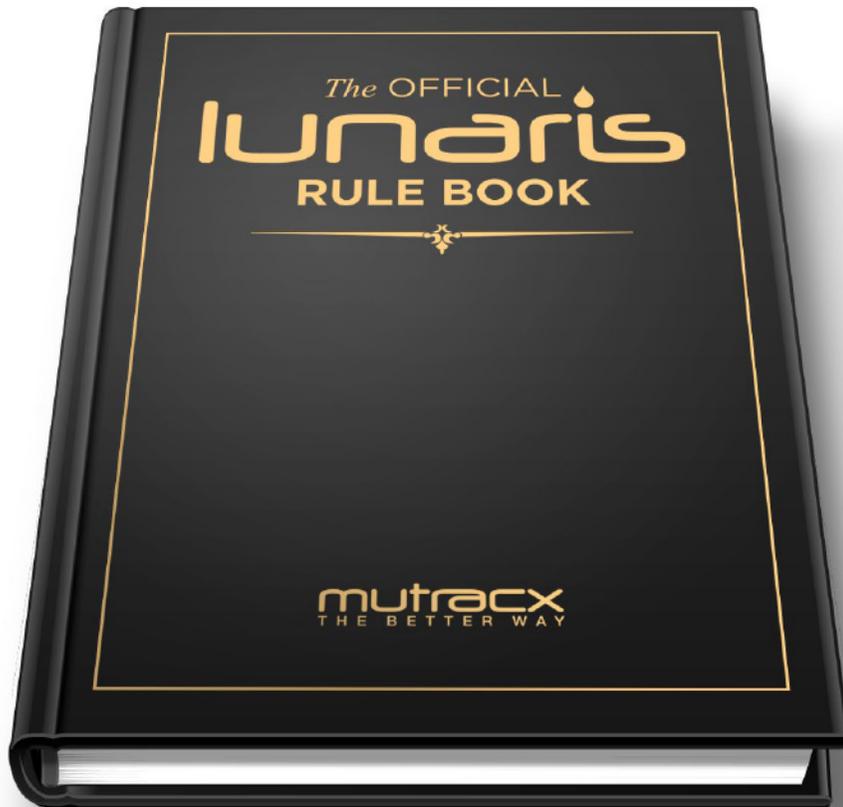
**Matties:** *You are based in Israel. What about U.S. distribution? How are you handling that?*

**Fried:** We're beginning to speak to the usual distributors of inkjet 3D printing systems. There's a very established market that's able to not only distribute, but also give excellent maintenance and support for precisely this kind of system.

**Matties:** *I certainly appreciate your time today, this is great.*

**Fried:** My pleasure. It was kind of you to swing by. **PCB**

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## **PCB Technologies Receives NADCAP Accreditation**

PCB Technologies announces that it has received Nadcap accreditation for Electronics.

## **A Conversation with IPC President and CEO John Mitchell**

I-Connect007's Patty Goldman was able to sit down with John Mitchell, president and CEO of IPC, to discuss the organization and where we are going as an industry. We discussed IPC's four aspirational goals—standards, education, advocacy and solutions—as well as short-term goals. We also talked a bit about going virtual and becoming paperless.

## **Raytheon's Development and Testing on Track for DDG 51 Flight III**

Raytheon Company announced its AN/SPY-6(V) Air and Missile Defense Radar (AMDR) team has completed the first full radar array, fully populated with component Line Replaceable Units (LRUs), including more than 5,000 Transmit/Receive elements, in 140 days.

## **NUS Takes the Quantum Leap into Space**

Galassia, a two-kilogramme nanosatellite, was developed by students and researchers from the Faculty of Engineering; Centre for Remote Imaging, Sensing & Processing (CRISP); and Centre for Quantum Technologies (CQT).

## **Highly Efficient, High-Speed Technology for Satellite Communications**

A group including University of Tokyo researchers used 64 APSK, a highly efficient signal modulation technology, to successfully demonstrate 505 Mbps communications with the Hodoyoshi-4 nanosatellite, the highest communication speed

yet achieved with an earth-observation micro satellite. This high-speed communications technology will be of great value to future generations of earth observation micro satellites of under 100 kg.

## **Innovative Designs, Smart Manufacturing Deliver Soldier Readiness**

"The Army has called for increased innovation, which is shining a spotlight on prototype designs," said Christopher Manning, Prototype Integration & Testing Division chief, under the Army's Communications-Electronics Research, Development and Engineering Center, or CERDEC. "However, it is imperative that our designs can be leveraged for mass production and sustainment."

## **Northrop Grumman to Design and Produce Shipboard Laser Weapon System Demonstrator**

The U.S. Navy will get a peek at a future where high energy laser weapons could defend its ships against attack under a contract awarded Oct. 22 to Northrop Grumman Corporation by the Office of Naval Research (ONR).

## **Indium Features Gold-Tin Solder Preforms for Precision Die-Attach Applications at AeroDef2016**

Indium will feature its precision gold-tin (AuSn) solder preforms for die-attach at the upcoming AeroDef 2016 event in Long Beach, California. Designed for high-reliability applications, Indium's Pb-free and RoHS-compliant AuSn preforms are available in a variety of standard and custom-engineered designs.



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# Copper Via-Fill Technology in Development

by Tara Dunn  
OMNI PCB

The use of via-in-pad technology is increasing rapidly in today's PCB designs. The need for miniaturization, combined with the rapidly decreasing pitch of component footprints, drives printed circuit board designers here. Via-in-pad requires the vias to be filled, planarized and then over-plated with copper. Once a designer has decided to move forward with this technology, the next question to be answered is what type of fill material should be specified. Typically, these vias are filled with either epoxy, conductive epoxy or solid copper plating. All have pros and cons to be considered.

I recently spoke with David Ciufu, program manager for printed circuit board technologies with Intrinsic Materials, to learn about an exciting new product in development that will

dramatically change the existing manufacturing parameters of the filled-copper via option.

Intrinsic's nano copper has been formulated into a screen-printable paste that is compatible with commercial via-fill equipment. This paste can be dried and sintered in commercially available ovens and results in pure copper after sintering. The end-product is highly conductive, both thermally and electrically, when sintered.

## Benefits

Now, for the exciting part, there are two distinct advantages for PCB manufacturing with this product. First, because it is run with commercially available equipment, as seen in Figure 1, the capital investment needed to offer copper-filled via technology is significantly re-

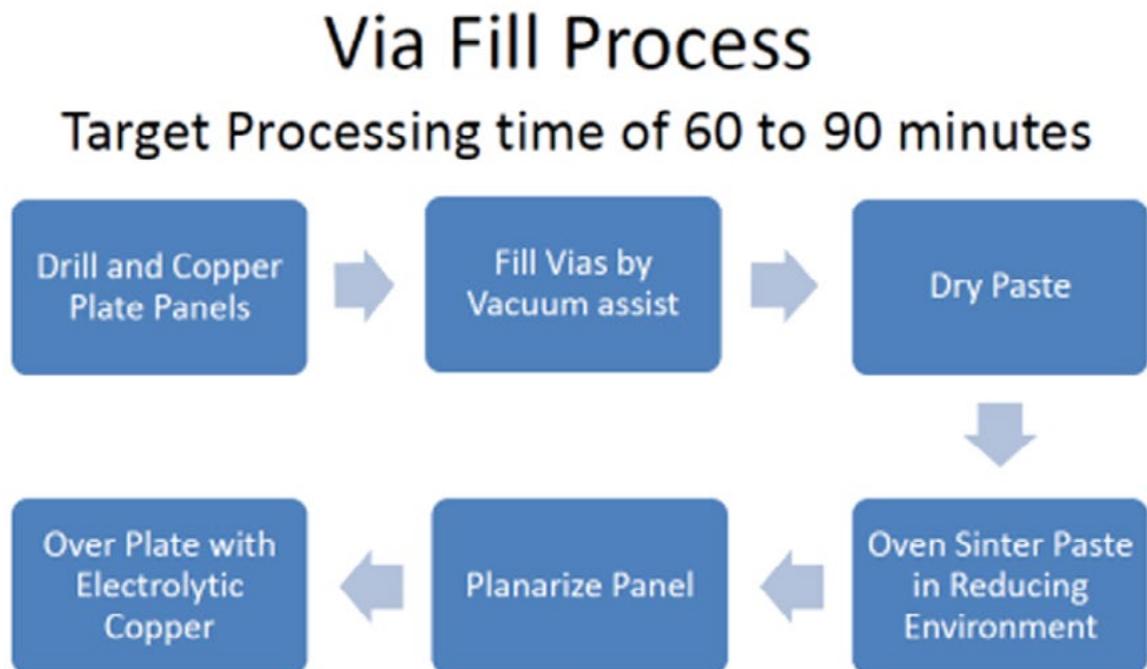
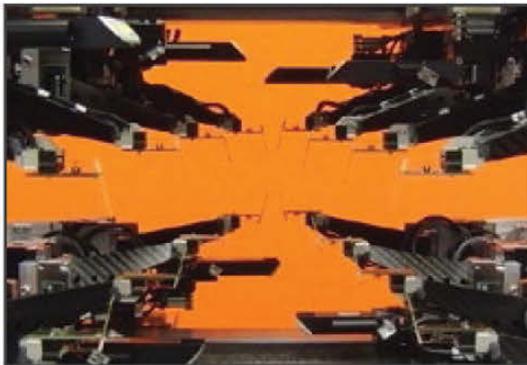


Figure 1: Copper-filled via process completed with standard PCB equipment.

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duced. Many printed circuit board manufacturers are not able to offer the copper-filled via option due to the cost of plating equipment and chemistries. The barrier to entry for these PCB manufacturers will be eliminated.

The second exciting benefit to this technology is the process time requirement. Solid copper-plated vias typically require 4–6 hours of plating time by the manufacturer, along with the specialized equipment and chemistry. This new product will enable PCB manufacturers to produce copper-filled vias in 60–90 minutes. A shortened cycle time will have benefits in lead time and processing costs.

Product release for this screen printable paste is currently scheduled for the end of 2016. Throughout this year, pilot programs will be released, further testing completed and reliability data gathered.

### **Product Development: An Interesting Process**

Nano copper inks and pastes are typically sintered photonically with broadband (xenon) flash or near-IR laser. Because the copper cladding is too thermally conductive to allow complete sintering and high-power lasers are a barrier to entry due to cost and complexity, an oven solution was sought to keep the process compatible with existing technology. Heller Industries manufactures a formic acid environment convection oven to be used for flux-less reflow. This was determined to be the perfect environment to sinter nano copper without oxidation. Nano copper paste can be completely sintered in 40 minutes or less.

The process development for this product has had several iterations. The initial proof of concept was to deposit paste into mechanically drilled blind vias using a vacuum bag to help fill the holes. Those initial coupons were plated and etched prior to filling to allow for laser sintering. As the development progressed, the testing moved to copper-clad PCBs with mechanical blind vias. The panels were electroless copper-plated then electroplated to simulate actual via filling requirements. Unfortunately, the thermal conductivity of the copper foil prevented the ability to sinter the copper paste. Research then pointed to thermal sintering in a formic acid environment.

As the development process continued, it was determined that the extended time necessary for formic acid sintering at 250°C destroyed the PCB laminate. Moving forward, other nano additives were included in the formulation to lower the temperature requirement to 225°C. This formulation and temperature sintered the vias completely in 60 minutes.

The next phase in the development process was to screen print trace patterns on FR-4 to be sintered alongside the via-filled coupons. These samples were used to calculate bulk resistivity as compared to copper. Typical measurements were 6–8x that of bulk copper. Typical epoxy-based conductive via fills are in the 20–50x range.

### **Today's Product**

Moving forward, additional product development was undertaken resulting in the current formulation, which allows the sintering temperature to be reduced to 190°C. The paste is sintered to pure copper in only 40 minutes in the Heller conveyor oven. Samples of this formulation were via-filled using the vacuum bag technique, on copper-clad panels, with copper-plated blind vias. The panels were Heller sintered, planarized, over-plated and solder floated. Samples were then subjected to IPC standard reliability testing parameters. Each sample was floated at 288°C, held at temperature for 10 seconds, cooled, and refloated four times. The vias survived five solder float procedures.

It is always exciting to learn about the new developments in products and processes for the PCB industry. In this case, incorporating nano copper inks and pastes into standard printed circuit board manufacturing techniques will allow manufacturers to offer a solid copper-via option to their customers without significant capital investment in specialized plating equipment. **PCB**



**Tara Dunn** is the president of Omni PCB. To contact the author, or see past columns, [click here](#).

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# CAMTEK TAKES INKJET TECHNOLOGY INTO THE FUTURE

**by Barry Matties**  
I-CONNECT007

I recently spoke with Amir Tzhori, vice president of the PCB (AOI) division of Camtek in China, about the current and future status of their solder mask and legend inkjet technology, Gryphon. Also, with automation so instrumental, we discussed a new automated robotic arm that can be attached to their AOI systems.

**Barry Matties:** Amir, let's start with a little context about Camtek and what you do.

**Amir Tzhori:** Camtek develops and manufactures state-of-the-art inspection and metrology systems for the semiconductor and PCB markets. The business is being run by two separate divisions. Recently, the PCB division entered into the inkjet technology with its Gryphon, a full digital manufacturing station designed for PCB solder mask and legend deposition. The Semi and the PCB divisions share a technological-driven synergy, while within the PCB division we maintain a market-driven synergy between our AOI and Inkjet product lines.

**Matties:** There's a real move to inkjet in circuit board fabrication on a lot of different levels, like the solder mask system you guys brought out recently. Where do you see inkjet headed? Right now it seems to be in what I would call its infancy state.

**Tzhori:** Personally, I believe that this will take the market; it's just a matter of time. Whether it's going to be through Camtek or somebody else, and whether it's going to be this year or five years from now, printing technology will come to the PCB industry in the future. As well as other industries like touch panel or even semiconductor, because it eliminates complex, very expensive and long processes.

However, at the moment we depend on the technology of the printer heads, which we don't develop. The more they evolve, the better we will be able to adapt our technologies to a thinner line and space.

**Matties:** So the print heads are really the gating factor?

**Tzhori:** Actually, it's a combination of the system itself—the ink, the formulation of

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the ink, the print heads, and the surface preparation. All of this should be integrated perfectly. This is why Camtek decided to develop the ink, although this is not our core business. We believe that without mastering the ink itself and having the ability to tweak the formulation of the ink and play with the print heads and the surface preparation together in one system, it will be impossible to just buy the ink and print it.



Amir Tzhor, vice president PCB (AOI) division of Camtek, China.

**Matties:** *If someone purchases your system, are you the only ink supplier, or do they have a choice?*

**Tzhor:** At this stage, Camtek is the sole ink supplier, but this is not our intention. We understand that the market will look for companies that specialize in consumables. We are talking to everybody, and everybody is talking to us. We believe that once we are ready we will achieve a commercial advantage with the big players.

After completing a very aggressive marketing and promotional step, we are now at phase two, which is centered on qualifying the process. We have several installations worldwide and all our efforts are focused on passing these customers' qualifications and eventually their customers'.

**Matties:** *We're sitting here in China, where speed is a very big issue.*

**Tzhor:** It's a very big issue, and although we are exploring mass production solutions, at this stage we are not competing on the mass production lines. We know that we have to pass qualification of our customers and the end-user, and those qualifications are for small batches with quick turnaround. We want to be introduced to the market with as wide a customer base and

end-user base as possible, but the current system is mostly suitable for quick turnaround and high-mix, low-volume needs.

**Matties:** *So, this equipment is well-suited for Europe and North America at the moment?*

**Tzhor:** Yes, it's suitable for what we call mass production in North America and Europe, but it's also very suitable for a Chinese market. There are a few high-mix, low-volume producers in China, and one of them is currently going through the qualification process for our system. Secondly, we believe that any mass production producer would want to have one or two of these systems in order to reduce its production cycle time. The advantage that we have compared to the traditional process is an overall cycle time improvement for batches of less than 15 panels. So, although we are slightly slower in the actual printing, we are much faster in overall cycle time.

This is because we are offering a solution with fewer stations—neither exposure units nor developers are needed in the solder mask and legend processes because we're printing solder mask and legend in one station. We don't need to move the panel around. Final curing is half the final curing of the current process. If you are a mass production producer and you want qualification done by your customer, you don't need to use your high volume mass production to send the panel to your customer to be qualified. You use the Gryphon SL, ship it out in 24 hours, pass qualification and then move the order into your mass production line.

We discussed this concept with many of our customers and everybody likes the idea and everybody wants to try it. Actually, we have more demand than we wished for at the moment. We want to tightly control the amount of installations at this stage and focus on qualifying the process and only then deploy the technology to the rest of the market.

In addition, we are successfully experimenting with zero clearance and printing in clearances smaller than 100 microns; adding those capabilities to our existing system will open new opportunities and new markets for this amazing technology by allowing the Gryphon

users to offer their customers unparalleled competitive advantage.

**Matties:** *That sounds like a prudent move. There's no reason for getting it out there and then having recalls or issues of any kind. You want it to work perfectly.*

**Tzhori:** Exactly. It's also about selecting the right customers. We had a year to plan, we chose carefully the strategic partners to work with. We believe that the market is waiting for them to qualify the process. Again, unlike AOI where we have been a big player for many years, we're not selling just a system but rather a full process, therefore the qualification process is much longer. It's not only about whether the system is doing its job or not, that's not enough. It's the process that needs to be qualified from start to finish. We need to pass UL approval for the process, not just for the system or the ink.

**Matties:** *I was recently at Bay Area Circuits in California, one of your qualification sites, and they're quite proud to be doing this.*

**Tzhori:** We are also very proud of the technology. We believe that this is the future and that we are on the right track.

**Matties:** *I believe so too. Moving to your AOI, you've obviously been a strong player in that market for many years and I've seen your products all around the world. In fact, I was recently at the Whelen facility in New Hampshire and saw your equipment there.*

**Tzhori:** It's an amazing facility.

**Matties:** *But what I notice here at the HKPCA show is you have a robotic arm now in front of your equipment.*

**Tzhori:** Unlike employees the robot doesn't ask for a salary raise every year, and the average turnover in China is very high. We are a very strong believer in automated systems, but ours is the only system on the market that has kept the original design with the ability to support back and front, loading and unloading.

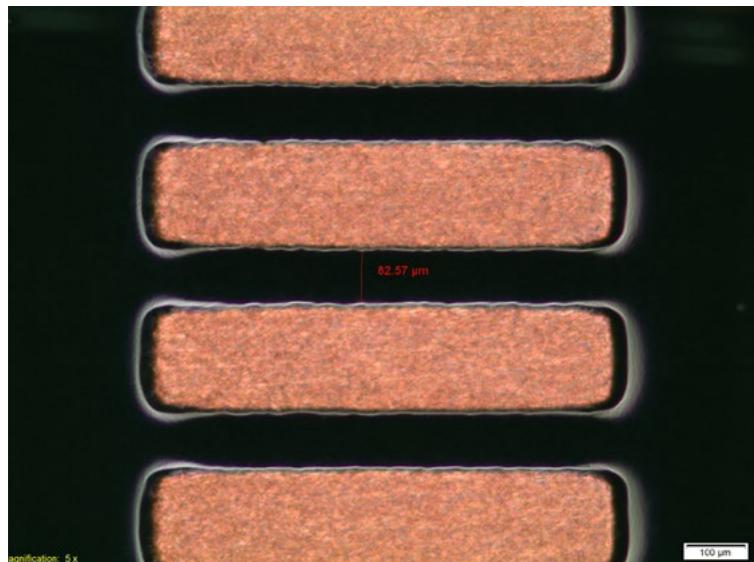
The rest of the market has moved to systems with a smaller footprint. We believe this is the future and we are a bit ahead in terms of our anticipation that the automation concept will be accepted in the market. We are not there yet, but it's coming. The new robotic arm is a new technology in that market.

**Matties:** *Is Camtek building the arm?*

**Tzhori:** No, but we are cooperating with somebody else in a joint venture, you could say. It's not a commercial joint venture, but a technology joint venture. We share our knowledge with them and they share their knowledge with us, and we try to improve the product together. It's much the same as the printing technology, it will take the market but it's just a matter of time. Also, here in China the automation technologies keep on improving. The robotic arm that we're showing here is, in terms of speed, comparable to a human for loading and unloading at around four to five seconds. Until now it wasn't like this, as automation solutions usually were a bit slower.

**Matties:** *Is the arm capable of going into any facility and adapting to your existing systems?*

**Tzhori:** Yes, it's very easy. There are a lot of different possible configurations, but we are show-



Gryphon printing sample, top view.

ing only the basic configuration here. Everything in China needs to be in harmony so it's a harmonious solution.

**Matties:** *What's an arm like this run for in terms of cost? Is it comparable to the salary of an employee?*

**Tzhor:** No doubt it's the equivalent or even better. The ROI is less than one year. The robotic arm can work 24/7 with no downtime, whereas the operator needs three shifts with three different operators, so no doubt the return on investment is immediate. It's just a matter of accepting the future and the change.

**Matties:** *I think here in China they're embracing it, because they realize labor cost is a factor and they have to drive it down to keep their business. So if a board doesn't pass inspection, does the arm move it to a separate stack or how does that process work?*

**Tzhor:** That is a possible option, but there are several different scenarios. You can install an automated marker on the system, so the system will mark the defects and then the robot will load the perfect panels to one pile and the defective ones to a different pile.

**Matties:** *It's speaking to the machine, which is all part of Industry 4.0, right?*

**Tzhor:** Yes. The beauty of this is that it's customizable, so we have different customers that run different scenarios and with this we easily adapt to each.

**Matties:** *In my mind, I don't know why board shops wouldn't just put a robotic arm in front of these machines to begin with, even in a quick-turn shop.*

**Tzhor:** Looking at it from a shop perspective, I would go for it anywhere it's an option. It doesn't matter if it's one system, two systems, or 50 systems. Again, the reason it wasn't there yet is because the robotic arm technology is only now reaching the phase where they are equivalent to the speed of a Chinese worker. They are very fast and very efficient.

**Matties:** *Well congratulations, it really looks like some great equipment here. I was impressed when I first saw your Gryphon system at APEX earlier this year, and it was a nice surprise to then see it in action at Bay Area Circuits.*

**Tzhor:** It's a great achievement. I don't want to take the credit as I wasn't the one involved in developing this.

**Matties:** *Well, it's a company-wide effort.*

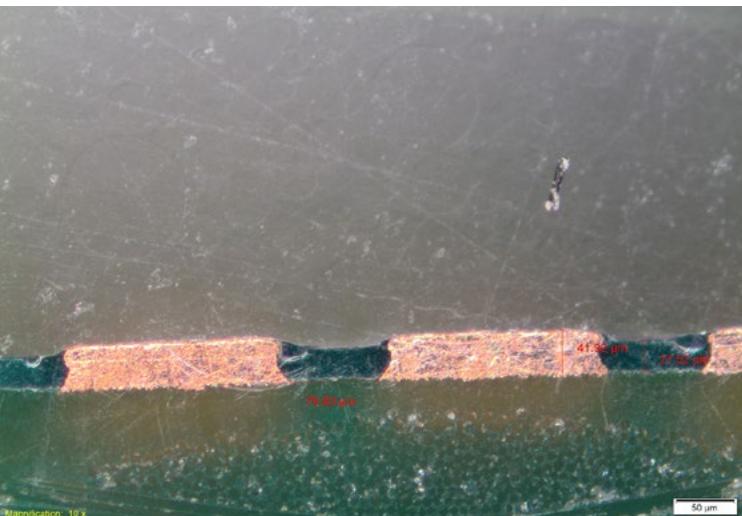
**Tzhor:** I agree, but no doubt the people who engineered and developed this solution are an amazing group of people.

**Matties:** *I was at the Printed Electronics USA show in Santa Clara recently, and there was a guy with a machine there, four feet by three feet, sitting on a table, printing out complete prototype circuit multilayer boards.*

**Tzhor:** Yes. It was also an Israeli company?

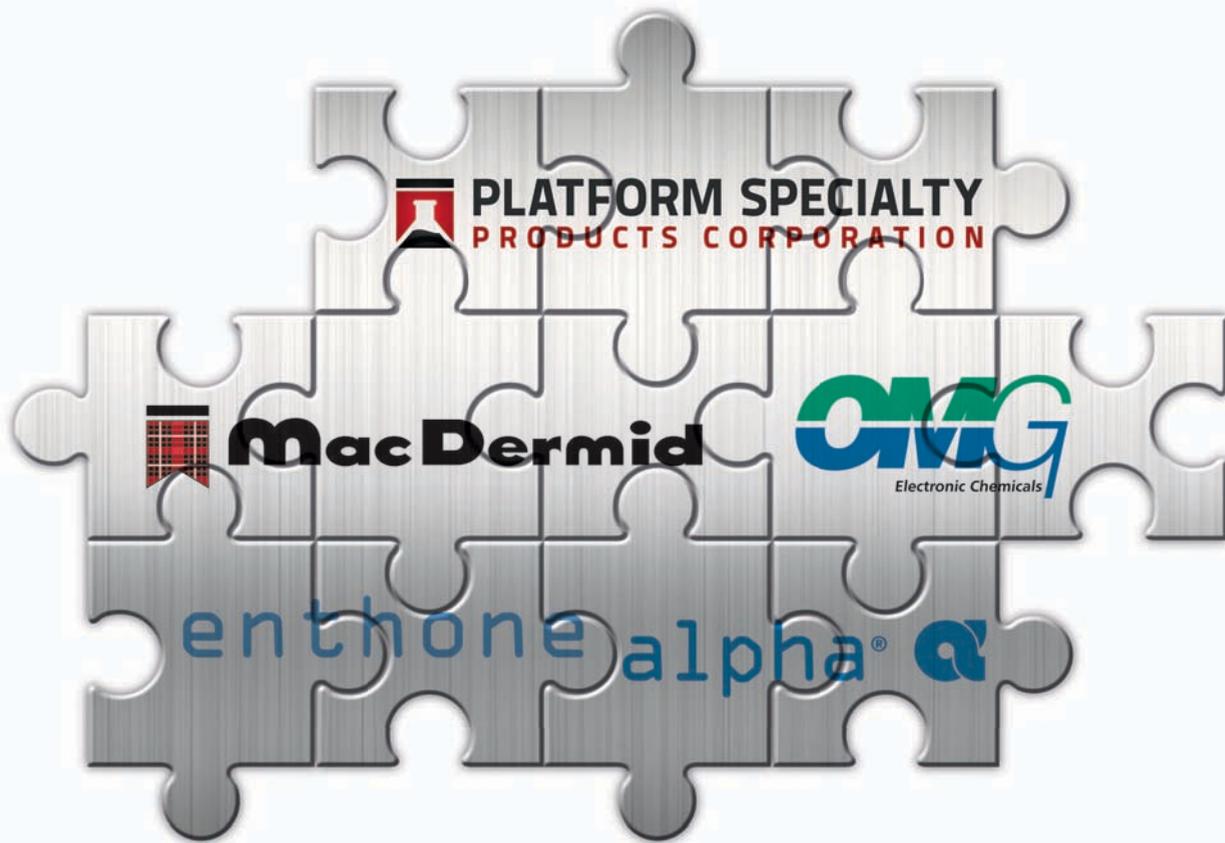
**Matties:** *Yes, do you know this company?*

**Tzhor:** Yeah, we know the company. Everything is close enough that everybody knows everybody. I'm not familiar with the technology, but I don't believe it's a competing technology.



Gryphon printing sample, cross-section.

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Gryphon.

**Matties:** *It's not competing but it could be disruptive, for sure, in a number of years.*

**Tzhor:** Theoretically, yes. But the challenge for them—as far as I can see, and maybe I'm missing something—is much bigger than the challenges we are facing in terms of qualification. We are now struggling with qualifying the solder mask, which is only just the cover layer. For their technology to become commercial they would need to qualify the entire structure. This means the entire material, the conductive lines, everything. It's a huge challenge and even to pass all of the stress tests it's going to take years of effort to be qualified.

**Matties:** *I may be wrong, but I'm thinking in 15 years we're going to be printing our circuit boards.*

**Tzhor:** I agree with you. As I said before, printing is going to take most of the existing processes, but it is really dependent on the printer heads, the chemistry, the size of the drops, the materials, and so on, not the PCB industry. It is improving, but what we don't know and won't know is how fast. I'm not a chemist, and I'm

not an expert in the printing industry, but you can see that this is one of the industries that keeps on innovating and actually we can print almost anything now.

**Matties:** *It's a really exciting time in this industry; I've been in it for more than 30 years and back then it was all manual. There's been a lot of equipment change, like AOI and things like that, but there hasn't been a lot of actual process change, and we're right on the verge of seeing a lot of changes that you're talking about.*

**Tzhor:** One thing you can see is that the semiconductor and PCB industries are getting closer and closer to each other. Some of the semiconductor equipment producers are stepping down towards the IC substrate market, and the IC substrate producers are trying to shrink their technology to wafer level packaging. In the semiconductor industry there is no doubt a different level of innovative technologies, and I think this relationship is going to change the PCB industry as well.

**Matties:** *I think so too.*

**Tzhor:** It's also true for us. Actually, most of our high-end AOI equipment is being equipped now with a metrology solution that comes from the semiconductor AOI solution. We are no longer selling AOI to only scan traces. We are doing traces and then we are doing 2D and 3D and all kinds of other metrology measurements. So the tool is being used as a production tool, but also as a QC and process improvement tool.

**Matties:** *If we're not improving the process, what's the point? When we look at the high-reliability markets like medical and automotive, inspection and the cost of inspection is not even an issue. They have to have it because many manufacturing processes just aren't stable enough to not inspect when the cost of failure is so massive.*

**Tzhor:** You can see those are two drivers for increasing inspection demand. It used to be capacity, but you don't see a lot of capacity. The

PCB market actually didn't grow this year—it shrank a bit—so you don't see a big capacity demand, only for new factories. But in terms of technology, there are a lot of demands. The big smartphone producers are pushing for 100% inspection. It wasn't there on the flex boards and it wasn't there in the laser via application. They didn't demand it. They don't only focus on the quality of the product itself. Regardless of the quality, they demand 100% inspection.

You also see an additional trend that is related to liability. The end-users are pushing the smartphone producers to push down the liability in terms of failure. So the entire food chain is trying to protect themselves. The only way to protect yourself is to provide reports that you did 100% inspection and attach the report showing that it's not you, but somebody else in the food chain.

One of the challenges for us is that we usually sell our AOI equipment to the production managers. What we're trying to educate the market about is the QC tool, and that salespeople need to be involved. What we provide now is automated reports that are being generated from a complex database that allow you to attach a report saying, "Okay, look, for this batch I measured the copper thickness on a specific coupon that the customer designed, and the copper thickness is fine, the critical dimension is fine, and I proactively attached a report."

So what we're trying to do is work with QC and also with the end user. We have a long relationship with some big end users, and they are actually approaching the PCB producers and saying, "Okay, you have to do 2D or 3D measurement and provide me the report on every batch that you send back."

**Matties:** *How do you see the marketplace coming up in 2016?*

**Tzhori:** Obviously there is a slowdown in China, over the economy. The PCB industry, specifically the 4G infrastructure, will slow down. I don't know if it's my feeling or based on my experience, but I feel that we are in the bottom now and the market will recover in China. The U.S. is doing relatively okay. Japan is doing so-so. They're moving a lot of production away



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from Japan to Southeast Asia, but not to China. The Korean market is very soft, but I believe it's just a matter of time until they really recover. So overall I think 2016 will be better than 2015, but marginally. It's not going to be a big jump.

**Matties:** *If you look at this show and the people that are here, the activity is good; it looks like equipment is being sold, and the energy is positive. It's not like the crash of late '90s.*

**Tzhori:** No doubt the energy is positive. Also in terms of our business, 2015 was much better compared to 2014, and our focus for 2016 is even better so we don't see any slowdown in our business. We also will take some market share from our competitors, based on technology, and so we feel very comfortable about next year.

**Matties:** *Amir, I appreciate you spending time with us and sharing what's going on here. Thank you so much.*

**Tzhori:** Sure, thank you very much. **PCB**

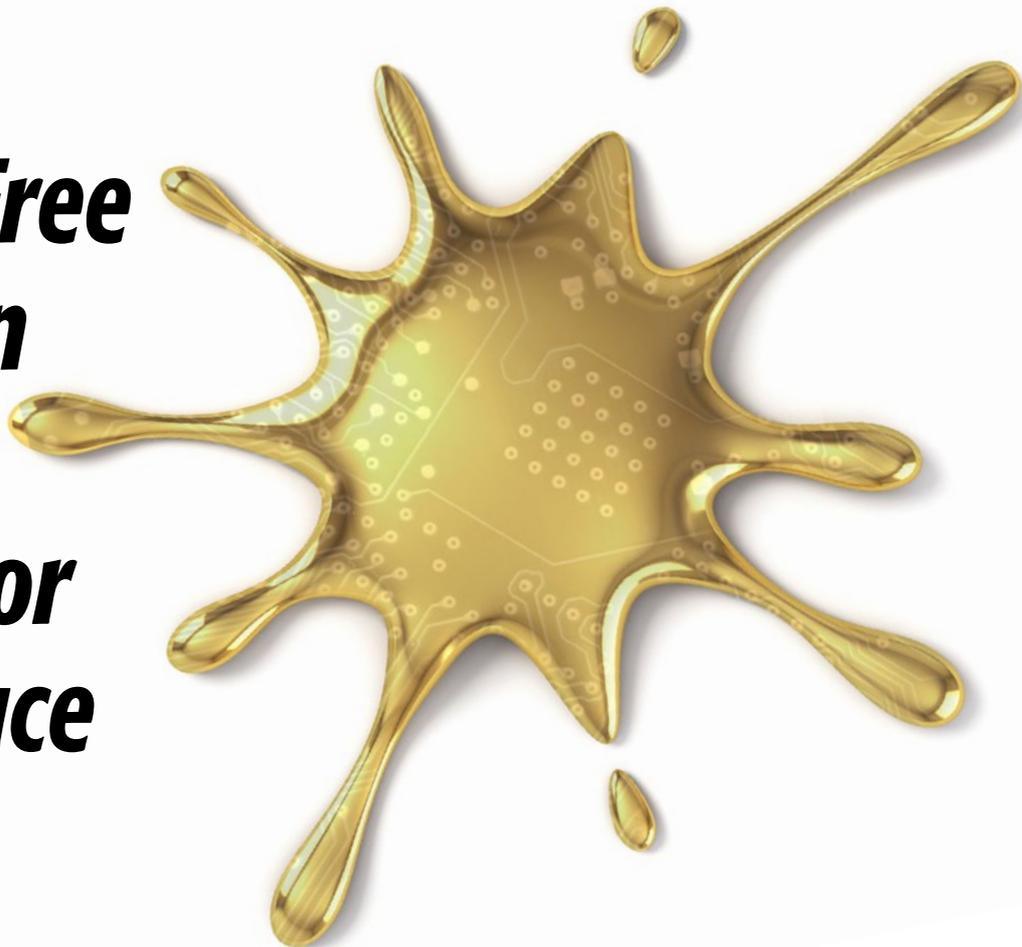
# Cyanide-Free Immersion Gold Suitable for PCB Surface Finishing

by Jun Nable, Ph.D.; Emely Abel-Tatis; Ernest Long, Ph.D.; John Swanson; and Martin Bunce  
MACDERMID INC.

## Introduction

Among the most utilized PCB surface finishes is gold. Gold has been used in conjunction with other metals such as Ni and/or Pd underneath to provide a solderable surface finish<sup>[1,2]</sup>. The metal undercoat is commonly applied via an autocatalytic electroless process while the gold top coat can be immersion deposited.

Immersion gold plating has long been used in the electronics industry as a surface finish because of its excellent solderability and its ability to resist corrosive substances. Most conventional immersion gold plating solutions utilize a cyanide containing gold salt as the gold precursor which poses environmental and health concerns. Besides the health and environmental concerns, most cyanide-containing baths are operated at temperatures of about 80°C or above. A cyanide-free gold plating solution that does not consist of any harmful and toxic substances would be an attractive alternative.

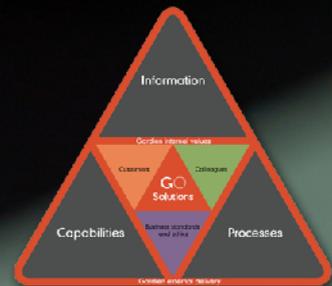


In this paper, we introduce an immersion gold plating process suitable for ENIG surface finishes that utilizes no cyanide-containing reagent and operates at near neutral pH and 40°C. The performance is evaluated to check its suitability as a surface finish.

## Plating

One of the unique features of the cyanide-free immersion gold chemistry is its ease of operation. The operating temperature for this gold bath is 40°C while still achieving a plating rate of 0.2  $\mu\text{m}/\text{min}$ . The operating pH is close to neutral pH. The plating rate can be maintained consistently throughout the entire bath life with proper pH control.

In all the plating shown below, the average electroless nickel thickness is 150  $\mu\text{m}$  while the gold thickness was targeted at a minimum of 2  $\mu\text{m}$  in 10 minutes of gold plating. The plating rate curve from 0–12 mto is presented in Figure 1. The rates are considerably steady throughout the entire bath life staying within the range of 0.2–0.24  $\mu\text{m}/\text{min}$ . This plating rate is satisfactory for the processing of immersion gold for the ENIG finish which targets about 2  $\mu\text{m}$  of gold within 10 minutes of processing time.



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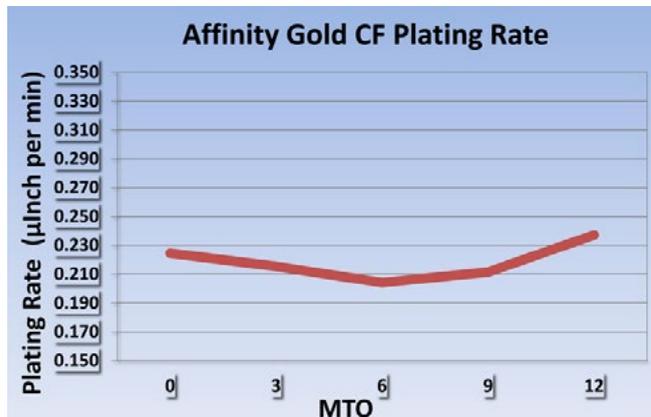


Figure 1: Plating-rate curve throughout the entire solution life.

**Corrosion Investigation**

Cross-sectional FIB image results are presented in Figure 2. None of the samples showed corrosion damage in the electroless nickel layer. There were no visible black pad spikes that had

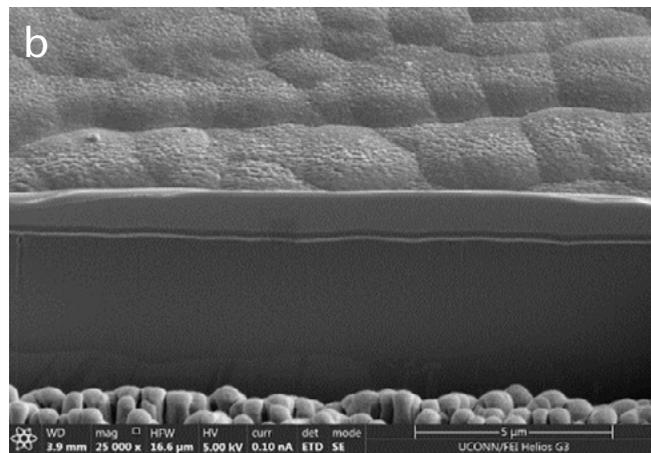
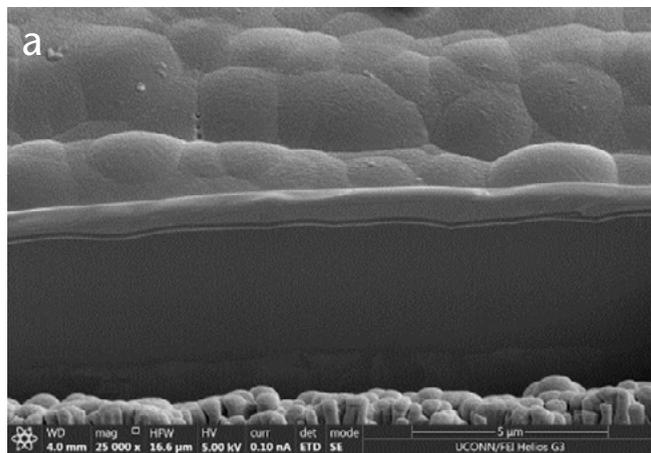


Figure 2: Cross section FIB images of the ENIG finish investigating for black pad corrosion (a) 0 mto and (b) 12 mto.

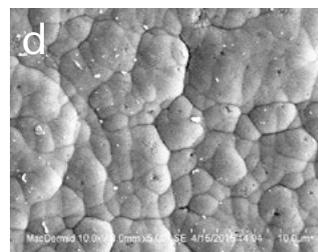
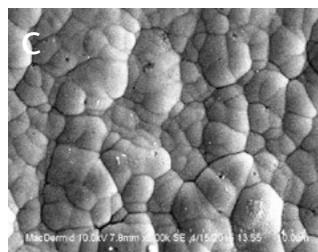
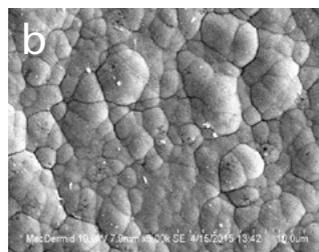
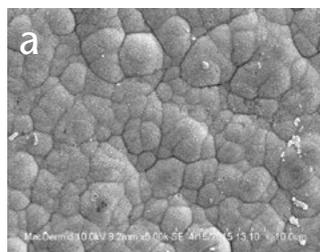


Figure 3: SEM image of the surface after stripping the gold layer (a) 0 mto (b) 4 mto (c) 8 mto and (d) 12 mto.

penetrated into the electroless nickel region.

Furthermore, surface corrosion by stripping off the gold layer also revealed no significant black pad attack (Figure 3). From these images, the underlying nickel layer is relatively intact. Surface damage is limited to very small pits on the surface of the grain and not along the grain boundaries. Conventional cyanide-containing gold plating would normally corrode along the grain boundaries and penetrate through the entire electroless nickel layer.

**Solder Performance**

The Pb-free solder performance of the ENIG finish are presented in the following section.

The through-hole fill result is shown in Figure 4. All of the samples had exceeded the IPC requirement of 95% fill. The thermal reflow had no detrimental effect on the solder hole-fill. In fact, samples that had been subjected to 2x thermal reflow have the same hole fill result as freshly plated samples.

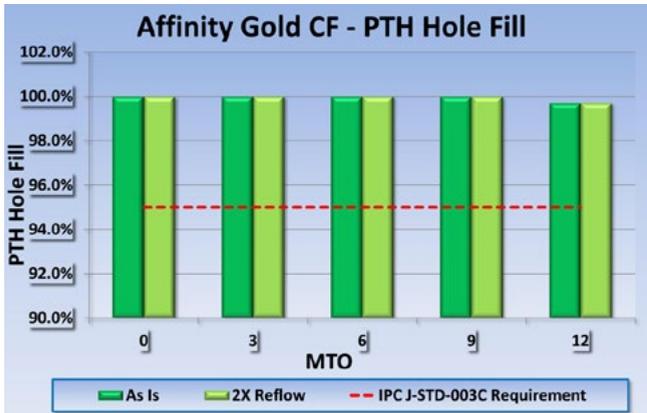


Figure 4: Pb-free solder PTH hole fill results from 0–12 mto.



Figure 5: Solder spread results from 0–12 mto.

Solder spread is another useful metric for solderability. This test is a measure of how well the solder would wet over an area of the surface finish. Fresh solder paste is applied onto a feature design with the original area noted. After thermal reflow, the size of the solder area is evaluated against the size of the initially applied solder paste. The solder spread is then calculated based on how much area the solder paste expanded to.

The solder spread result from 0–12 mto is illustrated in Figure 5. The graph shows as-plated samples and after 3x reflow samples. The 3x reflow is to simulate the ENIG surface finish undergoing several thermal exposure cycles. Even after the thermal excursion, the solder spread is still excellent. The reflow did not have any detrimental effect on the solder spread of the surface finish. The solder coverage area of both as-plated and after 3x reflow have increased up to 600% for all of the mto sets.

### Wetting Balance

Another measure of solderability is by wetting balance. This technique measures the wetting force between the molten solder and the surface finish as a function of time. The instrument records the time and force for the solder to wet the pad. This method is considerably sensitive and quantitative. Figure 6 shows the compilation of the wetting balance results.

The plots on the left column show the wetting for as-plated samples from 0–12 mto while

the plots on the right column are the samples after going through 3x reflow. There is a discernable difference before and after the 3x reflow. Freshly plated samples have relatively closer wetting curves whereas after 3x reflow the individual measurement curves are more scattered apart. This scatter indicates some of the plated component pads within the same sample have slightly deteriorated leading to loss of wetting. Despite the scatter, all the wetting balance results are still considered acceptable. The  $T_{zero}$  is similar for all cases, which is less than one second.

### Solder Joint Integrity

The solder joint integrity is determined by shear test. In this specific test, solder spheres are placed and assembled onto a defined area or a suitable pad feature such as ball grid arrays (BGAs). Once the solder sphere had been placed and soldered in place, a shearing arm that is part of the shear instrument would push the solder sphere until the sphere gets dislodged. A schematic of the ball shear test is illustrated in Figure 7.

The solder spheres used are also Pb-free. Solder paste is initially applied followed by placing the solder spheres at the designated pad. Once the spheres are in place, the entire panel is reflowed to melt and form the solder bond between the surface and the solder materials.

A shearing arm will push the formed solder sphere until the sphere dislodges from the pad.

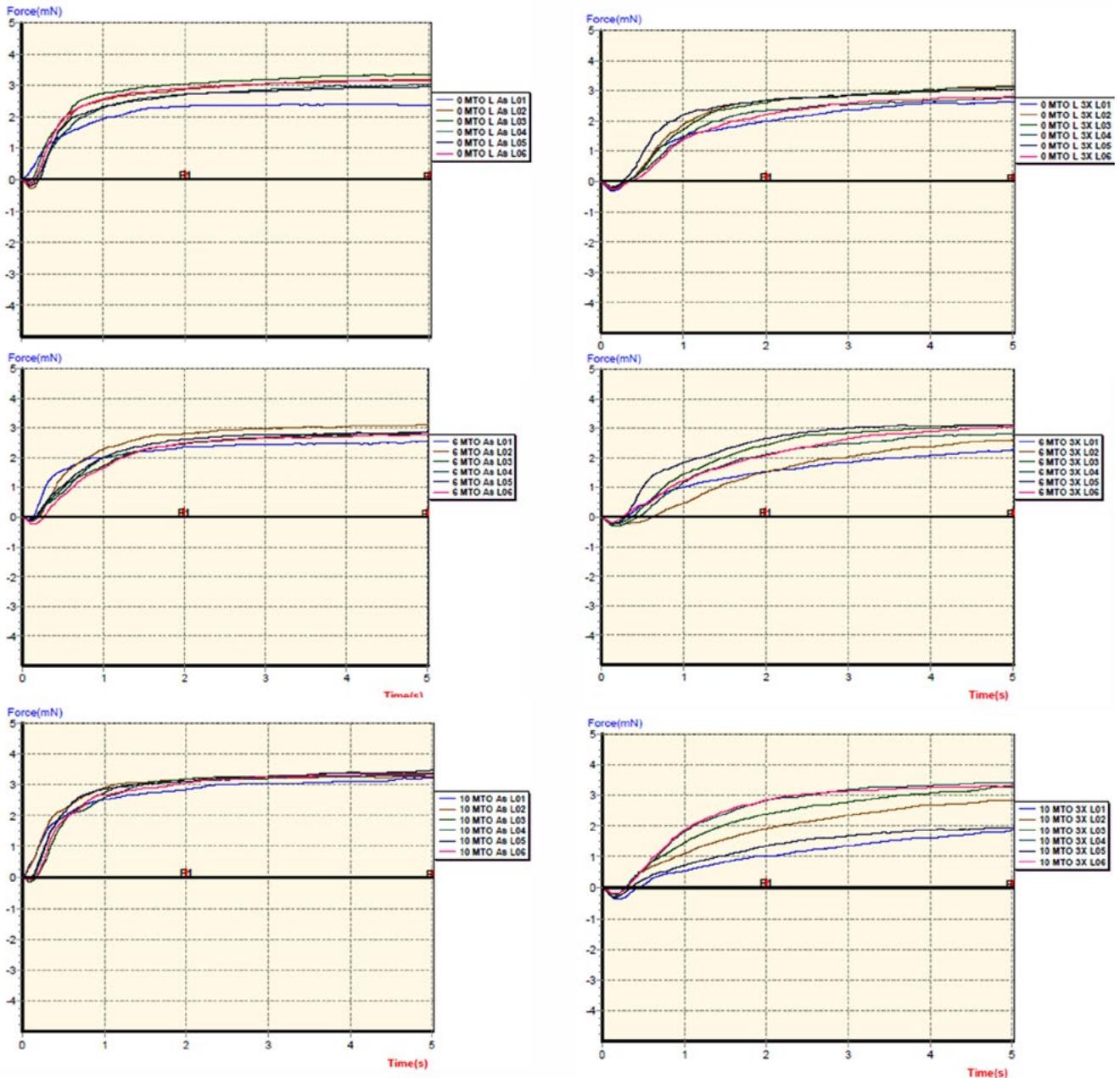


Figure 6: Wetting balance from 0–12 mto. The left column depicts as-plated samples and the right column is after 3x reflow.

The force required to remove the sphere is used as an indication of the solder joint strength. The higher the force required to dislodge the solder sphere, the stronger the solder bond is between the surface finish and the solder.

Two types of pad features are used in this ball shear test. One type of pad is the metal-defined pad while another is the solder mask

defined pad. It's worthwhile to differentiate the two pad features because it affects the solder shear integrity. Figure 8 illustrates the main difference between the two pad features. Metal-defined pads are features on the panel that are shaped or made up of the substrate metal itself, whereas solder mask defined pads are features shaped by the solder mask. In the latter case, a



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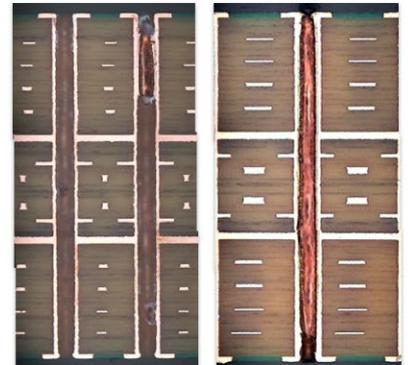
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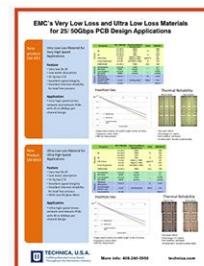


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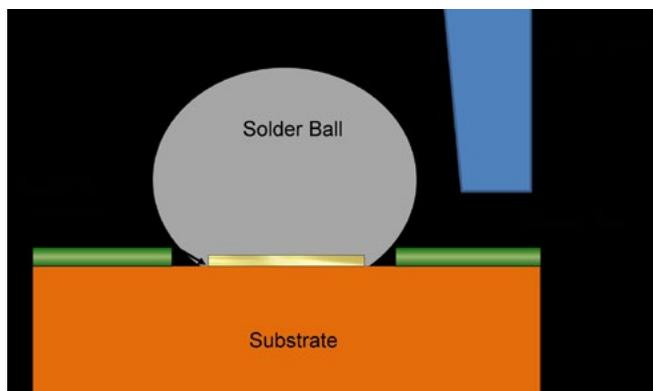


Figure 7: Schematic of a ball shear test.

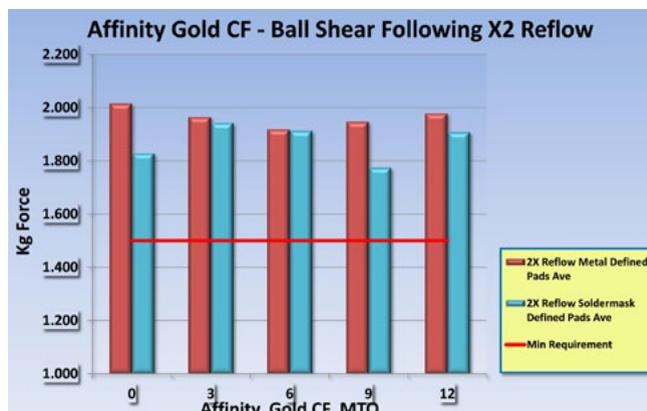


Figure 9: Ball shear test results from 0–12 mto for both metal defined (red) and solder mask defined (blue) pads.

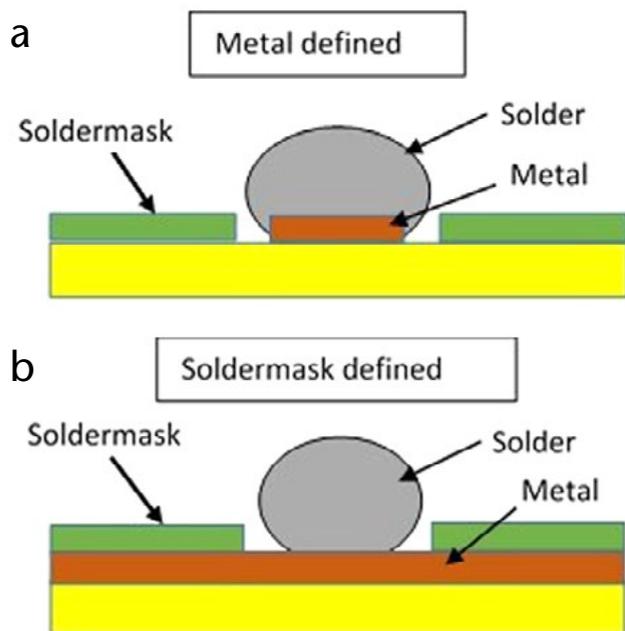


Figure 8: (a) Metal-defined vs. (b) solder mask defined pads.

single large pad can serve as the substrate metal for numerous solder mask-defined pads.

Figure 9 reports the ball shear results for 0–12 mto samples that had been subjected to 2x thermal reflow. All samples have exceeded the minimum required shear strength of 1.5 kgF. Most metal defined pad exhibited an average shear strength of 1.9 kgF or above while solder mask defined pads are slightly lower with a minimum of 1.8 kgF for the 9-mto sample set.

It's noteworthy to point out that the shear strength of solder mask defined pads are lower than the metal-defined pads for all of the mto sets. As exemplified in Figure 8, the solder for metal-defined pads also cover the side area of the entire pad when the solder bond is eventually formed. This added coverage also contributes to the increased bonding surface between the substrate and the solder leading to higher bond strength. However, the solder mask defined pads do not have the additional contact area for the solder to hold on to.

Another important key piece of information obtained from the shear test is the failure mode of the solder joint. The most desirable failure would be the ductile shear mechanism wherein the failure occurs within the bulk solder material and not along any of the interface region. Failure along the interface area would indicate a weak interaction between the interface materials. A break within the solder would indicate that the solder bond between the finish and the bulk solder is intact and not a weak point. Figure 10 shows two sample images of ductile failure using the new cyanide-free immersion gold in ENIG. The failure mode is the same for a newly prepared bath and near the end of bath life. The break shows solder material is still left on the surface when the solder spheres are completely dislodged.

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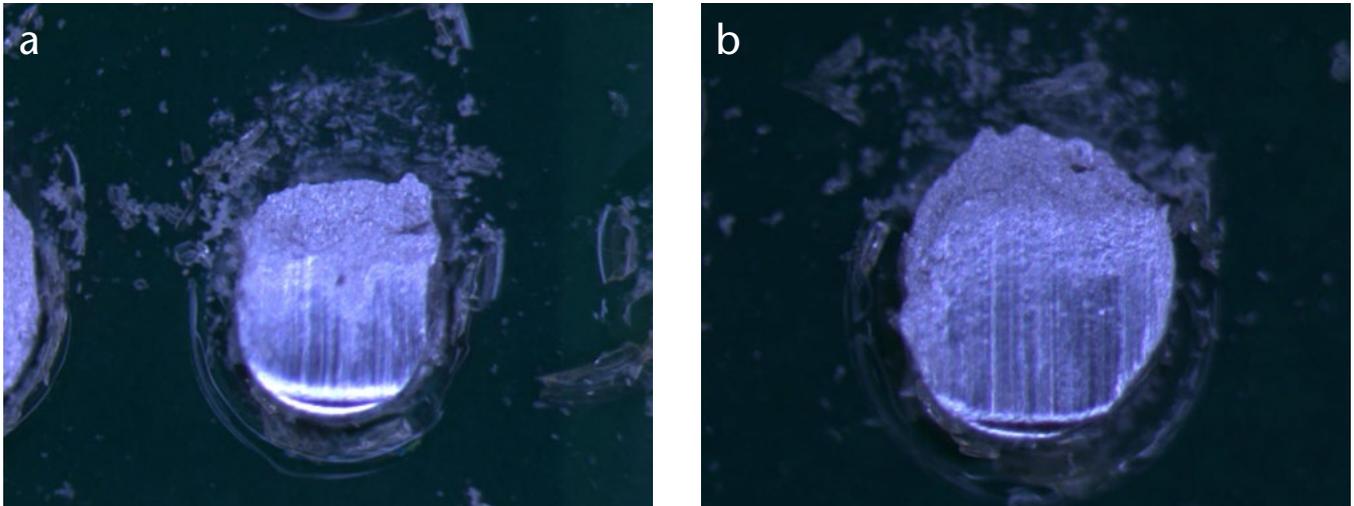


Figure 10: Images of the ball shear failure mode showing the preferred ductile failure mechanism for a new bath (a) 0 mto and at the end of bath life at (b) 12 mto.

**Conclusion**

A new cyanide-free immersion gold plating process is presented. The plating behavior and performance results in this study have shown to be suitable for ENIG. The corrosion caused by the displacement reaction to plate gold onto the underlying nickel layer is very minimal. The gold plating bath is very stable and gives a consistent plating rate throughout its bath life. The solderability tests have met or even exceeded IPC standard requirements.

The exclusion of cyanide from the plating chemistry makes it more environmentally friendly and lessen any potential toxic cyanide health hazards and risk to the user. Beside the health and environmental benefits, this cyanide-free gold allows a much lower operating temperature of 40°C, leading to better energy savings.

**Acknowledgement**

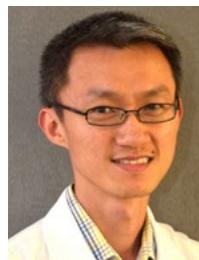
The authors would like to acknowledge the assistance of Paul Romaine and Ron Szulis for providing the electroless nickel plating and conducting some of the sample preparation and evaluation. PCB

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2. Mallory, G.O., Hajdu, J.B., Electroless Plating: Fundamentals and Application, New York: American Electroplaters and Surface Finishers Society.

*Originally published in the proceedings of SMTA International 2015.*



Jun Nable



Emely Abel-Tatis



Martin Bunce

*Authors:*

**Jun Nable, Ph.D.** is research project manager; **Ernest Long, Ph.D.** is director, research; **Emely Abel-Tatis** is chemist; **John Swanson** is director, final finish; and **Martin Bunce** is global application specialist—all with MacDermid, Inc. For more information, [click here](#).

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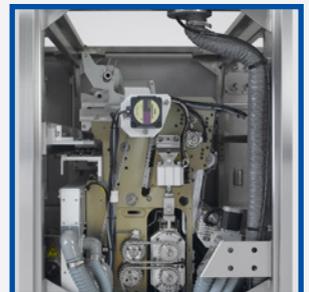
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# Supply Lines Highlights



## **Ventec International Group and TMT Trading Announce Intention to Merge**

Ventec International Group, a world leader in the production of polyimide and high reliability epoxy laminates and prepregs, announced the intention to merge with TMT Trading GmbH, a leading distributor of PCB base-materials including consumables and flex- and rigid-flex circuit board materials.

## **Plasma Etch to Hold Live Plasma Cleaning Demonstration at MD&M West 2016**

Plasma Etch Inc., a leader in plasma treatment, will be providing live demonstrations of the company's popular PE-50 Plasma Cleaner to attendees at the Med Tech World MD&M West 2016 trade show. The show runs February 9–11 at the Anaheim Convention Center in Anaheim, California.

## **OEM Applications: MacDermid's OEM Director Embraces Renewed Focus**

Lenora Toscano, OEM director for MacDermid's electronics solutions division, discusses the needs of the end-user market of PCBs, her own role at the company, which involves much interaction with OEMs, and the benefits that both she and MacDermid bring to SMTA and IPC meetings.

## **Insulectro Hires Laminate Expert Leena Gulia to Join Silicon Valley Sales Team**

Insulectro, a leading distributor of materials for use in the PCB and printed electronics industries, has hired former Isola OEM sales manager Leena Gulia as a technical sales manager in Insulectro's Silicon Valley operation.

## **Ventec to Unveil New 'tec-speed' Brand for High-Speed/Low-Loss Materials at DesignCon 2016**

Ventec International Group, a world leader in the production of polyimide & high-reliability epoxy laminates and prepregs, will exhibit in Booth 118 at DesignCon 2016, where the company will launch a new brand identity, tec-speed, for its high-speed/low-loss product line. With the launch, Ventec will unveil a new logo, marketing collateral and technical specifications.

## **Isola Names Jeff Waters President and CEO**

Isola Group, a market leader in copper-clad laminates and dielectric prepreg materials used to fabricate advanced multilayer PCBs, announced today that its board of directors has appointed Jeff Waters as president and CEO, effective immediately. Waters succeeds Interim CEO Jeffery McCreary, who was brought in to enable leadership continuity after Ray Sharpe's retirement in August 2015.

## **Bay Area Circuits Adds Accu-Score AS-100-MAX V-Scoring Machine to its Silicon Valley Facility**

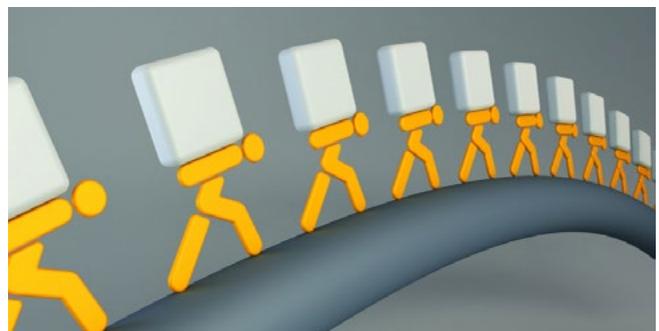
"This purchase is a part of our initiative towards investing in equipment which not only improves our manufacturing quality and precision but also reduces cycle time," said Stephen Garcia, President of Bay Area Circuits.

## **CCI Eurolam Group Expands Market Reach**

The CCI Eurolam Group, for more than 30 years, has been the distributor of Pacothane products in many of the key markets in EMEA. We are pleased to announce that from January 2016 the territories that CCI Eurolam Group will handle on behalf of Pacothane Technologies LLC has been expanded to include the UK, Benelux, Scandinavia and Switzerland.

## **Nano Dimension Files Patent for Printing Multimaterial 3D Objects**

Nano Dimension, a leading printing electronics company in the area of 3D printing, announced today that Nano Dimension Technologies, a fully owned subsidiary of Nano Dimension, has filed a patent application with the U.S. Patent and Trademark Office for the printing of 3D models, which includes electronic conductors.



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## **Ventec Europe Accredited to AS9100 Revision C**

We are proud to announce that the quality management system at our Leamington Spa, UK, headquarters is now fully accredited to AS9100 Revision C (the two facilities of our parent company, Ventec Electronics Suzhou Co Ltd, have been fully AS9100C certified since 2012).

AS9100 is the quality management standard specifically written for the aerospace and defence industry, to satisfy authorities such as the Federal Aviation Administration, ensuring quality and safety in the "high risk" aerospace industry.

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# THE NEXT STEP: Technology That's Driving Smaller Microvias

by **Osamu Sekine**  
NANO SYSTEM INC.

The trend for laser-drilled microvias keeps moving toward smaller diameters for higher-density PCB design. Along with the smaller microvias, demands for laser-drilling technologies will begin to shift further from CO<sub>2</sub> laser systems to UV laser (3<sup>rd</sup> and possibly 4<sup>th</sup> harmonics UV DPSS lasers) or combination tools such as UV/CO<sub>2</sub> dual laser systems. Our team sees the current needs within the U.S. marketplace heading towards modular platforms allowing for upgrades as technology shifts to reduce capital costs for companies operating within the U.S.; such upgrades include precision optics, faster scanning technology, and new laser wavelengths and properties, as well as material handling needs.

There are continuous demands of laser-drilled microvias on PCBs from smart electronic devices, or products that fall within the realm of the Internet of Things (IoT). Smart electronic devices require implementing and integrating various types of PCBs such as HDI boards, pack-

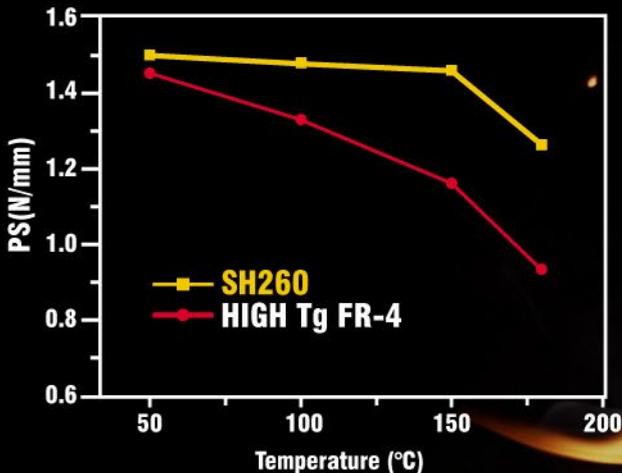
aging substrate boards and/or flexible circuit boards within limited space in a flexible layout. CO<sub>2</sub> laser systems have been considered the main tools to produce 60–100 mm diameter vias on HDI or packaging substrate boards because of the strong advantages of high throughput and effective cost. Flexible circuit board fabrication has mainly utilized UV laser systems to drill 75–100 mm diameter microvias; however, flex circuits need fewer laser vias compared with other applications. The development of smaller microvias continues towards <50 mm in diameter, with smaller vias earmarked for next-generation applications within the next two to five years. Smaller via sizes overall may push laser system capital investments from CO<sub>2</sub> laser products to exclusively UV lasers, which normally drill the smaller vias. The problem UV currently faces is the comparison to CO<sub>2</sub> laser systems, which offer advantages in terms of throughput and total cost of ownership.

UV laser drilling technology has been utilizing trepanning motion, driven by galvanometer scanners or other scanning devices with a tightly focused laser spot size, 25 mm or smaller. Due

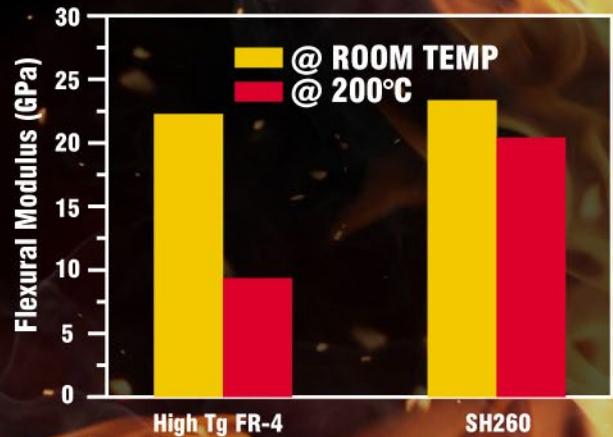


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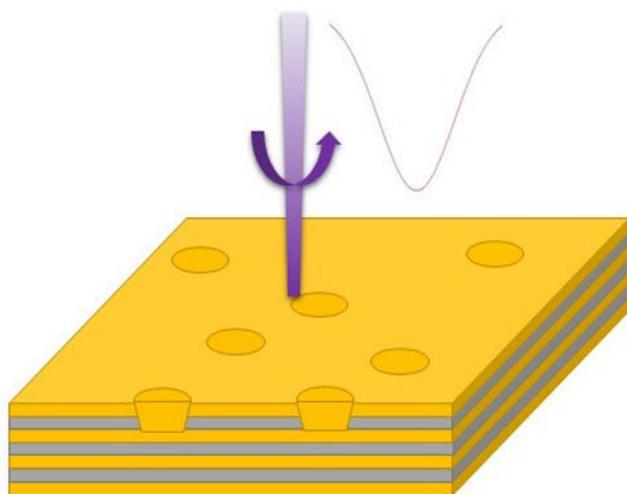
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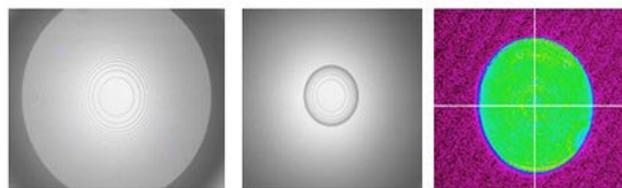
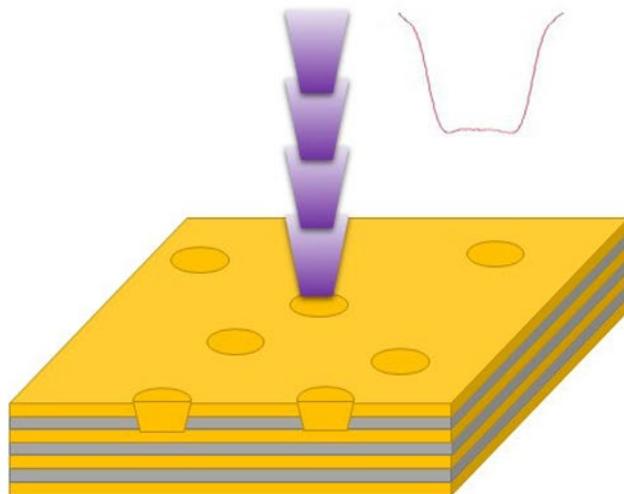
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Figure 1: UV laser drilling scheme with beam-shaping technologies.

to the limitation of a UV laser's pulse energy and frequency, percussion drilling has not been widely applied at the production levels. In order to make a breakthrough considering the above limitations, an optimal beam delivery system has been developed utilizing a unique and stable beam-shaping technology which opens up the ability of UV lasers to reach downwards to <50 micron via diameter.

This innovative design is able to deliver a flat-top energy distribution across the laser beam face from the laser to the drilling point with minimum power loss, which allows UV lasers to perform percussion drill on HDI boards with high throughput. Figure 2 shows a 50 mm diameter microvia on half-ounce copper created by UV laser percussion drilling. Those vias can be completed by UV lasers to form straight taper shapes in dielectric materials, or alternatively become conformal windows for CO<sub>2</sub> lasers to create taper shaped microvias.

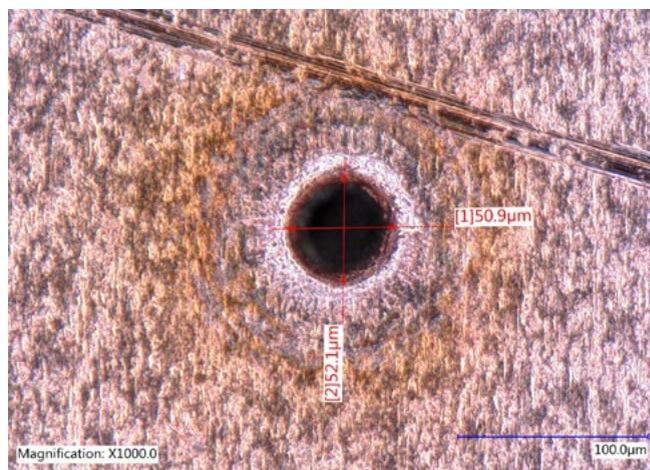


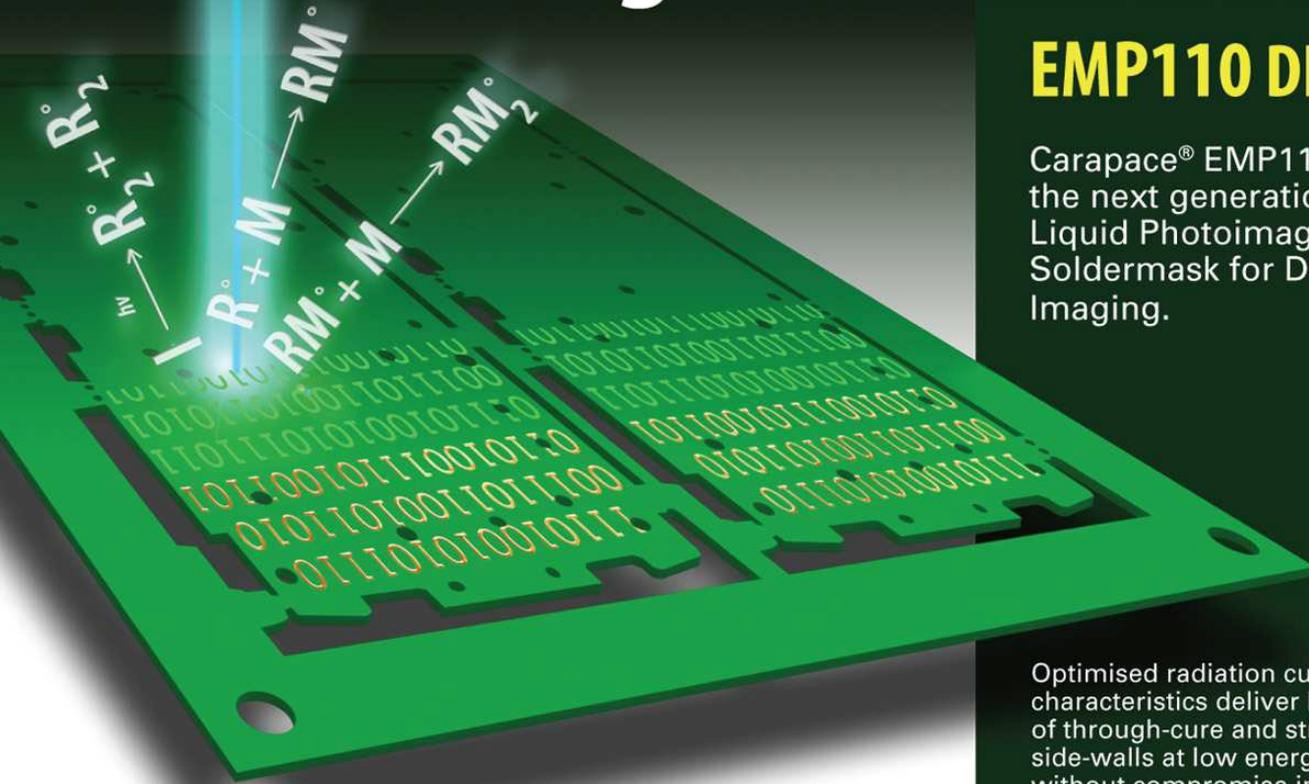
Figure 2: 50 mm diameter microvia on HDI boards drilled by UV laser percussion.

In addition, the beam delivery technology retrofits to installed laser systems so that the technology can be leveraged to meet further



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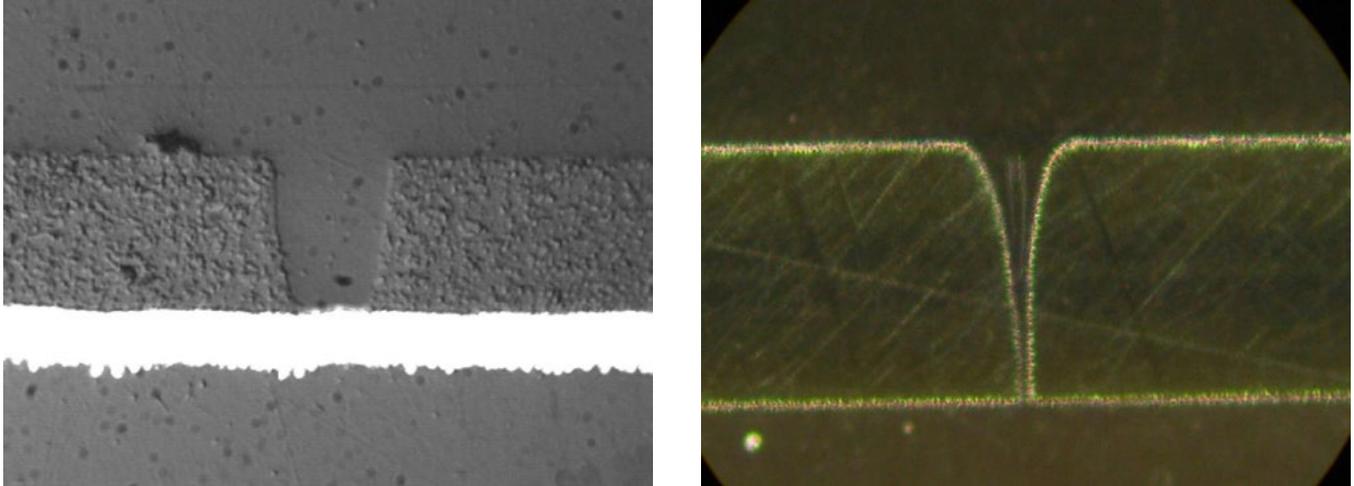
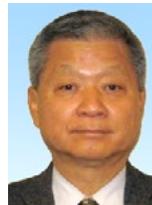


Figure 3: a) 25 mm diameter microvia on glass-filled resin; b) 25 mm/2 mm, top/bottom through-hole via on polyamide material.

demands for fine patterned packaging applications which require smaller than 25 mm vias, even on multi-beam UV/CO<sub>2</sub> platforms.

Because of the changing needs for lasers within a PCB facility, equipment that can evolve as process technology advances is always a good choice. An industrial platform that can be tailored to the specific needs of one's processes and outfitted for maximum production would be the most versatile. This would include a system that can be equipped with a variety of

laser sources, including UV, CO<sub>2</sub>, IR and green at various pulse widths. **PCB**



**Osamu Sekine** is president of Nano System Inc.

## Coming Soon: 25 Essential Skills for Engineers, by Happy Holden

A textbook-in-progress, authored by industry veteran Happy Holden and written specifically for engineers and those who want a better understanding of engineering best practices, is available on the pages of the [I-Connect007 Daily Newsletter](#) on the third Wednesday of each month. ([Click here](#) to become a subscriber.)



What started with an introductory article, [25 Essential Skills for Engineers](#), published in the January issue of *The PCB Magazine*, is now being developed into a long-term series that will appear monthly over the next 18 months. In this series, Happy will cover everything from problem solving,

DOE, and technical writing, to roadmapping, economics, and business plans—especially targeted to engineers.

From “The Need for Total Quality Control (Six Sigma and Statistical Tools), Part 1”:

“Continuous improvement must deal not only with improving results, but more importantly with improving capabilities to produce better results in the future. The five major areas of focus for capability improvement are demand generation, supply generation, technology, operations and people capability.”

Columns may also be accessed through Happy's columnist page by clicking [here](#).

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# Solder Mask for LED Applications: Formulation 101

by **Josh Goldberg**

TAIYO AMERICA

## The Rise of LED

In 2007, the United States passed legislation to phase out the manufacture and trade of incandescent light bulbs, the EU following passed similar legislation in 2009. The rest of the world has been following suit creating a huge opening in the lighting market for a technology to fill the gap. Fluorescent lights have become more compact with less mercury, but they still contain the heavy metal that could become a problem in landfills in large amounts.

Until recently, LED lights were expensive and poorly designed for general lighting usage. The manufacturing price and, consequently, the retail price have come down significantly in recent years, while the energy efficiency and brightness of LED bulbs have gone up. These improvements in the technology have led to some projections of 45% growth every year for the next five years. With the growth in the industry, there has become a higher demand for LED materials and higher expectations for LED material performance.

Solder masks are traditionally green in color, and are expected to withstand the high temperatures present in solder pots, with a need for a different color like blue, red, or black arising every once in a while. The rise in LED production has called for improvements in the color white and the color stability of the mask in general. For the lighting industry, not only are the solder masks expected to perform well, but the formulator needs to have an understanding of properties such as reflectance in relation to color theory and how this will change as various formula adjustments are made for different applications.

## What is Reflectance, and Why is it so Important?

The property of reflectance is consistently named as one of the most important properties when considering a white solder mask for LED applications, but what exactly is reflectance? First, we must differentiate between reflectance and gloss.

The strict definition of gloss is that it is an optical property which indicates how well a surface reflects light in a specular (mirror-like)

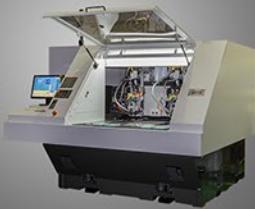
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direction. Since this is a surface property, it is affected by things like the surface topography, the refractive index of the material being measured, and the angle of incidence. The angle of incidence is important for different types of gloss. For instance, it is referred to as “sheen” when the gloss is measured at low angles to the substrate. The “luster” is the perceived brightness of the specular light and the diffuse light relative to the surface. “Specular gloss” is the light reflected at the surface opposite the incoming angle of light.

The strict definition of reflectance is that it’s a measurement of how well a surface reflects radiant energy. The surface is exposed to a light source, and the reflectance is how much and at what wavelength that light is reflected back. You typically see reflectance noted as a graph over the color spectrum with the reflectance number typically noted as the % reflectance at 450 nm. The graph in Figure 2 for a generic white product would be noted as having between 90–95% reflectance for the red and green lines with the spectrum reflectance decreasing towards red colors at around 650 nm.

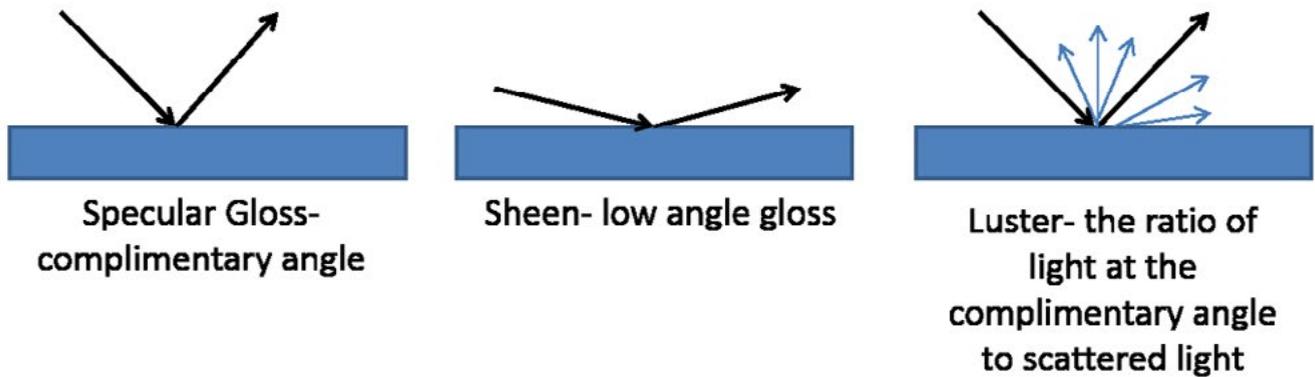


Figure 1: Examples of gloss measurements.

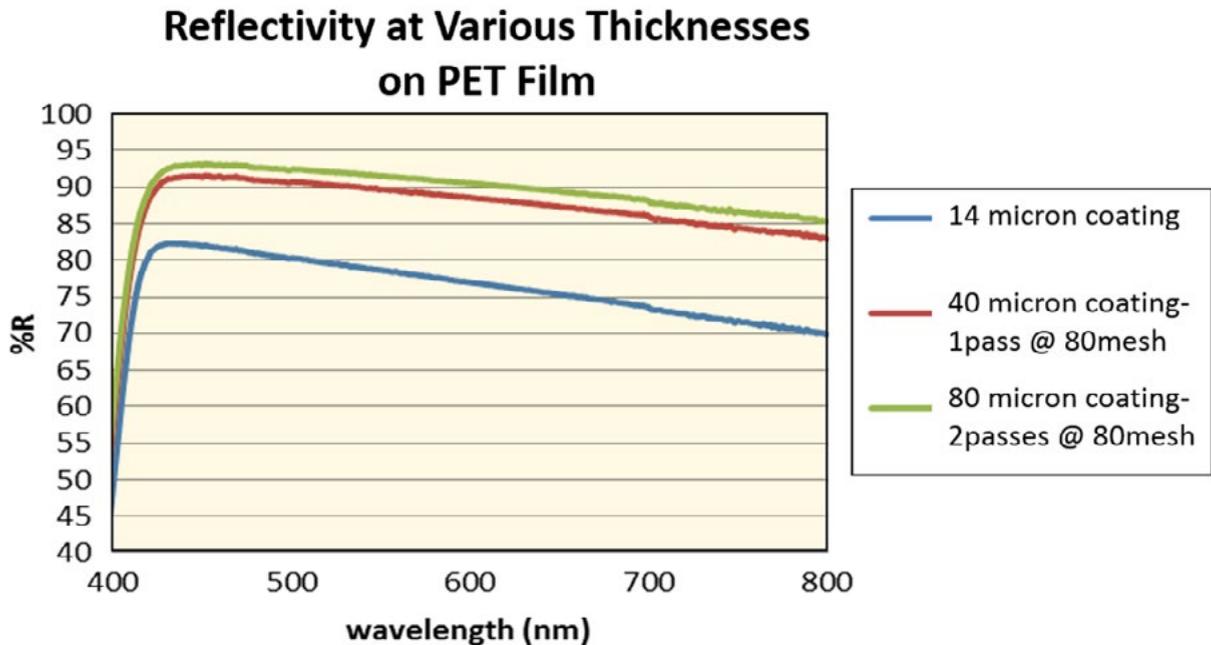


Figure 2: Reflectivity of white solder mask at various thicknesses.

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	High Reflectance	Low Reflectance
High Gloss	White glass, glossy white paint, etc.	Black glass, obsidian, etc.
Low Gloss	Movie theater screen, printer paper, etc.	Asphalt, matte black paint, etc.

Figure 3: Examples of gloss and reflectance on various materials.

Since reflectance and gloss are different properties, it is possible for something to be high reflectance and low gloss or visa-versa. Figure 3 gives some examples of how the two properties would work together.

### White Materials

Typically, the reflectance is achieved in solder mask, and just about every other material that is white, with titanium dioxide ( $\text{TiO}_2$ ).  $\text{TiO}_2$  gives a very even reflectance across the entire visible light spectrum, and it is generally inexpensive due to its abundance in the earth. There are three types of titanium dioxide that are mined and used in industry: ilmenite, rutile, and anatase. The ilmenite accounts for about 47% of the  $\text{TiO}_2$  produced in the world. The iron is removed from the ore and it is refined to the white powder used in coatings by the sulfate process or chloride process, with the chloride process being the more popular. The rutile form of  $\text{TiO}_2$  is the second most abundant natural form of the material, and anatase is rarer. Anatase is also semi-stable in that it will revert to the rutile form of  $\text{TiO}_2$  when heated around 600–800°C. Anatase  $\text{TiO}_2$  is reflective across a wider spectrum (400 nm–1000 nm), but has very poor hiding power. Rutile is reflective across a shorter spectrum (450 nm–625 nm), but has excellent hiding power. The lack of hiding power makes anatase a poor selection for LED products, but it can be used in photoimageable and UV products since it scatters light less than rutile  $\text{TiO}_2$ . Thermal curable materials will generally be whiter since the film doesn't rely on

light or UV penetration to polymerize the film, so more  $\text{TiO}_2$  in general can be used. We will discuss later about the formulation trade-offs that prevent a truly 100%-reflectance material.

### A Brief Guide to Color Theory

Sometimes, white films are made to appear whiter by using some visual tricks. One such way into tricking the eye to see a whiter film is to add a small amount of blue pigment, called “bluing.” To understand how this effect works, we must first understand how color is measured.

There are two methods that are generally used in industry to measure color now. One method is the  $L^*c^*h^*$  method where  $L^*$  is the lightness/darkness scale of the measurement,  $c^*$  is the chroma measurement that tells how pure or how grey a color is, and  $h^*$  is the hue or type of color (e.g., red, blue, green, etc.). This method is used a lot in the ink and paint industry for color matching since it closely correlates to how the human eye distinguishes color. The hue is measured in circular coordinates while the chroma is the distance from the center of the color space (the distance from gray). The color wheel in Figure 4 illustrates this concept.

The other common method for measuring color is  $L^*a^*b^*$ , or more formally known as CIE  $L^*a^*b^*$ . The CIE denotes that it was developed by the Commission Internationale de l'Eclairage, or the International Commission on Illumination. The  $L^*a^*b^*$  color space was developed to include all colors, even the ones that can't be seen by the human eye. While the  $L^*c^*h^*$  color space was circular, the  $L^*a^*b^*$  color space uses

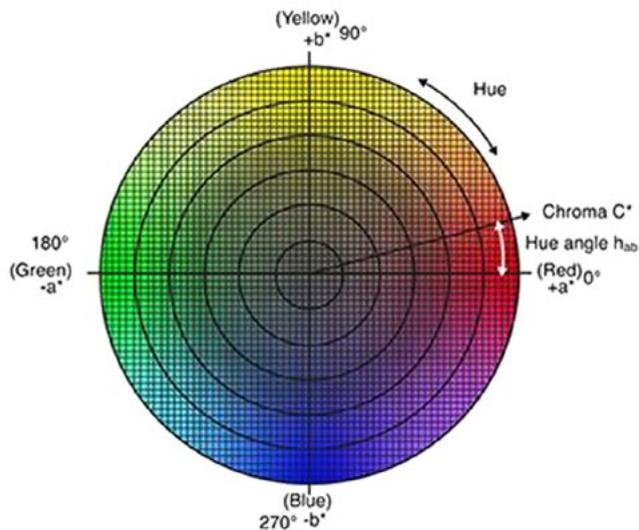


Figure 4: L\*c\*h color space  
(source: [Konica Minolta](#)).

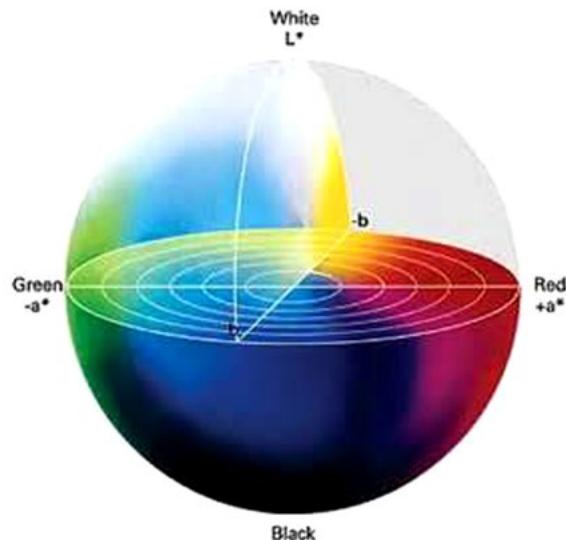


Figure 5: L\*a\*b\* color space  
(source: [ColorCodeHex.com](#)).

an xyz setup. The X-axis corresponds to red (+a) and green (-a), and the Y-axis corresponds to yellow (+b) and blue (-b). The Z-axis is the same where it represents light to dark. Figure 5 illustrates a visual representation of the L\*a\*b\* color space.

One of the less desirable properties of the epoxy materials used in solder mask is that the epoxy material tends to oxidize over time when exposed to heat, turning the epoxy yellow. Typically, you would not see this yellowing when using colored solder masks, but the yellowing is very pronounced when the mask is a white color. Unfortunately, there is no replacing the base resins in a solder mask formulation and not have it either adversely affect the physical properties of the material or the overall cost of the formulation. One of the tricks that can be used to counteract the yellowing is to add a little blue into the formulation. As you can see from the color space, yellow and blue are on opposite ends of the “b” color axis, so the blue counteracts the yellowing tendencies of the resin by pulling the color more towards the center of the “b” axis (and more towards the light/dark L\* axis). This is a great visual trick, but there can be issues when we look at a graph of the full color spectrum.

When blue pigment is added, it enhances the blue end of the spectrum as seen from the

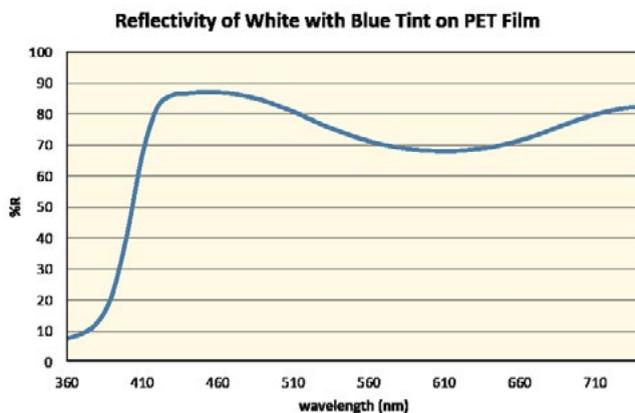


Figure 6: White solder mask with blue tint.

bump around 450 nm in Figure 6, but blue pigments also absorb colors in the green and yellow part of the spectrum (as seen from the dip in the middle of the graph). This dip reduces the overall “lightness” of the white material. In other words, the white material with the blue tint may appear whiter to the eye, but it is not as white overall, as the board that appears yellow to the eye without the blue pigment. Board manufacturers should be aware of the requirements of the OEM with regard to the type of white that they are looking for in a solder mask, as some may see this as an undesirable property.

A couple of other factors should be considered when judging a white material visually. One factor is the light source. Sometimes a color can appear different visually when it is under indoor fluorescent light, for example, compared to outdoor sunlight in a phenomenon called metamerism. When the color spectrum is measured with a spectrophotometer, the light is normalized to mimic sunlight at a color temperature of 6500°K, or 11,240°F (also known as D65 or “daylight at 6500K”). This helps to ensure that all color measurements are taken at a standard light temperature.

Another factor to consider when evaluating a white material visually is the age of the person doing the observation. As people age, the lenses in our eyes have a tendency to yellow, caused by a hardening of the lens and exposure to UV radiation. The yellowing in our eyes can cause what is known as “blue blindness,” leading to an inability to see shades of blue. So a younger observer may see a blue tint in a white solder mask while an older observer may not see blue tint at all. The overall lesson here is that visual observations are good for quick assessment of white products, but the color measurement

from a spectrophotometer is a much better indication of the true color of the solder mask.

### Formulation Tradeoffs

Generally speaking, there are three types of curing methods that are utilized for solder mask: UV cure, thermal cure, and photoimaging (which is followed by a thermal cure). There are tradeoffs with each of these curing methods with regards to how reflective a formulation can be made. The general rule regarding reflectance is that the more  $\text{TiO}_2$  in a product, the higher the reflectance. While UV curing is the fastest production method, the material cannot be loaded with a lot of  $\text{TiO}_2$  if you want to get good cure through the film. Photoimaging may be the best way to get good circuit resolution, but photoimageable materials are also limited in the amount of  $\text{TiO}_2$  that can be added. Thermal cure materials are lower resolution (limited by the resolution and alignment of the screen being used to print the solder mask), but can be loaded with a high amount of  $\text{TiO}_2$  giving the highest reflectance out of the different materials. Figure 7 gives a good representation of this tradeoff.

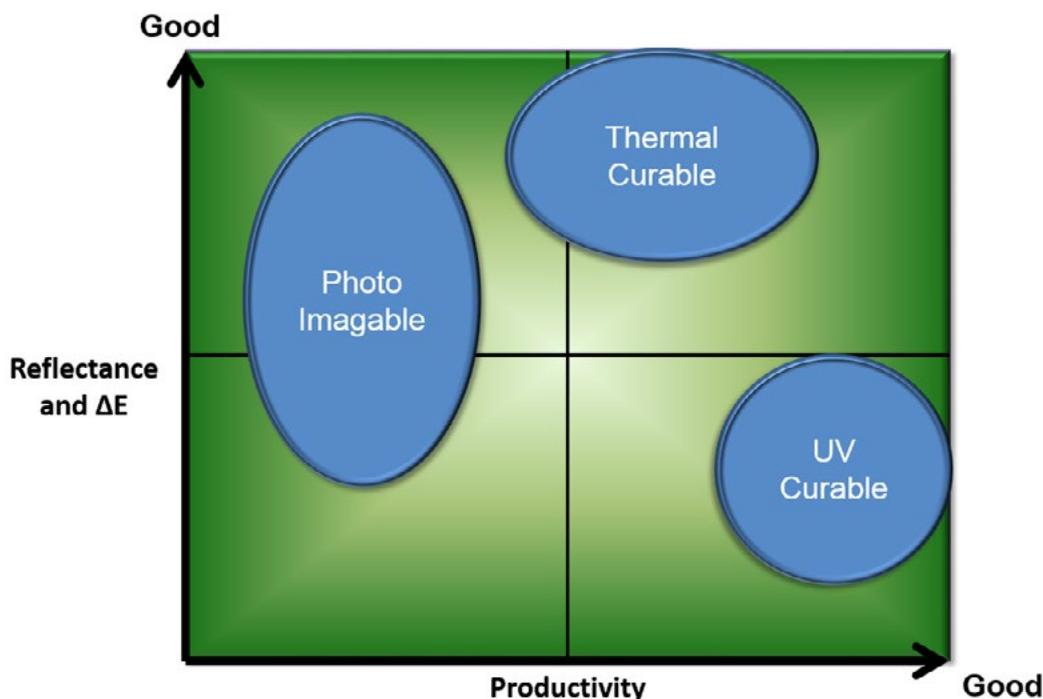


Figure 7: Comparison of productivity speed and reflectance for different types of solder mask.

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With the rise in flexible LED devices, there is also a need for flexible white solder masks. The flexibility of a solder mask is generally adjusted by using resins that have a lower cross-link density. However, there comes a point where the cross-link density gets too low to be able to have the solder mask withstand the temperatures in the soldering process (around 260°C–270°C). Additionally, the more  $\text{TiO}_2$  you load into a resin, the less flexible it becomes since there is less space in the mask

for the  $\text{TiO}_2$  particles to move past each other. Even with the current limitations of materials, the flexible LED market is making huge advances in the design and production methods that open up new possibilities for materials that will keep the flexible market competitive.

The density of titanium dioxide can also play a part in the solder mask properties.  $\text{TiO}_2$  is a dense material (around 4.2g/cm<sup>3</sup> for rutile  $\text{TiO}_2$ ), so high concentrations of it in a mask can affect the rheology and bulk behavior of the liquid solder mask, otherwise known as sag and slump. At higher concentrations, the overall mask becomes quite a bit denser. If the flow, or rheology, of the liquid solder mask is more fluid (less gel-like), then the solder mask will have a tendency to run during the tack-dry step for photoimageable masks and during the curing step for thermal masks. The density of the solder mask can also affect how thick a layer of material can be laid down at a time. The critical thickness of a layer of solder mask before the bulk material moves is the slump. Since a lot of ovens in the PCB industry are vertical-drying ovens, these can both be a problem. There are some formulation additives that can be used to beef up the rheology, but they usually sacrifice the reflectance or final gloss of the cured solder mask. Switching to a horizontal-curing oven can greatly reduce this problem, but proper oven maintenance can also greatly reduce sag-



Figure 8: The panel above demonstrates sag where the drips start at the top of the panel and slump (the thicker bottom edge of the lines). The thickness ranges from 2 mil to 12 mil from top to bottom.

ging or slumping of the liquid solder mask. If an oven has low or less than optimal air flow, then the liquid solder mask has more residual time at elevated temperatures on the board before it starts to dry. A number of solder masks have slow evaporating solvents in order to improve material flow, workability, and shelf-life. If they are put into an oven with low air-flow, then the solvents are removed from the system more slowly, increasing the dry time. The increased dry time allows the resin to dwell on the surface as a liquid longer. The higher temperature changes the surface energy and rheology of the liquid solder mask making it more prone to flow. So, proper air-flow maintenance of the curing oven, especially if it is a vertical-curing oven, is very important for white LED solder masks.

With photoimageable solder masks, straight side-walls are desirable after UV exposure and development. The property that makes  $\text{TiO}_2$  highly reflective can be a double-edged sword in the case of straight side walls. As the material is exposed to UV light, the reflectivity of the  $\text{TiO}_2$  can also bounce around light causing the curing to spread more at the top of the material with less energy reaching the bottom of the solder mask causing under-cut in the solder dam.



Figure 9: Example of undercut in a solder dam.

Unfortunately, adding more photo-initiator to the solder mask will increase the curing at the bottom of the mask, but it will also increase the sensitivity of the upper part of the mask making the under-cut worse. The best way to counteract this problem is to reduce the amount of  $\text{TiO}_2$  in the formulation, but this will lower the solder mask's reflectivity.

The UL flammability rating of a solder mask can also be a very important property to a PCB shop or OEM. Typically, the substrate of the circuit board is the largest contributing factor in determining its flammability rating. The substrate makes up the bulk of the circuit board with the layer of solder mask a relatively small contributing factor. If the substrate does not have a good flammability rating, then the solder mask will do little to improve this rating. If an additive is needed in the solder mask to try to improve the overall flammability rating, then the reflectivity of the mask is sacrificed. The additives used to achieve certain flammability ratings are not white and take up the space that would have been occupied by the  $\text{TiO}_2$  particles reducing the overall reflectivity of the solder mask. There are additives where phosphorous is added into the polymer itself improving the flammability rating, but these tend to be expensive raising the overall price of the solder mask.

## Conclusion

With the increasing production of LED products for everything from indoor to industrial applications, it has become increasingly important to enhance the technology that goes into white solder masks for LED applications. Currently, most of the property trade-offs affect the reflectivity, physical properties, or overall cost of the solder mask. However, rapidly increasing markets can also trigger rapid improvements in technology and production methods. For example, the increase in the use of inkjet printing could be coupled with the conventional screen printing used in PCB manufacturing to improve the resolution of LED PCB boards while utilizing the increased reflectivity of a thermal cure solder mask. Using print-

ed electronic additive manufacturing methods could also usher in new circuit board designs and manufacturing methods that could utilize lower temperature assembly opening up more classes of polymers outside epoxies, decreasing yellowing, increasing flexibility, improving speed of cure, or increasing reflectivity. Finally, new materials could be developed or applied in the near future that could improve the reflectivity or reduce the adverse effects of other additives that are necessary for film properties. For the LED industry, the future of materials is indeed bright.

## Acknowledgements

The author would like to thank Lisa Kennedy at our R&D facility for providing input and illustration for this article. **PCB**



**Josh Goldberg** is a marketing specialist with Taiyo America.

# Electronics Industry News

## Market Highlights



### **New Stanford Battery Shuts Down at High Temperatures and Restarts When Cool**

Stanford researchers have invented a lithium-ion battery that turns on and off depending on the temperature. The new technology could prevent battery fires that have plagued laptops, hover boards, and other electronic devices.

### **Largest Flexible X-ray Detector Made with Thin Film Transistors**

The Flexible Electronics and Display Center (FEDC) at Arizona State University and PARC, a Xerox company, announced today that they have successfully manufactured the world's largest flexible X-ray detector prototypes using advanced thin film transistors (TFTs).

### **Automotive Display Systems to Grow to \$18.6B by 2021**

Driven by continued innovation in vehicle connectivity and safety technologies, global revenue from automotive display systems will grow at a compound annual growth rate (CAGR) of more than 11% to \$18.6 billion by the end of 2021.

### **A Different Way to Make a Cathode May Mean Better Batteries**

Lithium nickel manganese cobalt oxide, or NMC, is one of the most promising chemistries for better lithium batteries, especially for electric vehicle applications, but scientists have been struggling to get higher capacity out of them.

### **Intel's 3D XPoint to Shake High-End SSD Market in 3Q16**

Aiming to enhance the efficiency of OEM system products and widen the lead over trailing competitors in the SSD market, Intel plans to ship its next-generation SSD memory products in the third quarter of 2016.

### **Breakthrough Achieved in Ceramics 3D Printing Technology**

Researchers at HRL Laboratories LLC have achieved a new milestone in 3D printing technology by demonstrating an approach to additively manufacture ceramics that overcomes the limits of tra-

ditional ceramic processing and enables high-temperature, high-strength ceramic components.

### **Engineers Demo First Processor that Uses Light for Ultrafast Communications**

Engineers have successfully married electrons and photons within a single-chip microprocessor, a landmark development that opens the door to ultrafast, low-power data crunching.

### **Satellites Find Sustainable Energy in Cities**

Underground heat islands in cities have an enormous geothermal potential. Warm groundwater can be used to produce sustainable energy for heating and cooling. Researchers of Karlsruhe Institute of Technology (KIT) have now developed a new method to find underground heat islands: They estimate groundwater temperature from surface temperatures and building densities measured by satellites.

### **New Acoustic Technique Reveals Structural Information in Nanoscale Materials**

Understanding where and how phase transitions occur is critical to developing new generations of the materials used in high-performance batteries, sensors, energy-harvesting devices, medical diagnostic equipment and other applications. But until now there was no good way to study and simultaneously map these phenomena at the relevant length scales.

### **Graphene Proves a Perfect Fit for Wearable Devices**

Cheap, flexible, wireless graphene communication devices such as mobile phones and health-care monitors can be directly printed into clothing and even skin, University of Manchester academics have demonstrated.



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# How to Set Up a Successful Blind Via Hole Fill DC Plating Process

by **George Milad**

UYEMURA INTERNATIONAL CORPORATION

Blind vias that connect layer 1 to layer 2 or layer 3 are an enabling technology for HDI-type boards. Via fill makes for a robust connection (Figure 1) with no chance of any voids during assembly. Vias with 1:1 aspect ratio are common.

Successful via-fill plating requires a specific electrolyte; the copper concentration is high at 50–60 g/L copper with low sulfuric acid at 30–60

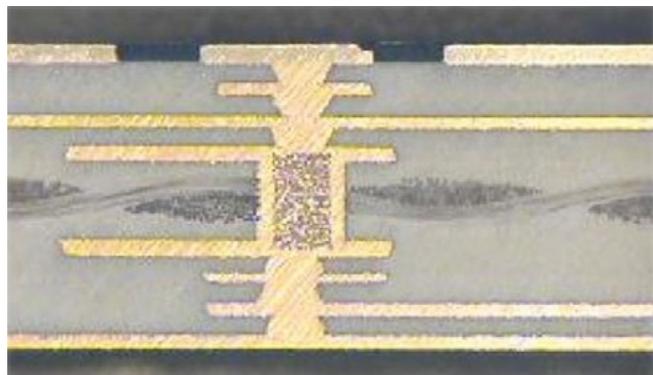
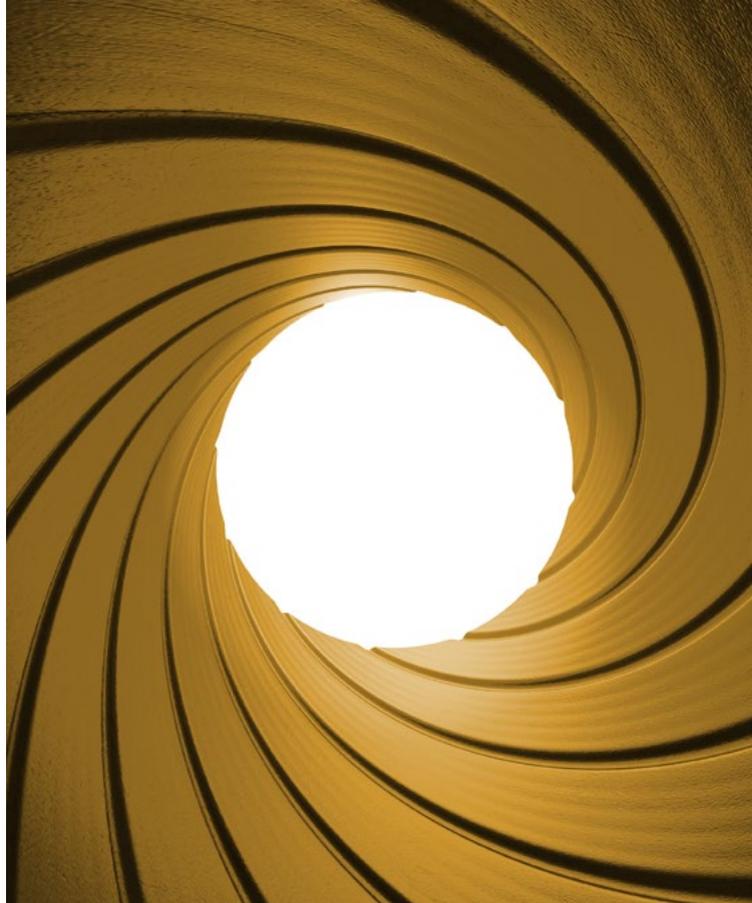


Figure 1: Stacked vias as an enabling HDI technology.

g/L. This is combined with a unique organic additive combination with a prominent leveling component. The leveling component acts predominantly on the surface and suppresses the surface plating allowing the brightener and carrier combination to plate up from the bottom of the via. Ideally the solution movement must be vigorous and parallel to the surface (laminar flow); this ensures adequate leveler replenishment.

The mechanism of via filling is different from through-hole plating. A good understanding of the following influencing factors is paramount to the success of the process.

## The Electrolyte

The electrolyte is composed of inorganic and organic components. The inorganic component for via fill is primarily a high-copper low-acid system. This ensures that there is no shortage or depletion of copper ions anywhere on the plating surface. The organic additives are composed of three components, namely the carrier or suppressor, the brightener or accelerator, and the leveler which is a selective suppressor.

Carriers increase the polarization resistance and are current suppressors. The suppression is a result of the carrier being adsorbed to the sur-

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face of the cathode; this results in increasing the effective thickness of the diffusion layer. The result is better organization. This gives rise to a deposit with a tighter grain structure. The carrier-modified diffusion layer also improves plating distribution without burning the deposit.

The brightener is a grain refiner. Its random adsorption produces a film that will suppress crystallographic differences. The brightener produces a fine-grained, non-directional (equiaxed) grain structure. It is the additive that directly affects the tensile strength and elongation properties of the deposit.

Levelers are small molecules that carry a partial charge that are attracted preferentially to the higher current density areas on the plating surface. Levelers, or leveling agents, are selective inhibitors present at low concentrations in the electrolyte, as compared to the depositing metal. Vigorous solution movement is required to replenish the leveler at the surface of the panel. Figure 2 shows an example of a mis-located air sparging pipe resulting in vigorous solution movement on the filled side with hardly any movement on the voided side.

Maintaining the organic additives within the recommended operating window is critical to the success of the process. This is accom-

plished by establishing a dosing system that is triggered by an ampere-hour accumulator. The additives are analyzed using cyclic voltametric stripping (CVS) analytical techniques.

### Filling Mechanism

There are multiple concurrent mechanisms that take place for the via-filling process to occur. The brightener and the carrier are evenly distributed throughout the via and their combined effect is to promote plating. The leveler component is only active at the knee of the hole (high current density area). It inhibits the plating at the via entrance which helps to keep the via open, allowing the brightener/carrier combination to preferentially plate up the bottom of the via. Refer to the progress of plating in Figure 3. Replenishment of the leveling component at the copper surface is a function of solution movement. Vigorous laminar flow across the surface must be designed in the original setup. In the absence of the leveler effect, the knee of the via would plate at an accelerated rate, closing the via before the filling is complete (Figure 4).

This same mechanism can fill a small diameter, low aspect ratio through-hole like a 6.0-mil diameter hole in a 10-mil thick laminate.

### The Plating Cell Setup

The plating cell design is not that different from standard acid copper plating. Attention must be made to ensure adequate anode cathode spacing (7–12 inches) in the initial design. The plating cell must be equipped with temperature control capabilities, mostly cooling. An overflow weir is recommended to maintain solution level and to facilitate filtration of suspended particles. Filtration thru 5–10 micron filter cartridges should be continuous and designed at a flow rate to ensure a minimum of two solution turnovers per hour (>2 STO). The filtration system draws from the bottom of the weir and returns below the cathode.

The number of anodes (usually titanium baskets filled with copper balls) should be optimized for the platable area of the cathode; maximum for panel plate and minimum for dot pattern (pads only). Anode placement should be such that the active length of the anode is 3–4



Figure 2: Misplaced air sparger; solution movement only on one side (filled vias).

inches shorter than the cathode, and should be tucked in 3–4 inches inside the cathode window on the outside vertical edges.

The panels ideally should have a common vertical dimension and should be racked with

minimum gaps. If the cathode bar is not fully racked, dummy panels or thieving strips must be used to prevent imbalance in thickness distribution; alternatively the anode baskets opposing the gap may be isolated.

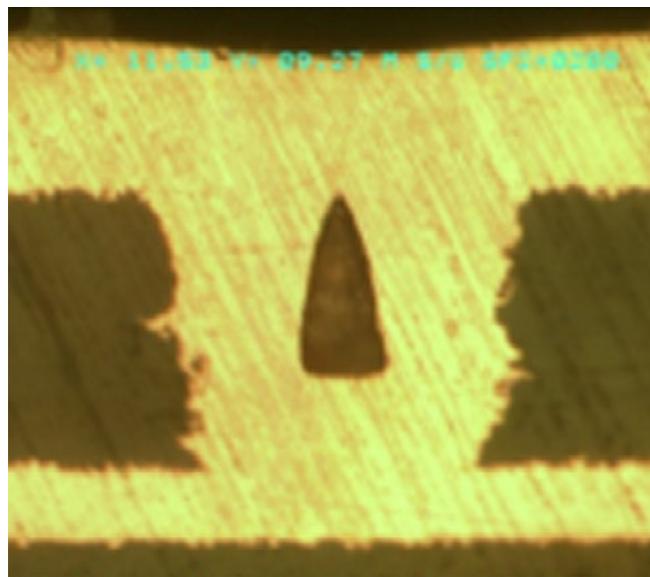
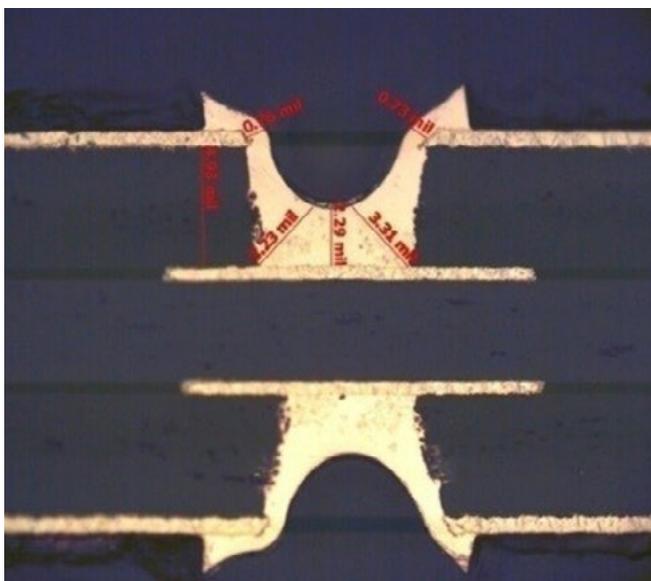
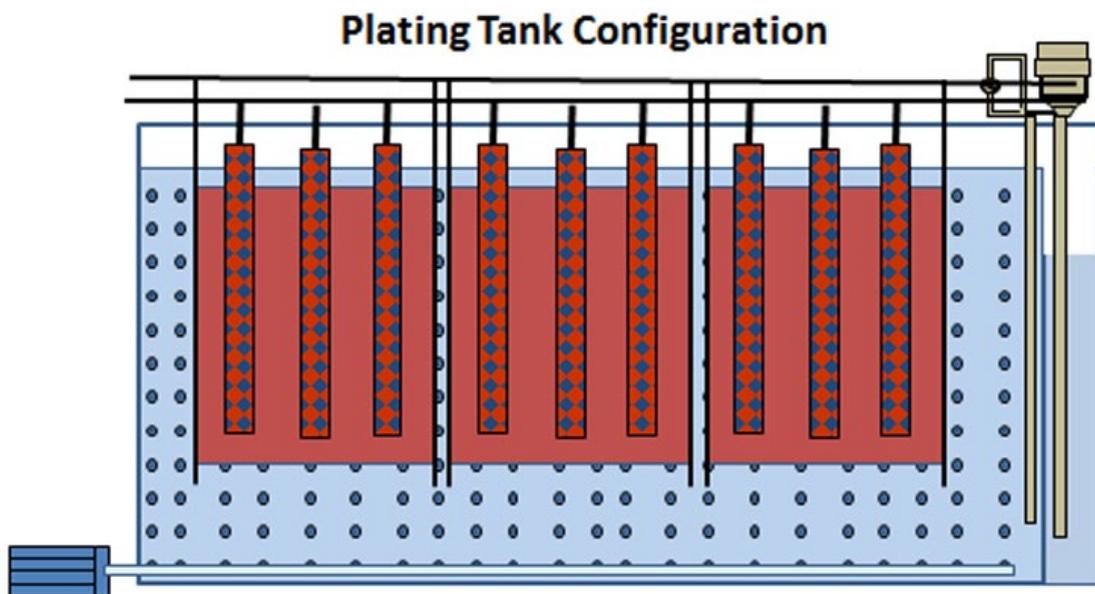


Figure 3: Preferential bottom plating in progress.

Figure 4: Conformal plating.



**3 anode baskets per 18 X 24" panel'. Air Blower with bottom air sparging pipe. Filter pump withdrawing from "Overflow Weir" discharging into plating tank.**

Figure 5: Schematic of plating tank configuration.

Solution agitation is initiated at the bottom of the tank; it may be air sparging or eductor agitation. There should be two manifolds, one in front of the panel and one in the back. The spacing between the top of the sparging system and the bottom of the panel should be at least six inches. It is intended to produce a uniform laminar flow across the surface of the panel. The flow should be vigorous to ensure sufficient leveler replenishment at the entrance of the via. Via filling will not occur if solution agitation is inadequate as demonstrated in Figure 2. Part agitation is not necessary in this setup.

**Rectification**

The rectifier should be sized to supply the desired output. For example if the platable area is limited, a smaller rectifier would be the right choice, it is not advised to use a 200 ampere rectifier to plate at 10–20 amperes per load. Ripple (% AC or alternating current) should be less than 5% to ensure the deposit is fine-grained,

adherent and equiaxed. High ripple would have an adverse effect on the physical properties of the deposit. The rectifier control accuracy or resolution should be 1–2% to ensure consistency of output.

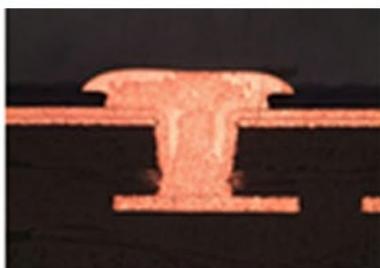
The ASF to be used in plating the blind via should be optimized for the via dimensions. More demanding vias (higher aspect ratio) will require lower ASF for a longer time. Traditionally there are two approaches to the plating current density (CD). The first approach is a single CD for the duration of plating. The second approach is to step up the CD with time, for example, 10 ASF for 45 minutes followed by 20 ASF for 30 minutes and then 25 ASF for 15 minutes. Both methods work and the choice should be made at the initial installation through experimentation and testing. Once established, this becomes the method. The method may be optimized again as the next level of difficulty (higher aspect ratio) is encountered.

**Comparing Surface Copper Thickness as a Function of Proximity to the Thieving Edge**

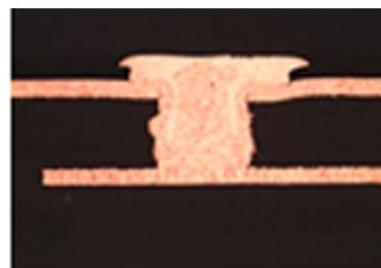
CENTER (2.2)



OFF THE EDGE ( 1.6)



EDGE (1.0)



It is clear from the thickness on the surface that the current density is very different in the three locations. The “Center” carries the most current the “Off Edge” and the “Edge” are much closer to the theiving edge and are robbed of current. The ratio of the surface copper plating thickness is 1.0 for the Edge to 1.6 for Off Edge and 2.2 for the Center.

Figure 6: Variation in current density distribution in “dot” pattern plating.

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**Panel vs. Pattern Plating**

Both methods of plating are being utilized in the industry. Panel plate creates greater uniformity across the board; however, it is more demanding on the planarizer to reduce the plated surface copper. Flash plating the electroless copper is not recommended as it tends to increase the aspect ratio of the hole.

In most cases pattern plate is a pads-only pattern, referred to as a “dot” pattern. The panel after electroless metallization is imaged using photoimagable dry film resist. A half inch of non-imaged laminate copper is left exposed on all four sides. This edge is used for rack connectivity during electroplating. This copper edge has a thieving effect on the distribution of the copper thickness above the via. Vias or pads in

the center of the panel will plate much thicker than their counterparts closer to the edge. Figure 6 shows that the current density at the different locations varies more than 2X between the vias along the edge versus the vias in the center of the panel; note that all the vias are filled in spite of the large variation in current density from via to via. All the variability in copper thickness above the via is removed during planarization.

Periodic carbon treatment, to remove organic contaminants leaching from the dry film, must be set up on a regular basis to ensure consistent performance from the electrolyte.

**Pre-treatment**

The pre-treatment is composed of the following steps: cleaner, micro-etch and acid pre-dip.

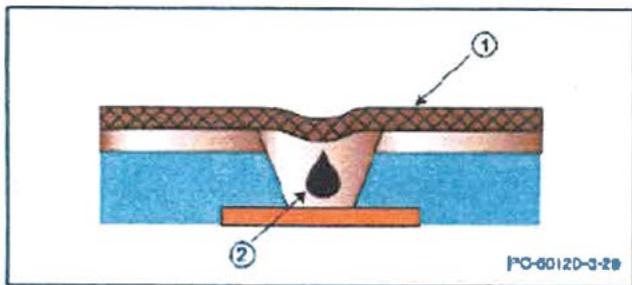


Figure 3-29 Example of Acceptable Voiding in a Cap Plated Copper Filled Microvia

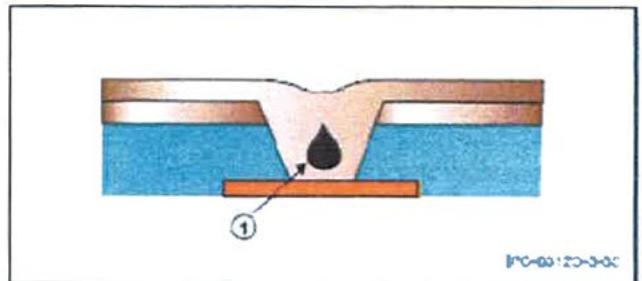


Figure 3-30 Example of Acceptable Voiding in a Copper Filled Microvia Without Cap Plated

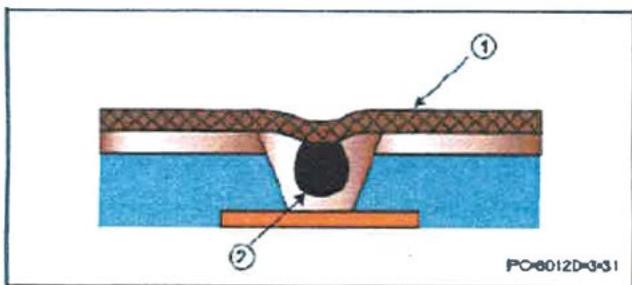


Figure 3-31 Example of Nonconforming Void in a Cap Plated Copper Filled Microvia

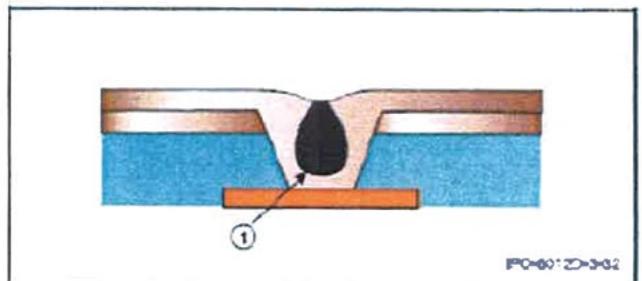


Figure 3-32 Example of Nonconforming Void in a copper filled Microvia

**3.6.2.11.3 Plated Copper Filled Microvias** Microvias shall be completely filled with copper except that voids will be acceptable provided they are completely encapsulated and in total do not exceed 25% of the viewable area of the filled microvias shown in figure 3-29 and figure 3-30. Voids not fully encapsulated within these limits are not acceptable as shown in figures 3-31 and figure 3-32.

Figure 7: IPC-6012D, filled via plating requirements.

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### The Cleaner Step

The cleaner is composed of a solvent, an acid and a surfactant. The solvent removes organic surface residues by dissolution. The acid removes oxidation and the surfactant wets the surface. The wetting is very important when plating small high-aspect ratio holes or blind vias; a well wetted surface will not entrap air. Intermittent vibration in this step is helpful to ensure that all air is dislodged from tight spaces. Follow vendor's recommendations of concentration, temperature, dwell time, and dump and remake schedule to ensure the cleaner functions as intended. Good two-step rinsing is important after the cleaner as its components in trace amounts, if dragged down the line may adversely affect the plating.

### The Micro-etch Step

The micro-etch is made up with a strong oxidant like sodium persulfate or hydrogen peroxide in a sulfuric acid medium. The micro-etch oxidizes the surface copper and literally etches it away, exposing a fresh copper surface for plating. If the metallization used is electroless copper; the concentration and dwell time should be controlled to ensure that the electroless copper is not etched away. In addition, the micro-etch can undercut minute stubborn residues that the cleaner did not remove. Concentration, temperature, dwell time, and dump/remake schedule must be adhered to. The panels are double-rinsed after the micro-etch.

### The Pre-dip Step

The pre-dip is made up with sulfuric acid at 5–10%. This step ensures that the surface is oxidation-free and is acidic to match the acidity of the electrolyte. There is no rinse between the pre-dip and the acid copper bath.

### Voids

Ideally there should be no voiding in the copper-filled via. The latest version of IPC-6012D spells out acceptability criteria as detailed in Figure 7.

The primary cause of voids is poor wetting of the via by “entrapped air.” All air must be removed from the via in the initial cleaner step. Cleaners with low surface tension are better

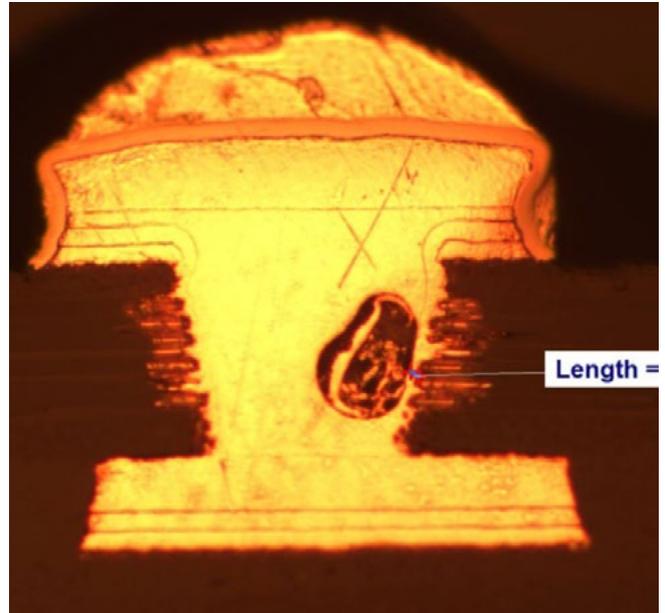


Figure 8: Void due to air entrapment in the via.

suited for this task. Intermittent vibration in the cleaner ensures that all air is dislodged and that the surface of the via is fully wetted. Figure 8 demonstrates air entrapped voiding.

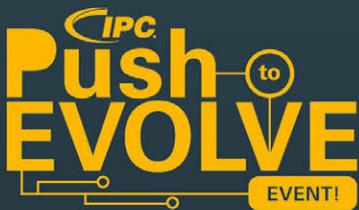
Another form of voiding occurs when the plating at the knee of the via proceeds at a faster rate than at the bottom (Figures 2 and 4). Here the hole is closed at the entrance before the bottom plating has filled in. This is the result of imbalance in the leveling component, poor solution agitation or both.

With a good understanding of the plating principles of the process, proper choice and control of the chemical process, periodic carbon treatment, and paying attention to the details of cell design, the “via fill” process can run trouble-free. **PCB**



**George Milad** is national accounts manager for technology with Uyemura International Corporation.

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# Root Cause Analysis: CSI for the PCB Industry

by **Steve Williams**

THE RIGHT APPROACH CONSULTING

One of the most frustrating parts of a customer's life is dealing with a performance issue that hasn't been properly addressed at a supplier and continues to resurface. What it usually boils down to is not lack of effort, but lack of root cause analysis (RCA) training.

## Recognize the Symptoms

Most companies have some form of a corrective action system in place to handle customer complaints, returned goods, defects, internal scrap, etc. And while any system can always be improved upon, the source of the frustration is not the system, but the methodology.

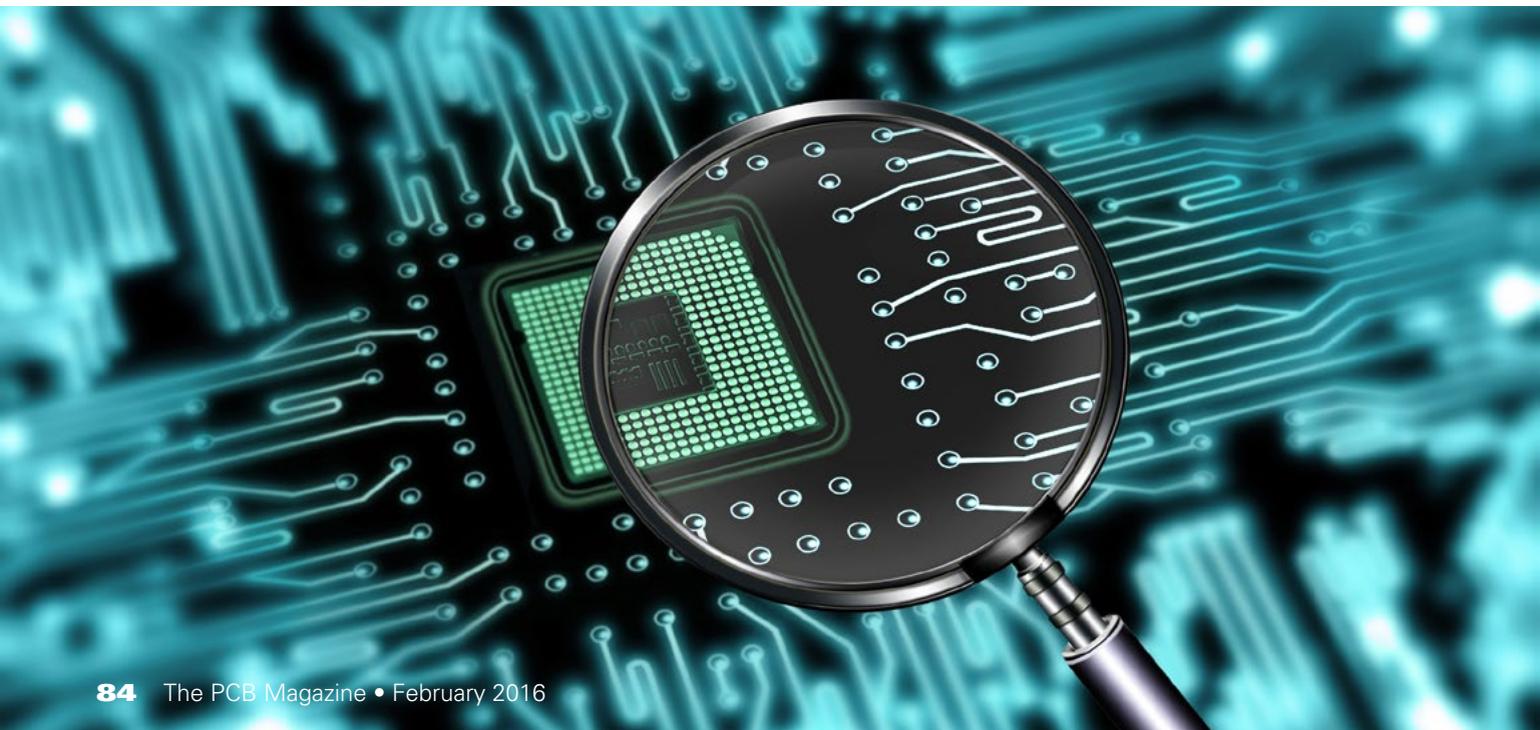
It is somewhat embarrassing to observe the overall quality of the corrective action analysis that is published by the PCB industry as a whole. Of course, many companies excel at root cause analysis, but far more pale in comparison. Treating the symptoms is a condition that afflicts many PCB companies, and a general edu-

cation in true root cause analysis methodology is sorely needed.

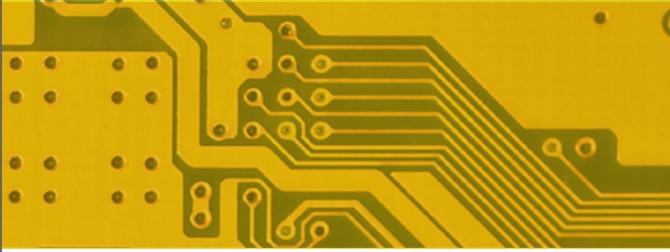
One of the most abused people in the industry is the poor line operator. How often has your company stated to a customer that the root cause for such-and-such a defect was operator error? More than you would be willing to admit, I would venture. It is my belief that if a company did a true root cause analysis, it would discover that only about 5% of these causes actually would be attributable to true operator error, and that 95% would be directly attributable to a management or system issue. Without the proper training, tools and system, the poor operator doesn't stand a chance.

## Root Cause Analysis

The goal of RCA is to find out what happened, why it happened, and how to prevent it from happening again. Chasing symptoms instead of digging deep to find root cause will



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almost certainly guarantee that the problem will repeat. Although RCA is initially a reactive mechanism, it can become a tool for developing prevention strategies if used properly. Whatever methodology of RCA is used, the system must:

- Be interdisciplinary and team-based
- Include those most familiar with the situation
- Dig deep at each level of cause and effect (The 5 Whys)
- Be a process that identifies needed system changes
- Be unbiased

**Drill Deep**

A good place to start is to make sure that defect classification codes are truly describing the defect, not the symptom. It still amazes me when I go into a shop and review internal scrap data and see generic defect codes such as “electrical test short/open” or “undersized hole” for example. I’m pretty sure that the electrical test department did not create the short. Is it an internal or external short? Did incorrect CAM data, a damaged phototool, resist breakdown, a handling scratch, or something else cause the short?

To continue, was the undersized hole a result of an engineering error, wrong drill bit, drilling

## 5 Whys

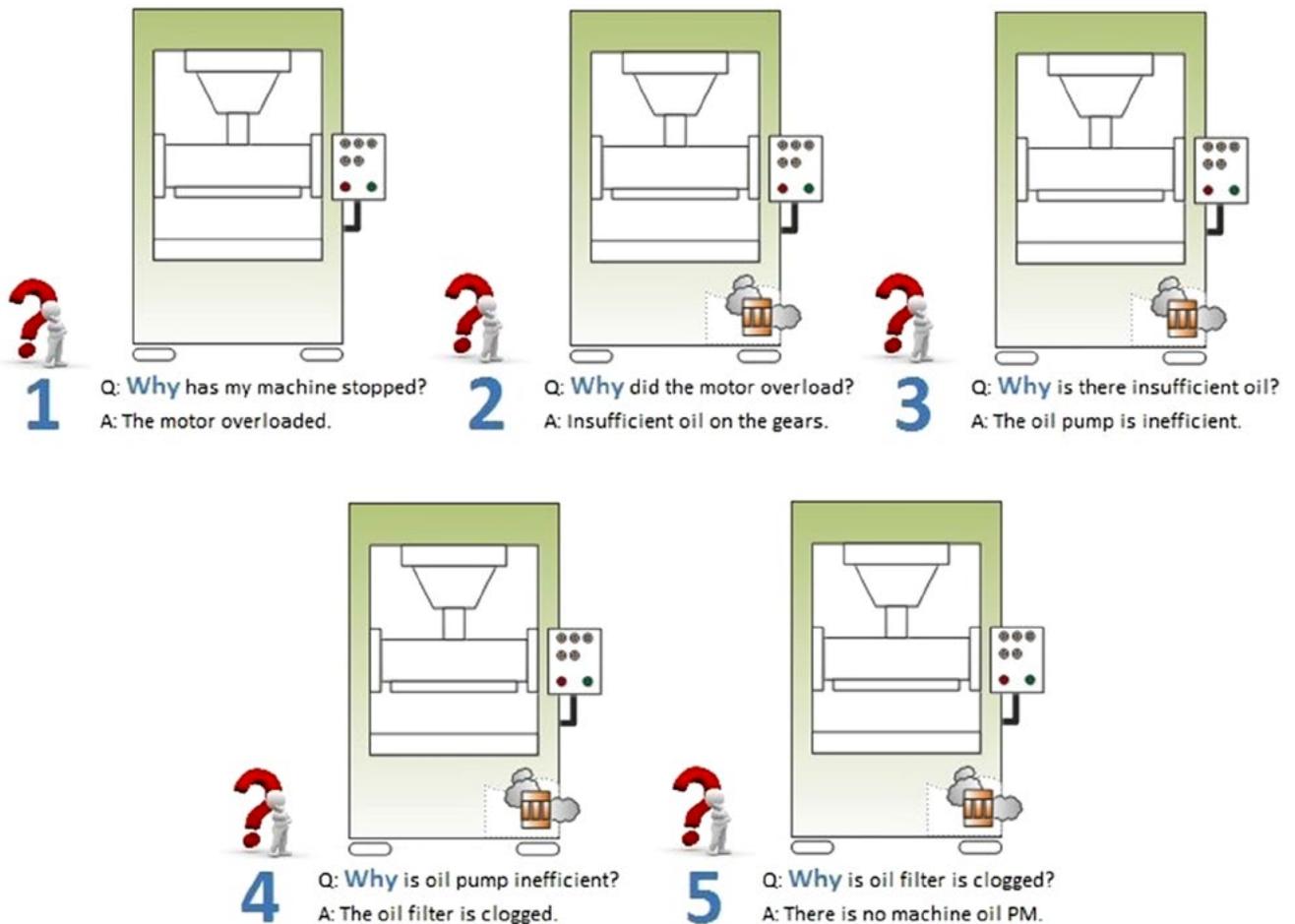


Figure 1: Practical example of the 5 Whys.

debris, or over plating? If it was over plating, was it caused by an incorrect plating program, incorrect plating square inch data, inaccurate copper thickness measurement or a tool? See where this is going...there are multiple permutations of each potential root cause that needs to be broken down and evaluated. When the quality group runs the monthly quality report, the defect Pareto will not be very effective if generic, broad-based defect codes are used. Peeling back the onion, layer-by-layer, can be a long and tedious process, but it will be very difficult to attack the heavy-hitters by analyzing the symptoms and not the source.

**Tools**

There are many RCA tools available, including Ishikawa Cause & Effect Diagrams, Fault Trees, Brainstorming, Scatter Diagrams, DOE

(design of experiment), and the 5 Whys technique.

The 5 Whys have become a very popular and highly effective RCA tool. The technique gained prominence when it became an integral part of the Toyota Production System in the 1970s. By continually asking “Why?” (5 times seems to be effective, but it could be four or it could be seven) you can quickly peel away the symptoms and drive to the true root cause (Figure 1). While embroiled in the “why” game with your five-year-old, you probably never imagined that they were using an advanced root cause analysis technique on you! Ah, the wisdom of children.

**Three Types of Causes**

The basic premise of RCA is that it assumes that systems and events are interrelated. You have heard the maxim, “For every action there

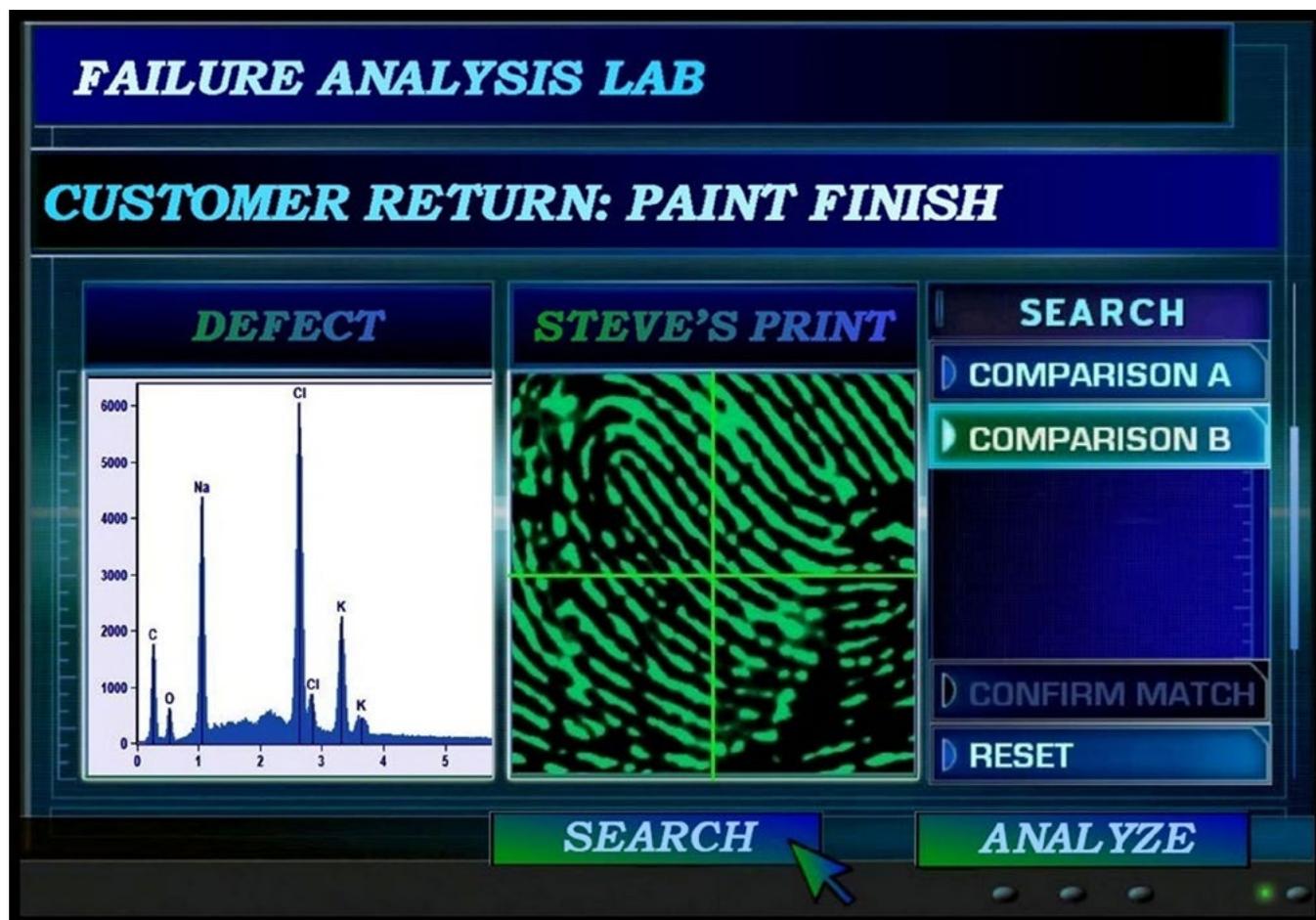


Figure 2: CSI-style root cause analysis.

is a reaction.” As applied to RCA it means that an action in one area triggers an action in another, and another, and so on. By tracing back these actions, you can discover where the problem started and how it manifested into the symptom you’re now facing.

You’ll usually find three basic types of causes:

1. Physical causes: Tangible, material items failed in some way (e.g., a plating rectifier stopped working).
2. Human causes: People did something wrong, or did not do something that was needed. Human causes typically lead to physical causes (e.g., no one performed PM on the rectifier, which led to it failing).
3. System causes: A system, process, or policy that people use to make decisions or do their work is faulty (e.g., the rectifier was not included in the PM system). (Remember my earlier statement that 95% of causes would be directly attributable to a management or system issue?)

RCA considers all three types of causes and involves investigating the patterns and trends of negative effects, finding hidden flaws in the system, and discovering specific actions that

contributed to the problem. This often means that RCA reveals more than one root cause, each of which needs to be thoroughly vetted through the process.

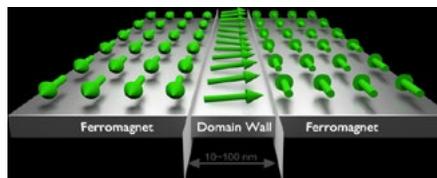
While there may be the occasional Nero Wolfe in a company (or for my younger readers, a Gil Grissom), advanced RCA skills are generally a learned behavior. The first investment should be in advanced problem-solving training for (at a minimum) all management on the tools discussed earlier in this column. I like to make the analogy to one of my favorite television programs, Crime Scene Investigation (the Grissom reference). A quality professional is like a crime scene investigator, and the defect is the crime scene. As illustrated in Figure 2, and during each episode of CSI, the point is reiterated that the evidence will lead to the origin of the crime. The same is true with root cause analysis; where you find one you will always find the other. **PCB**



**Steve Williams** is the president of The Right Approach Consulting LLC. To read past columns, or to contact Williams, [click here](#).

## A Highway for Spin Waves

The success story of information processing by way of moving electrons is slowly coming to an end. The trend towards more and more compact chips constitutes a major challenge for manufacturers, since the increasing miniaturization creates partly unsolvable physical problems. This is why magnetic spin waves could be the future: They are faster than electronic charge carriers and use less power. Researchers at the Helmholtz-Zentrum Dresden-Rossendorf (HZDR) and TU Dresden have developed a method for controlling the propagation of these information carriers at the nanolevel in a targeted and simple way; so far, this required a lot of power. They have thus created a basis for nanocircuits that use spin waves.



“Our current information processing is based on electrons,” explains Dr. Helmut Schultheiß from the HZDR’s Institute of Ion Beam Physics and Materials Research. “These charged particles flow through the wires, creating electric currents. Yet in the process they collide with atoms and lose energy, which escapes into the crystal lattice in the form of heat. This means that chips get all the warmer, the closer the elements on them are grouped together. Eventually they fail, because the heat cannot be conveyed anymore.” This is why Schultheiß, head of an Emmy Noether Junior Research Group, pursues a different approach: information transport via spin waves (magnons).

## TTM TECHNOLOGIES - CHIPPEWA FALLS DIV

Chippewa Falls, Wisconsin, U.S.A.



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The TTM Chippewa Falls facility is located in Chippewa Falls, Wisconsin and is approximately 234,000 sq ft. This facility employs approximately 1,000 production staff and specializes in NPI and volume production of high layer count PCBs.

This facility began as a captive operation for Cray Computer. It was sold to Honeywell and operated as Honeywell ACI until being purchased by TTM Technologies in December of 2002.

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# TOP TEN



## Recent Highlights from PCB007

### 1 IoT, Community and Content at the Centre of CES

Phillip Stoten writes about his observations during the recent CES 2016 Show in Las Vegas, including new trends driving the next generation of consumer electronics technologies such as IoT and content.



### 2 Happy's Essential Skills: The Need for Total Quality Control (Six Sigma and Statistical Tools), Part 1

In this first of many columns covering my "Twenty-Five Essential Skills Every Engineer Needs to Learn," I will expand on each of those skills. The introduction to this series published in the January issue of *The PCB Magazine*. As a quick recap, here are the 25 skills that I will be writing about over the next 18 months or so, to publish every three weeks or so in the PCB007 Daily Newsletter.



### 3 CES 2016 Wrap-Up, Part 1

CES 2016 is now history and most of us are home, or at our next port-of-call. I have seen various attendance numbers, but it's somewhere in the range of 175,000; it was busy, crowded and impossible to see everything. Here is my review of some of the most innovative devices and technologies at CES.



### 4 CES 2016: Press Day, Showstoppers and LaunchIt Event

Tuesday, January 5 was press day at CES 2016. Some of the largest press conferences are held on press day. Many of them are one- or two-hour advertisements with a number of new product announcements inserted, and some do provide a great deal of market data and trends. The bigger "pressers," such as the Samsung event, fill multiple auditorium-sized rooms as well as overflow rooms.



## 5 Weiner's World

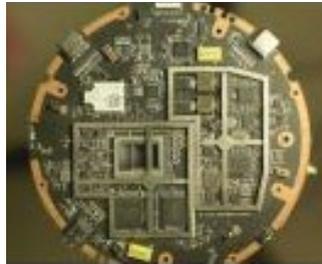
In this article, industry veteran Gene Weiner looks back at some of the industry highlights in 2015, and ponders on the challenges and opportunities to expect this year. He also highlights recent industry events, including the 2015 International Printed Circuit & APEX South China Fair and SEMICON Japan.



Gene Weiner

## 6 CES: Day One

CES Unveiled is the official media event for CES. It is the first official happening of what promises to be a very busy and fascinating week. At this event, members of the press get to preview a number of innovative startups as well as some new products from a few established global brands.



## 7 WKK's Hamed El-Abd on the Current State of China

In the world of real estate, the key term might be "location," but in manufacturing today, it's automation, automation, automation. I had the opportunity to interview WKK's Hamed El-Abd at the recent HKPCA show, who discussed the company's entry into the direct imaging market and how certain areas of the Chinese market are being flooded by a staggering amount of Chinese equipment manufacturers.



## 8 AT&S Offers Expanded PCB Sales Support in the U.S.

AT&S, one of the global leading manufacturers of high-end PCBs, with headquarters in Leoben, Austria, is committed to absolute customer orientation supporting its vision: "First choice for advanced applications."



## 9 Digital Imaging Revisited

The advantages of digital circuitization techniques have been described in detail by suppliers of equipment and photore-sist. Since phototool generation and conditioning are omitted, there is the advantage of shorter lead time.



## 10 Catching Up with HSIO's James Rathburn

I have interviewed James Rathburn a number of times in the past few years and he always has something new to say. One of the industry's leading technology inventors, Jim is always finding himself on the cutting edge of our technology. The recent acquisition of the former HEI operation in Tempe, Arizona exemplifies the path his company is taking towards a goal of being the industry's true technology leader.



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# Events

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For the SMTA Calendar of Events, [click here](#).

For the iNEMI Calendar of Events, [click here](#).

For the complete PCB007 Calendar of Events, [click here](#).

## **[MD&M West](#)**

February 9–11  
Anaheim, CA USA

## **[FlexTech Alliance](#)**

February 29–March 3, 2016  
Monterey, CA USA

## **[ICT-UK Evening Seminar](#)**

March 1, 2016  
Tewksbury, England



## **[IPC APEX EXPO 2016](#)**

March 13–17, 2016  
Las Vegas, Nevada USA

## **[25<sup>th</sup> China International PCB & Assembly Show 2016 \(CPCA\)](#)**

March 15–17, 2016  
Shanghai, China

## **[2016 Annual Foundation Course \(ICT\)](#)**

April 11–14, 2016  
Loughborough, England

## **[Thailand PCB Expo 2016](#)**

April 19–22, 2016  
Bangkok, Thailand

## **[JPCA Show 2016](#)**

June 1–3, 2016  
Tokyo, Japan

## **[IPCA EXPO 2016](#)**

August, 2016  
India

## **[IPC Fall Meetings](#)**

September 24–30, 2016  
Rosemont, IL USA

## **[SMTA International 2016](#)**

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## **[electronica](#)**

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## **[International Printed Circuit & Apex South China Fair \(HKPCA\)](#)**

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PUBLISHER: **BARRY MATTIES**  
barry@iconnect007.com

SALES: **ANGELA ALEXANDER**  
(408) 489-8389; angela@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**  
(916) 266-9160; tobey@iconnect007.com

*EDITORIAL:*  
MANAGING EDITOR: **PATRICIA GOLDMAN**  
(724) 299-8633; patty@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**  
+44 (0) 1455 293333; pete@iconnect007.com

*MAGAZINE PRODUCTION CREW:*  
PRODUCTION MANAGER: **MIKE RADOGNA**  
mike@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **MIKE RADOGNA, SHELLY STEIN, TOBEY MARSICOVETERE**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

COVER IMAGE: **DAN FEINBERG**

COVER DESIGN: **SHELLY STEIN**

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February 2016, Volume 6, Number 2 • The PCB Magazine© is published monthly, by BR Publishing, Inc.

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EDITORIAL CONTACT

**Patty Goldman**

[patty@icconnect007.com](mailto:patty@icconnect007.com)

+1 724.299.8633 GMT-4

SALES CONTACT

**Barb Hockaday**

[barb@icconnect007.com](mailto:barb@icconnect007.com)

+1 916 365-1727 GMT-7



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