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May 2015

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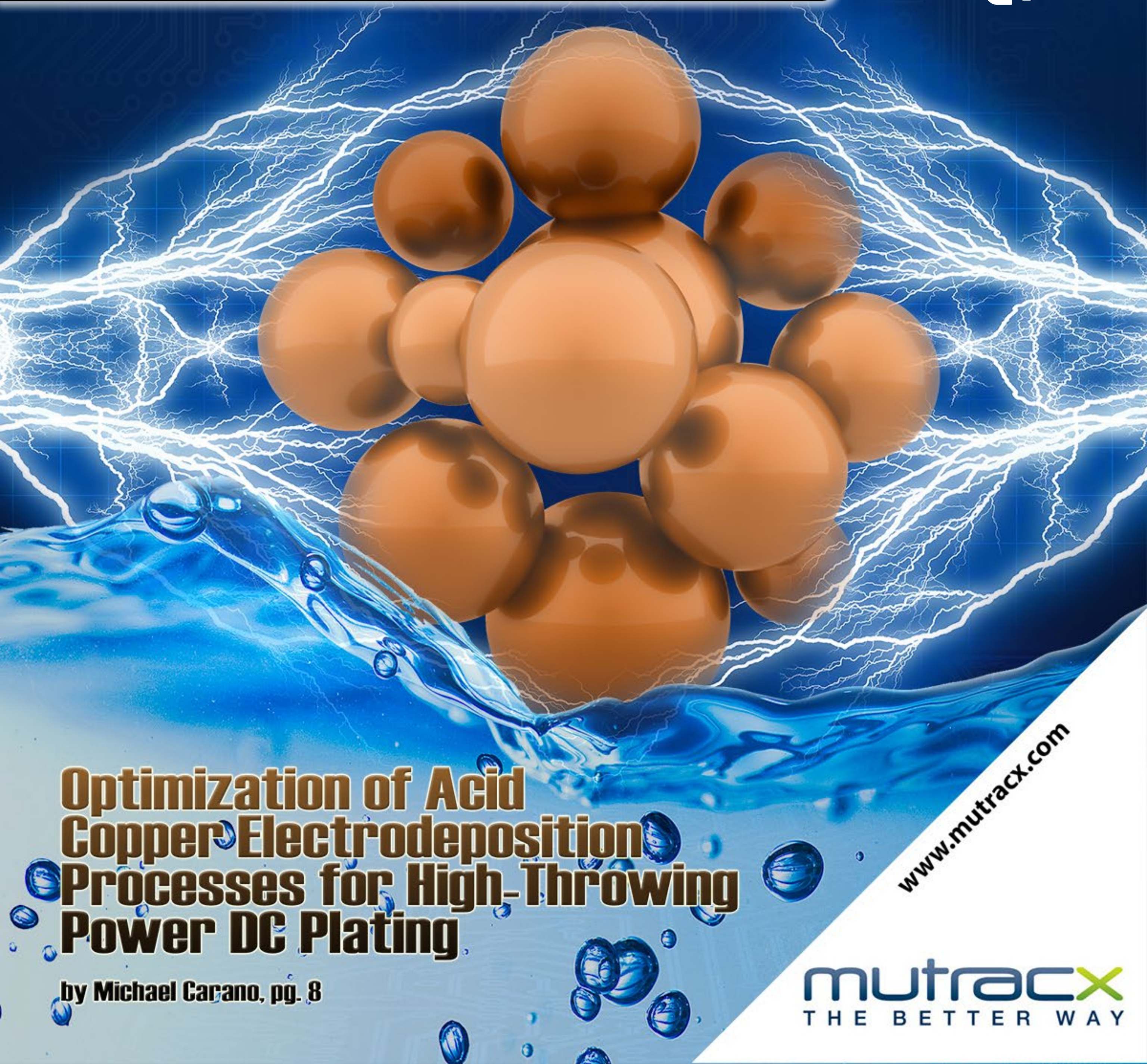
PLATING & ETCHING



Optimization of Acid Copper Electrodeposition Processes for High-Throwing Power DC Plating

by Michael Carano, pg. 8

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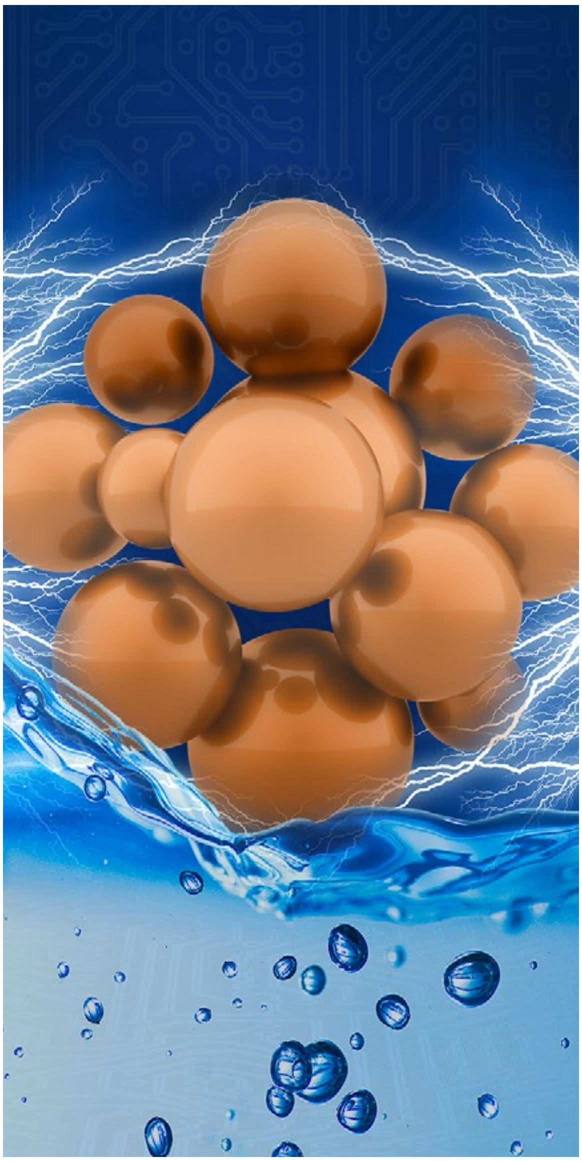
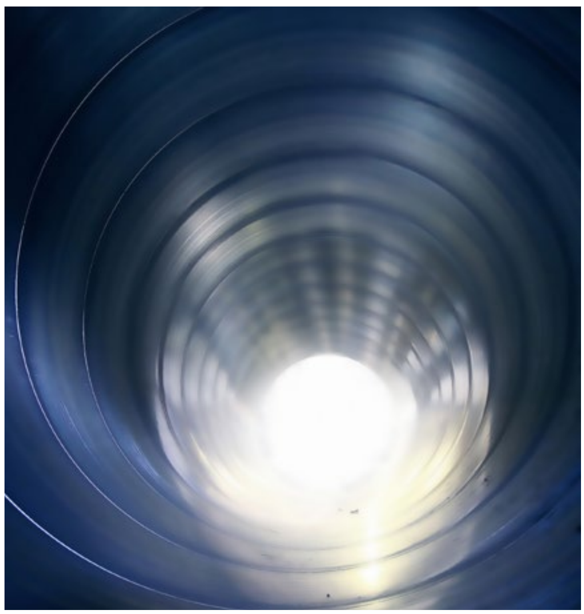
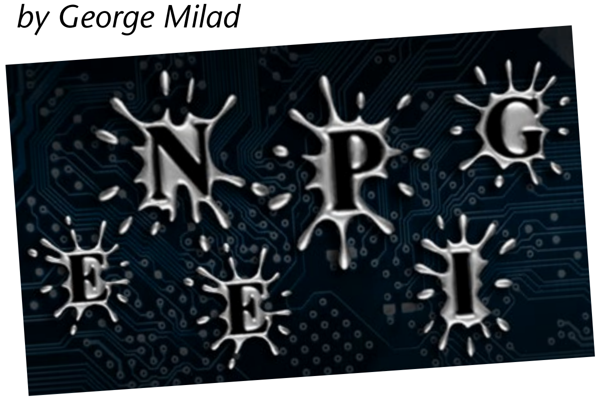
May Featured Content

PLATING & ETCHING

This month, features from Michael Carano (RBP Chemical Technology), a team from Dow Chemicals Company, and George Milad (Uyemura) share their perspectives on plating and etching issues.





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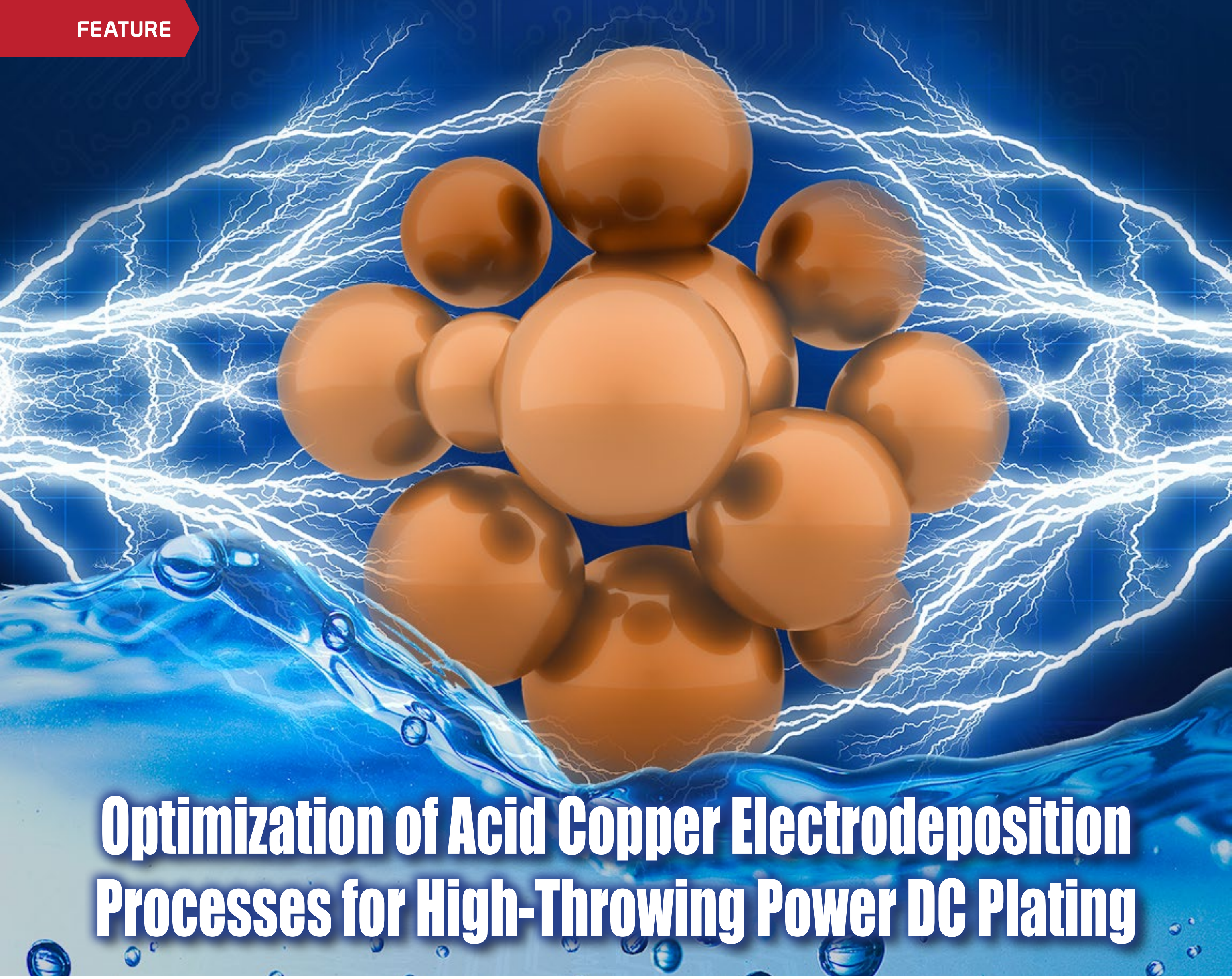

Optimization of Acid Copper Electrodeposition Processes for High-Throwing Power DC Plating

by Michael Carano
RBP CHEMICAL TECHNOLOGY

Introduction

Perhaps one of the three most fundamental aspects of printed circuit fabrication is the metallization and electroplating of through-hole vias and blind via interconnections. Ideally, one should also include fine-line imaging of increasingly smaller feature sizes and via formation, whether by mechanical or laser methods. Indeed, the foundation of technology roadmaps should, at the very least, encompass a discussion of line widths and spaces, PTH and blind via aspect ratios, and a metric that defines acceptability of plating uniformity and throwing power. These same parameters have been used for nearly four decades to quickly quantify the capability of a fabricator to profitably produce traditional boards. The ability to image conductor lines, and perhaps even more important, the insulating airspace between them, is considered a key characteristic. With surface mount components, a dramatic decrease in plated via hole diameter requirements occurred, and as a result, via holes have become simple vertical interconnections. Now, under competition from laser drilling, both drill bit and machine technology have driven mechanical holes capability much smaller.

In the most recent release of the IPC Technology Roadmap, PTH and blind via diameters and aspect ratios have been defined as to the technology sector where the boards are used. In order to provide a list of key attributes (layer counts, board thickness, number and diameters of vias, etc.) for the PCB, emulators are

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employed. Emulators (synthetic) are representations of a category of product, combining the attributes common to the type to avoid concerns about disclosure of specific company-proprietary designs. Technologists from around the world were asked to provide their respective view of the PCB technology required for the emulator. This exercise is critical in developing and understanding roadmaps. As an example, Table 1 below lists the minimum mechanical via hole sizes for the various emulators.

Table 2 depicts the maximum aspect ratio of mechanically drilled plated through-holes for the respective emulators.

The Challenge

It is quite clear from the two tables that there are rather high-aspect ratio vias that must be plated. It is understood that it is desirable to achieve as close to 100% throwing power as possible. At a minimum, market surveys have shown that for reliability, productivity, and performance purposes, a minimum of 80-85% throwing power is required. Further, process engineers desire to minimize plating on the conductor traces in order to minimize undercut and circuit width destruction due to final etching.

For purposes of this paper, throwing power is defined as the minimum electroplated thickness in the center of the PTH, divided by the thickness on the PTH surface (excluding copper

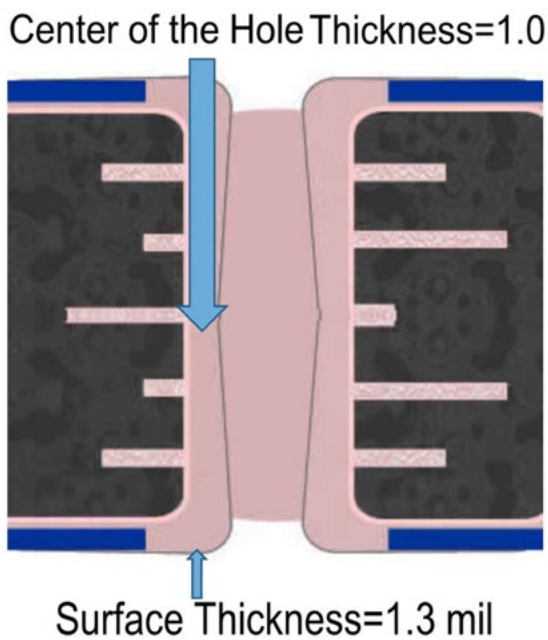

Figure 1: Throwing power: 1.0 mil minimum hole thickness and 1.3 mil surface thickness. Throwing power is 1.0/1.3 mil, or 77%.

EMULATORS	CURRENT 2015		LONG TERM 2020	
	RCG	SoA	RCG	SoA
Computer & Telecom	250	100	200	50
Consumer	150	70	100	50
Industrial & Auto (Portable)	275	175	200	150
Industrial & Auto (Product Bd)	200	100	200	75
Medical (Portable)	250	120	250	100
Medical (Product Bd)	200	200	125	100
Military (Portable)	200	100	150	100
Military (Product Bd)	250	75	200	50
Substrate or Module	175	50	165	25

Table 1: Minimum hole diameter for mechanically drilled vias (mm, rounded to whole number). (Source: IPC Technology Roadmap, 2015)

foil). Figure 1 illustrates the definition of throwing power.

While in Figure 1 the throwing power is 77%, one would prefer throwing power of 100%. Electroplating of high-aspect ratio through-holes becomes increasingly more difficult as via diameters decrease and board thicknesses increase. Figure 1 depicts a condition aptly named "dog-boning" for its thinness in the center of the via.

The following equation illustrates a model that provides insight into the difficulty factor encountered when aspect ratios increase. It is not as simple as it looks. As the model illustrates, board thickness has a much greater influence on degree of difficulty than does via diameter. Essentially, board thickness directly influences ohmic resistance through the via. Resistance is inversely proportional to plating propagation.

$$E = \frac{JL^2}{2KD}$$

Where:

E = Voltage drop down hole (energy lost)
J = Cathode current density
K = Solution resistance
d = Hole diameter
L = Length of hole

It is important to keep this in mind when designing plating processes for high-aspect ratio circuit boards. As circuit boards become more complex in their designs, more attention must be paid to plating cell design, plating chemistry, anodes and plating racks, electrical connections and solution agitation. This paper will also present various techniques on improving and enhancing throwing power for high-aspect ratio plated through-holes, with a focus on direct current (DC) plating.

Acid Copper Electroplating: Theoretical Aspects

In order to enhance plating uniformity (defined not only as plating thickness across the PCB surface but in the via as well), engineers should understand that there are several factors that influence plating uniformity. The Fishbone diagram below details in concise fashion those parameters that influence throwing power, plating distribution and overall quality of the finished printed circuit board.

EMULATORS	CURRENT 2015		LONG TERM 2020	
	RCG	SoA	RCG	SoA
Computer & Telecom	12	22	12.5	25
Consumer	6	13	6	20
Industrial & Auto (Portable)	6	12	8	12
Industrial & Auto (Product Bd)	9	14	9	20
Medical (Portable)	6.5	10	10	15
Medical (Product Bd)	9.5	10	11	12
Military (Portable)	10	20	13	25
Military (Product Bd)	10	16	11	20
Substrate or Module	1.0	1.0	2.0	2

Table 2: Aspect ratio, mechanically drilled hole via (max ratio).

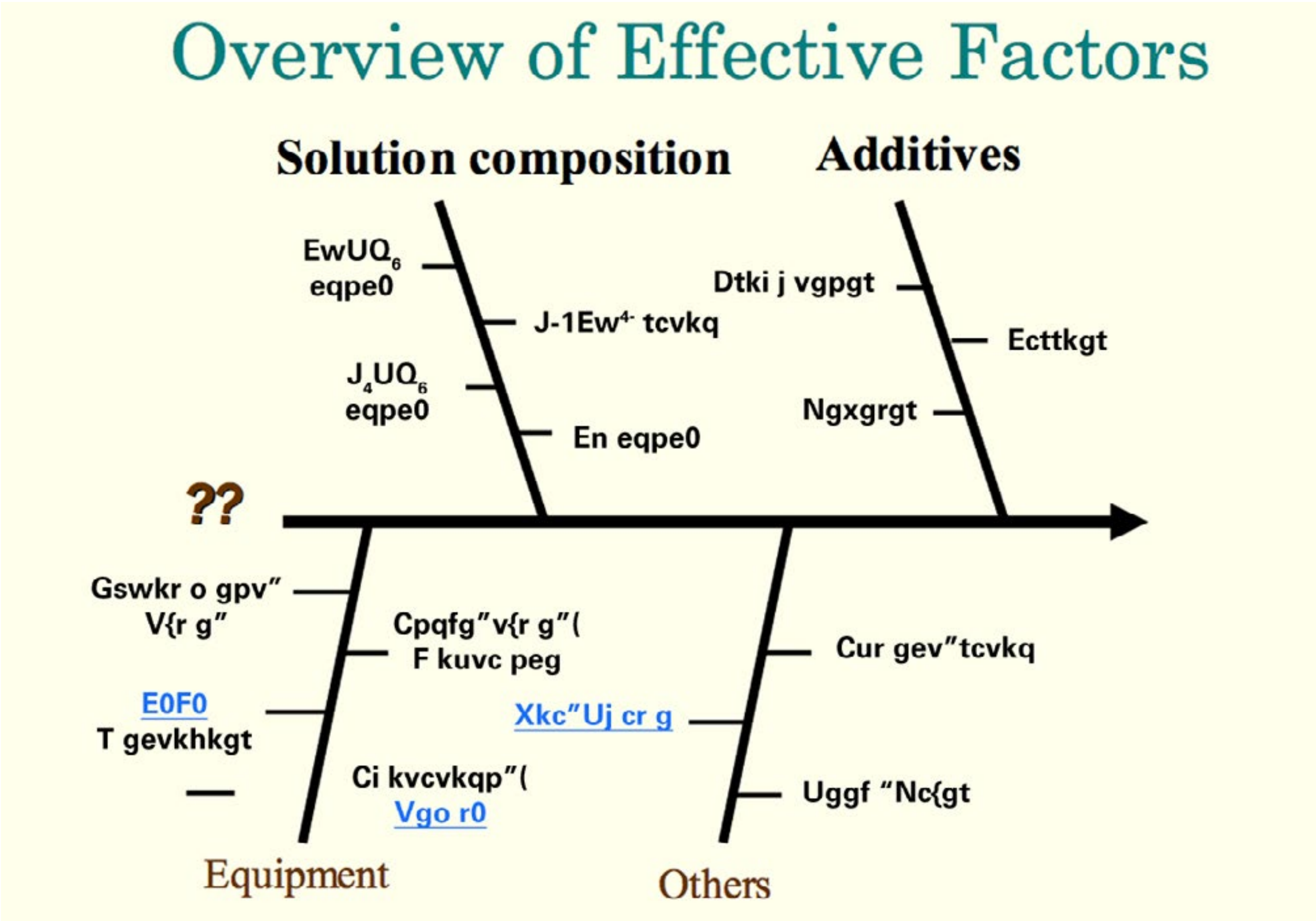

Figure 2: These factors and their influence on plating distribution will be presented throughout this paper.

Acid Copper Electroplating for High-Aspect Ratio PCBs: Practical Aspects

For any process engineer, getting a handle on the key elements involved in the process will provide the insight and understanding required to achieve optimum plating results. The first part of this equation is to recognize the relationship and interactions of the plating chemistry (inorganic and organic).

Influence of the Organic Additives and Plating Electrolyte (inorganic)

The organic addition agents utilized in the plating solution have an influence on plating distribution and throwing power under certain conditions. The additives distinctively influence this behavior when charge transfer and ohmic resistance dominate the plating system behavior. However, as the PTH diameter increases and the board thickness increases, ohmic resistance dominates and addition agents have less of an influence[2]. In this case, mass transfer of the plating solution into the vias is critical. However, with the higher-aspect ratio holes, mass transfer gives way to ohmic resistance. In order to compensate, one needs to reduce the cathodic current density and also reduce plating solution resistances. The latter is accomplished by increasing electrolyte conductivity, reducing resistances in plating cables and other cell design enhancements that will be mentioned in the next section. Since it becomes increasingly difficult to achieve near 100% throwing power in aspect ratio holes of 10:1 and above, the plating electrolyte must be set-up to maximize plating solution conductivity. This is accomplished by increasing the sulfuric acid concentration and reducing the amount of available copper ions in solution. Of course, one cannot reduce the copper ions in such a way that the limiting current density will be quite low. This is where mass transfer becomes increasingly important. And mass transfer is dependent on diffusion-the movement of ions and additives through the plating electrolyte.

Organic additives will also affect the grain structure, leveling and physical properties of the deposit. Strict control of the additive chemistry requires instrumentation such as cyclic voltammetric stripping (CVS) and perhaps ion chromatography. Additional agent imbalances will reduce the ductility of the copper deposit, thin plating at the knee of the via and poor leveling.

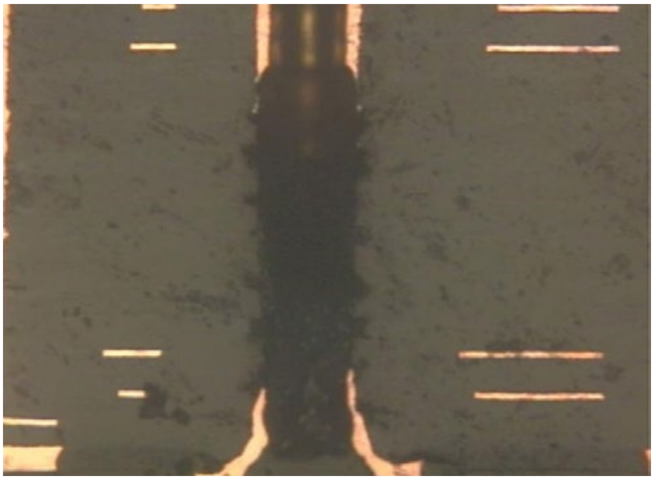

Figure 3: Air bubble entrapment in via leading to plating void.

Influence of Mechanical Aspects of the Process

In addition to the influence of the organic additives and the inorganic chemistry, there are several other factors that influence plating distribution and throwing power. One major influence is solution movement or agitation. Agitation influences mass transport. As one will recognize, the organic addition agents affect plating distribution and throwing power, among other attributes. And mass transport of the plating solution is key to "pushing" these additives from the bulk plating solution to the cathode (circuit board to be plated) surface. One can look at agitation as solution mixing and agitation at the interface of the cathode and solution boundary layer. Solution agitation of the copper plating electrolyte maybe accomplished with air agitation, eductors, solution impingement or cathode bar movement. The main purposes of agitation have been stated many times and include:

- Elimination of solution stagnation and dispersal of reaction products
- Increase of deposition rates by mass transfer enhancement
- Dissipation of heat at electrode/solution interfaces[1]

Air agitation suffers from three main disadvantages: It has a chemical oxidative action towards solution constituents; it is electrically resistive when present as a cloud or foam of bubbles; and, the general plating rate enhancement is modest despite several possible parameters for adjustment. The least appreciated characteristic is the resistivity, which can lead to an increase of electroplating power of 25–30% and is therefore a significant electrical cost factor. It also generates environmental pollution through dispersion of air bubbles. In addition, these tiny bubbles can lodge into the through-holes and blind vias, leading to a reduction in plating thickness or voids[1]. This micro-bubble void inducing condition is well-documented in the industry and can be seen in Figure 3.

Conversely, solution movement supplied by eductor agitation is much more effective than air. When agitation is supplied via eductors, the solution movement is significantly more uniform across the panel surface. One can describe this as 'laminar flow.' With air agitation, the solution is moving in a turbulent fashion and is often quite non-uniform. This turbulent flow creates areas within the plating cell consisting of dead spots, which appear as if there is no or very minimal agitation in that portion of the cell. This is a recipe for disaster. When this condition occurs, plating uniformity is not ideal and the cosmetics of the deposit as well as the physical properties suffer.

Eductors, on the other hand, can be implemented at a very low cost with respect to retrofitting any of the plating cells. This author has had documented success with respect to improving throwing power and plating distribution. More uniform plating distribution helps to reduce the plating cycle time (everyone likes higher productivity and efficient use of capital). Secondly, minimizing plating thickness on the surface of the board while enhancing throwing power in small diameter vias will provide less opportunity for circuit line width reduction due to etching. Fabricators should always keep this fact in mind especially as one migrates to 3 mil lines and spaces. Figure 4 shows an actual plating cell (without chemistry) with eductors.

Figure 5 shows a single eductor pod as a close-up. These eductors should be mounted on manifolds as shown in Figure 4. This type of agitation set-up requires a 2.5–4 HP pump for every 4000 liters of plating solution.

Of course, solution movement (eductor versus air agitation) cannot cure plating throwing power ills on its own. As mentioned above, there are other factors including the organic addition agents and the composition of the plating electrolyte itself. And many of these factors interact with each other. As the graph in Figure 6 below shows, when the organic addition agents (in this case the carrier component of the plating additives) are in the optimum concentrations, the throwing power is significantly better than when eductors are used to supply the solution movement. In this study, the circuit board test vehicle was 0.093 inches thick and the smallest via diameter was 0.008 inches. Cathode current density was set at 25 ASF (amps per square foot).

One should not underestimate the importance of plating cell design and geometry when it comes to optimizing throwing power and overall plating distribution. Factors such as anode-to-cathode distances, anode length and placement and plating rack construction/design greatly affect plating uniformity. With respect to rack design, a picture frame rack (multiple rack points around the periphery of the board) will provide more uniform current distribution as opposed to a rack with a few attachment points at the top or side of the panel.

In addition, anode length should be 3–4 inches shorter than the length of cathode. This will aid in mitigating excessive plating on edges of the panel.

With primary distribution, the electron potential field depends solely on cell geometry including anode length and placement (Figure 7). It is possible to use floating shields in the plating tank in order to divert current from those areas of the circuit board most prone to overplating.

Figure 4: Photo of plating cell with bottom up educators.

Figure 5: Close-up view of a single educator, also known as a pod.

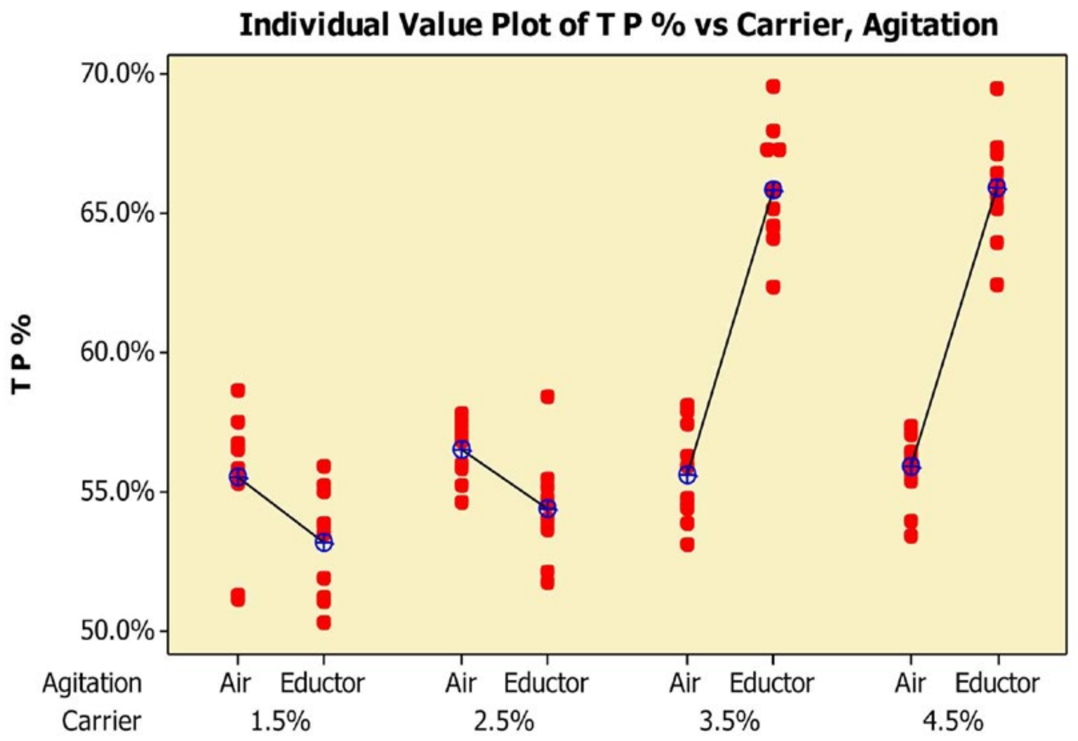

Figure 6: Influence of air versus eductors on throwing power.

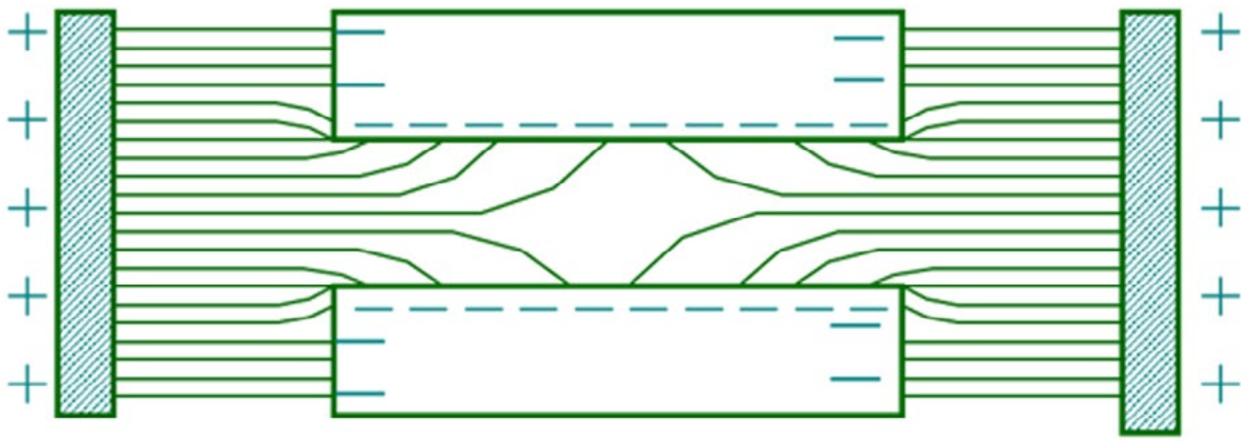

Figure 7: Current flux lines follow path of least resistance leading to over-plating and poor distribution.

Plating rack materials fabricated out of copper (Plastisol coated) provide more electrical conductivity than stainless steel material. This is an important fact for thicker panels and high-aspect ratio via holes.

Fortunately for plating difficult circuit boards, there is another factor to consider: secondary current distribution. Secondary current comes into play through a factor known as polarization. Polarization refers to the additional potential required above the equilibrium potential to drive the deposition of the metal to be plated. (Keep in mind that factors involved in primary current distribution should be op-


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timized in addition to manipulating secondary current distribution.) The potential is determined by Ohm's Law, which is the solution resistance between the anodes and cathodes. Additional resistances arrive through the voltage required to corrode the anode and the resistance required to reduce the metal ions to metal at the cathode.

In order to improve throwing power and plating uniformity, one can increase the conductivity of the plating electrolyte and increase the polarization. Polarization and conductivity are both dependent on solution operating temperature, solution agitation and cathode current density. The main consideration is recognizing that plating distribution across the surface of a printed wiring board panel and from the surface of the panel through the holes will vary due to resistances. By mitigating the effects of these resistances, plating distribution is improved.

The Importance of Quality Anodes-Care and Maintenance

It is surprising how little attention is paid to the quality and maintenance of the copper anodes. The grain structure is the most critical characteristic of copper anodes. This structure is predicated on the manufacturing process of the anodes, which in turn determines the grain structure of the copper. Fine grained size of the copper is the preferred orientation. The uniformity of grain size and the dispersement of the phosphorous along the grain boundaries will aid in the orderly dissolution of the copper. Large grained copper anodes dissolve unevenly, leading to heavy sludging and potential for impurities and particulate matter to enter the plating solution. An example of different anode quality is shown in Figure 8.

There are three different anodes from three different suppliers, each claiming quality anodes for printed circuit fabrication. Note that each anode looks much like the other.

Each anode ball was cut with a diamond saw to reveal structure. Figure 9 shows an SEM of each of those. Clearly there is a distinctive difference among the grain structures and phosphorous (shown as the dark areas). To read more about anode manufacturing and quality, see Reference 3.

Each anode ball was cut with a diamond saw and given a light etch to reveal. Figure 9 shows an SEM of each of those. Clearly there is a distinctive difference among the grain structures

Figure 8: External view of three anodes from three different manufacturers.

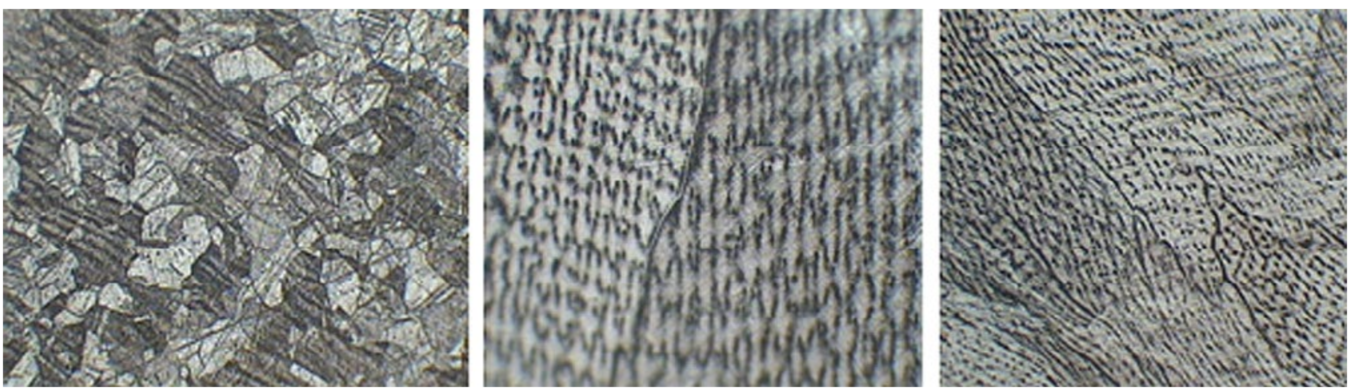

Figure 9: Manufacturer 1 (left), Manufacturer 2 (middle) and Manufacturer 3 (right).

and phosphorous dispersion (shown as the dark areas). As one views each of the structures, the differences are remarkable.

The anodes from Manufacturer 1 show large and uneven grain boundaries. In addition, the phosphorous is unevenly distributed. This leads to high organic additive consumption, anode sludge and plating roughness. The anodes from Manufacturer 2 and 3 are the ideal quality required for PCB plating for high-aspect ratio holes.

Summary

While electroplating PCBs with aspect ratios greater that 12:1 is probably best accomplished with periodic pulse reverse plating, direct current plating will produce high-quality circuit boards with aspect ratios up to 12:1. This requires that several parameters be optimized for throwing power and plating distribution. These parameters include plating cell design, high quality copper anodes, solution agitation with use of eductors, anode length and placement and proper selection of organic plating additives and the electrolyte (inorganic chemistry). **PCB**

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2. Yung, E.K. and Romankiw, L., "Fundamental Study of Acid Copper Through-hole Electroplating Process," Symposium on Electrodeposition Technology, The Electrochemical Society, Pennington, New Jersey, pages 612–635.

3. Chuck Walker and Steve Doyle, Electroplating: The Importance of Copper Anodes, Finishing World.

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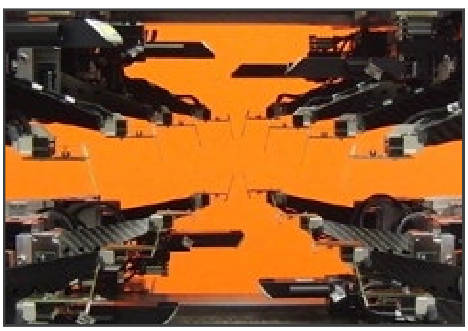

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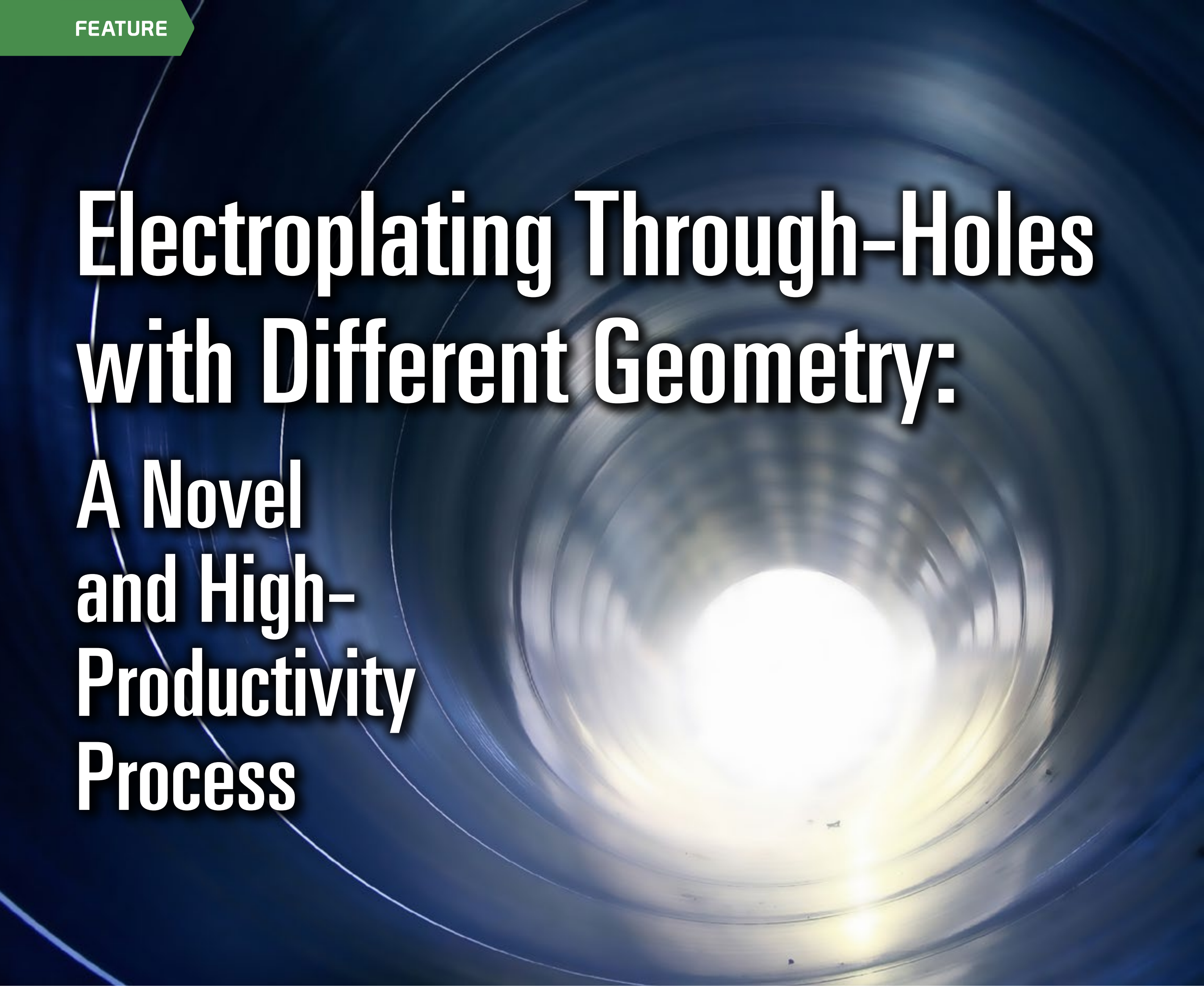

Electroplating Through-Holes with Different Geometry: A Novel and High-Productivity Process

by Elie Najjar, Leon Barstad, Jayaraju Nagarajan, Marc Lin, Maria Rzeznik and Mark Lefebvre
DOW ELECTRONIC MATERIALS

Abstract

Microfill™ through-hole fill (THF) electrolytic copper is a new process designed to offer outstanding through-hole fill, particularly for substrates intended for use as core layers in build–up applications, producing planar, solid copper plugs in high-volume production plating equipment. This technology is intended to replace resin or paste plugging, and offers many advantages, including improved reliability, higher electrical and thermal conductivity, increased productivity and reduced process costs.

This paper describes a novel copper through-hole fill electroplating process designed for use with insoluble anodes and direct current (DC) rectification. The copper through-hole fill chemistry is formulated to operate over a broad range of operating conditions, and offers end-users outstanding production flexibility in either panel or pattern plate operating mode.

The paper addresses electrolytic copper through-hole filling performance for a variety of substrate thicknesses and hole diameters. The impact of the hole formation method and hole quality on filling ratio and void formation will be discussed. In this work, production scale tests were performed on 100 µm and 200 µm thick substrates. The impacts of varying current density and solution flow on hole filling were examined. With optimized deposition condi-

tions, including on-line additive analysis, void-free, highly planar through-hole filling and excellent bottom-up blind microvia filling with low surface copper deposition thickness were demonstrated.

Introduction

Portability of consumer electronics has become the primary driver for the ever-increasing circuit density of today's printed circuit designs. Based on the small dimensions of these devices, through-hole and blind via diameters are typically in the 75–150 µm range. Performance improvement and process cost reduction make through-hole filling technology with copper an excellent approach, rather than the conventional plated through-hole.

Prior to the development of electrolytic copper through-hole filling, substrates for such applications were electroplated with a conventional through-hole process, then plugged with an epoxy material. Following these steps, additional planarization, re-metallization and electrolytic copper capping processes were required before the build-up process steps could begin.

Use of electrolytic copper through-hole filling eliminates several of these manufacturing steps and offers a number of additional advantages over the conventional build-up process by enhancing the thermal and electrical conductivity of the interconnections, and by reducing overall costs.

Inorganic Components

The vast majority of through-hole fill electroplating baths are based on acid sulfate electrolytes, containing copper sulfate (the primary source of cupric ions), sulfuric acid (for solution conductivity) and chloride ion (as a co-suppressor). Of these components, sulfuric acid, typically at concentrations below 60 g/L, has the most significant effect on achieving good through-hole filling. A plating solution with elevated acid concentration leads to conformal plating causing poor filling performance.

Organic Components

Acid copper sulfate system operated without additives typically yield deposits of poor physical properties. Organic additives, typically consisting of materials described as suppressors, brighteners, and levelers, are therefore used to further refine deposit characteristics. Via fill plating systems were not designed for through-hole filling applications. The organic components and their respective concentrations used to achieve bottom-up filling in blind microvias are less effective for initiating fill in the very different geometry of a through-hole. Therefore, a novel organic package was developed specifically to favor the fill mode essential to completely plug the through-hole with copper. While an accelerated bottom-up fill mechanism is the critical aspect of blind microvia filling, through-hole filling requires initial creation of a "butterfly" structure, formed by rapid copper deposition at the center of the holes. This change in geometry is the critical first step in achieving good copper through-hole filling.

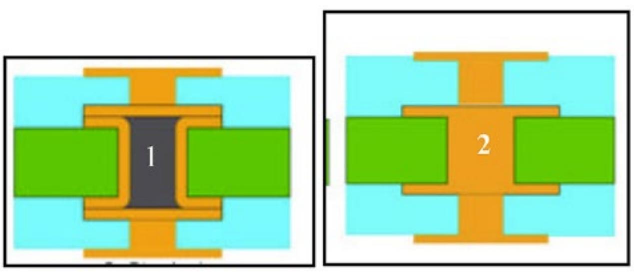

Figure 1: Through-hole plug: conventional vs. current technology.

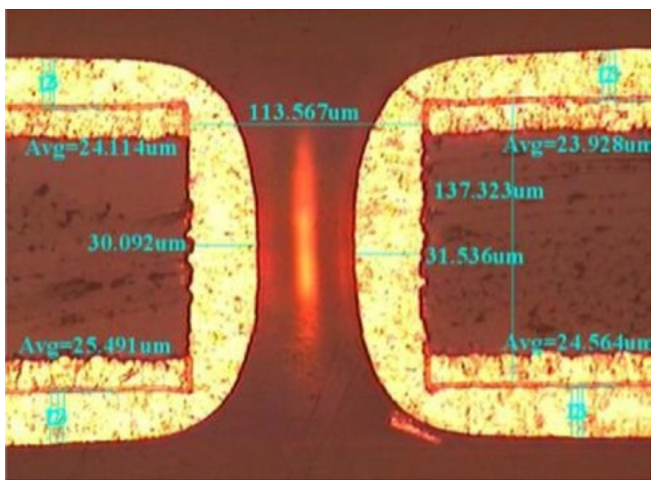

Figure 2: Conformal plating of a through-hole.

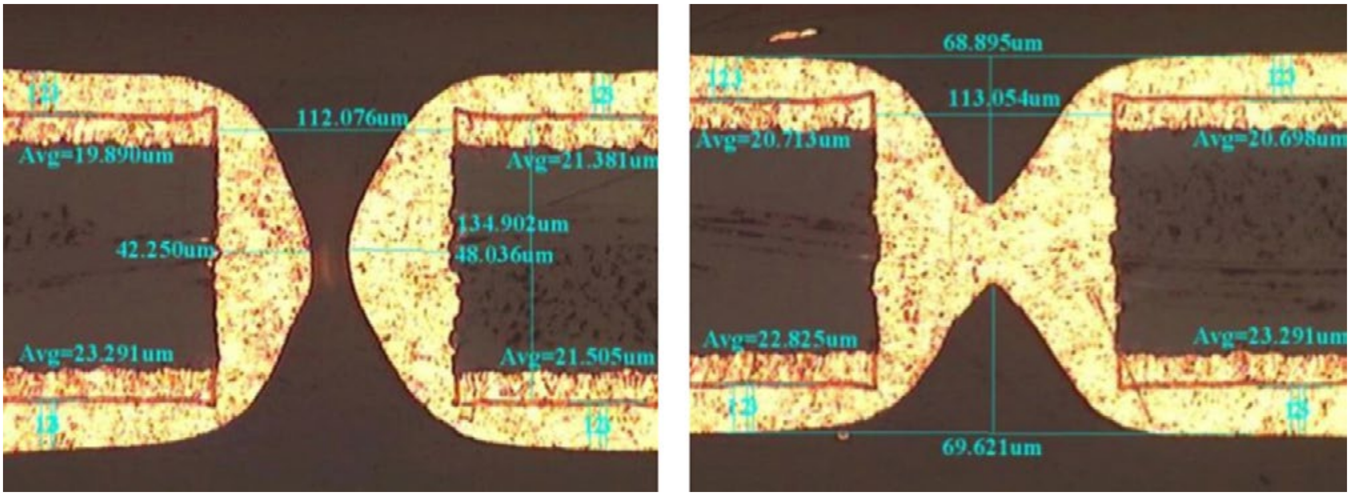

Figure 3: Butterfly structure leading to subsequent via formation.

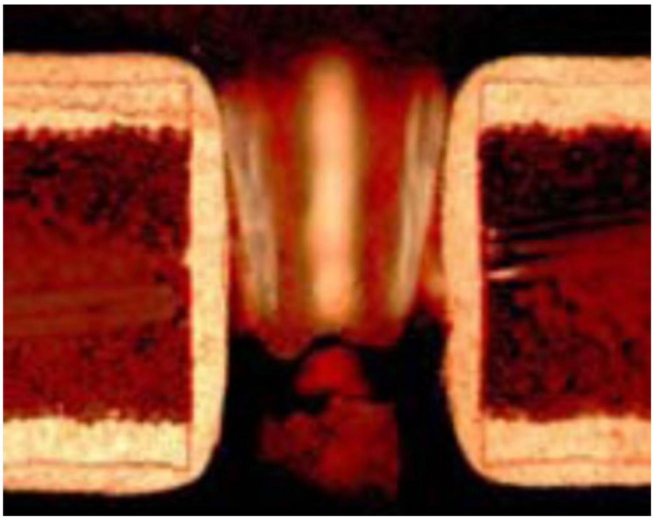

Figure 4: Mechanically drilled hole (100 μm x 100 μm).

In theory, once the transition from cylindrical through-hole to double blind via has taken place, a microvia fill system could be used to complete the filling. Although it is possible to use two different chemistries to achieve through-hole fill, most printed wiring board manufacturers have chosen to adopt a single chemistry/one step approach to through-hole fill, regardless of the hole shape. However, manufacturers may be forced to modify their approach as new challenges in hole size, planarity and void requirements emerge.

In order to appreciate all the aspects of the "single chemistry does it all" challenge, it is useful to discuss the effects of different through-hole geometries on through-holes fill.

Through-Hole Shape

Currently, blind vias, buried vias and though-holes are used in the fabrication of high-density interconnect designs.

Mechanical drilling has been the conventional way to form holes and this process is still the basis for most printed circuit board manufacturing.

In addition, through-holes can be formed using either one-sided (OSLTH) or double-sided laser drilling (DSLTH). The shape of such holes is not perfectly cylindrical, as shown in Figure 5 below. The tapered hole-wall profiles make such holes somewhat easier to fill with copper than the more cylindrical mechanically drilled holes. As a result of this difference, mechanically drilled holes may show a highest tendency for seam void formation than double-sided laser drilled through-holes.

One-sided laser drilled holes (OSLTH) can be prone to voiding due to the drilling process, which may cause excessive differences in hole diameter between the top and bottom of the panel.

Although panel thickness also has a major impact on the ability to achieve good fill without voiding, overall DSLTH are easier to fill and less prone to void formation.

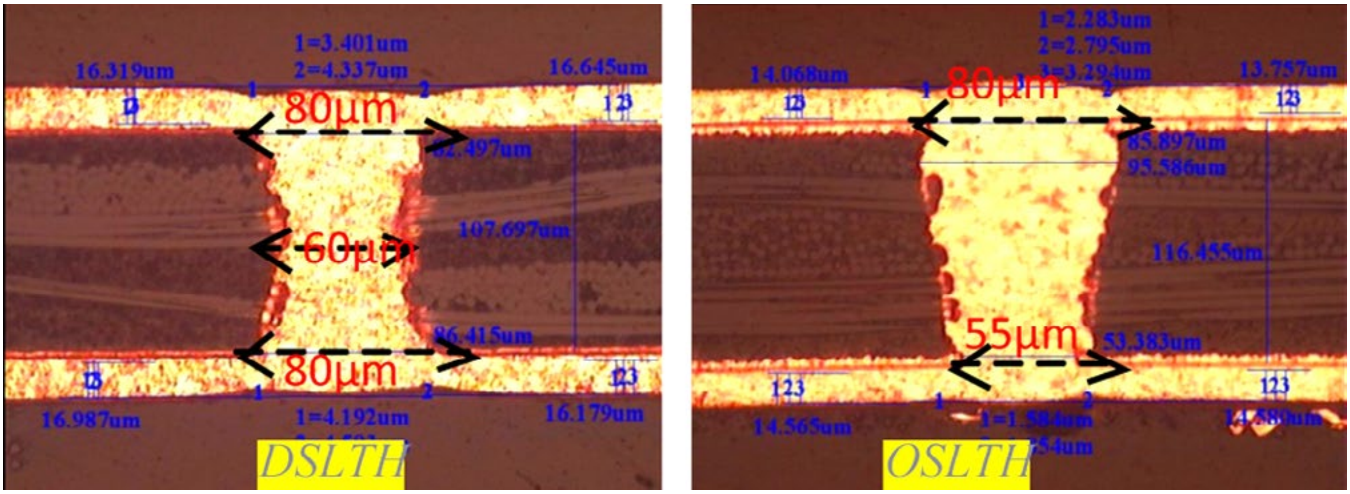

Figure 5: Double-sided and one-sided laser drilled holes.

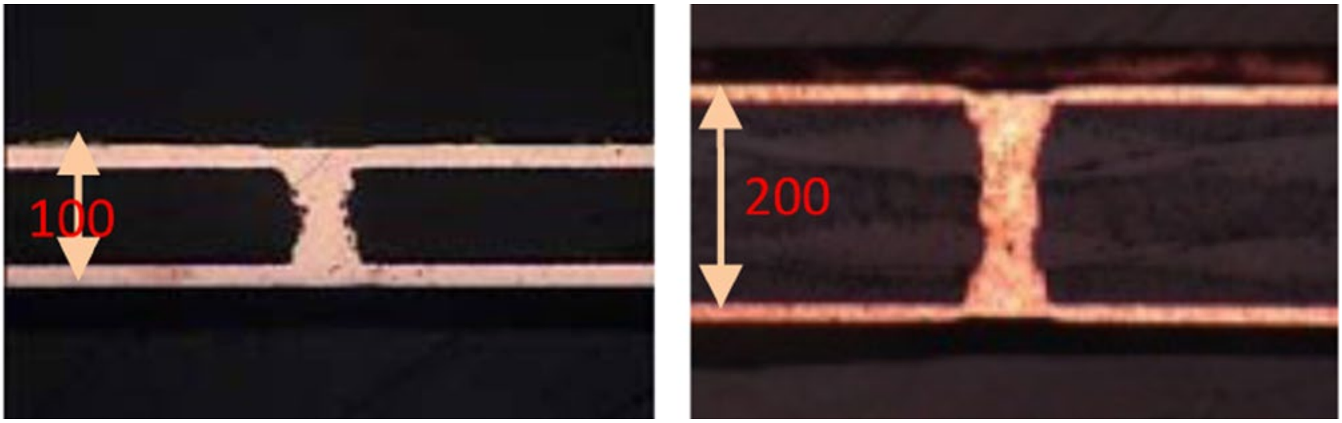

Figure 6: Double-sided laser drilled through-hole in 100 µm (left) and 200 µm (right) thick panels.

Chemistry Development

To develop a new DC-based plating bath that can achieve good hole filling performance with minimal voiding, development efforts were directed towards the interaction of brightener and leveler additives. Levelers are preferentially adsorbed at areas of higher curvature such as the entrance of the hole, where mass transfer is enhanced, and thus filling behavior is strongly influenced by convection.

The competitive adsorption between brighteners and levelers result in a concentration gradient along the hole wall, with the leveler-rich corner effectively inhibited relative to the brightener rich center, resulting in the non-uniform plating rate required for through-hole filling. Even with the use of a strong leveler, the leveler concentration has a huge impact on hole-filling capabilities and on the deposit appearance and surface morphology (roughness and resistance to formation of nodules).

For instance, a low leveler concentration will lead to a lack of inhibition at the entrance of the holes, with the result being excessive plating rate at the knees, leading to formation of seam voids. An excessive leveler concentration will negate the ability to selectively inhibit only those areas with high curvature, resulting in a conformal deposit and increased risk of nodule formation.

Electrochemical studies confirm that the adsorption of leveler on the hole openings and

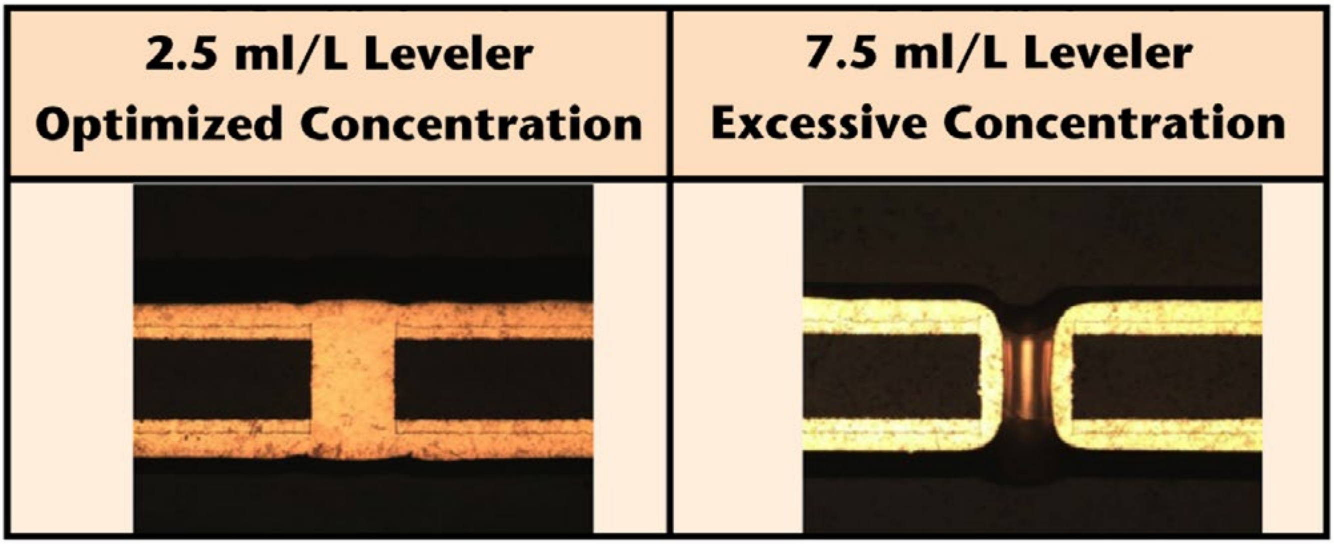

Table 1: Filling performance as a function of additive concentration.

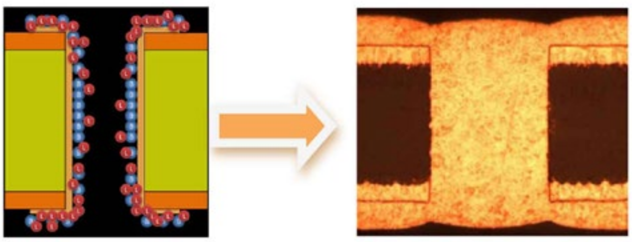

Figure 7: Optimized THF copper chemistry.

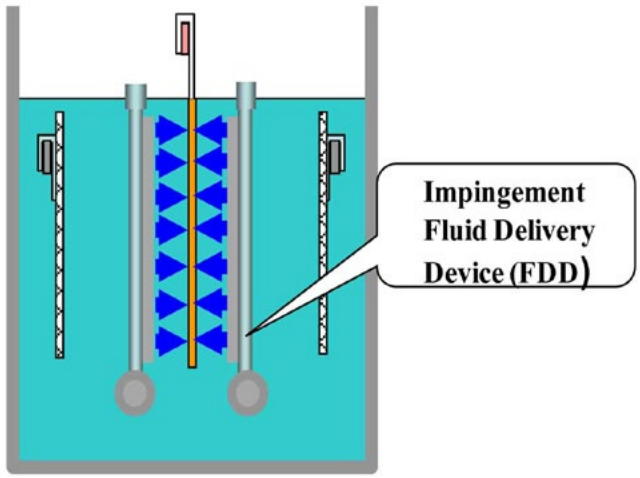

Figure 8: Side view of jet impingement plating cell.

outer parts of the through-hole walls are mass transfer dependent. Furthermore, both electrochemical and plating studies indicate that the inhibiting strength of levelers are also dependant on the leveler concentrations, as shown in Table 1.

After extensive research and development efforts, a well balanced additive package was developed to achieve the desired through-hole filling performance.

This process was developed to work with solution jet impingement and insoluble anodes in both vertical batch mode and vertical in-line and horizontal conveyorized plating equipment. A wide variety of equipment design features that further enhance though-hole fill plating performance may be incorporated. These include the use of engineered fluid delivery devices such as eductors or nozzles designed to create optimized flow impingement on panel surfaces.

Through-Hole Fill Performance Matrix

Through-hole fill plating performance, like blind microvia filling, may be characterized by the calculation of the dimple depth or bump height. Dimple depth is the most commonly used metric to quantify both through-hole and via plating performance. Depending on customer and application, void area (Figure 9) may also need to be determined. Customer specifications for void area are typically expressed as % void, that is, void area/hole area.

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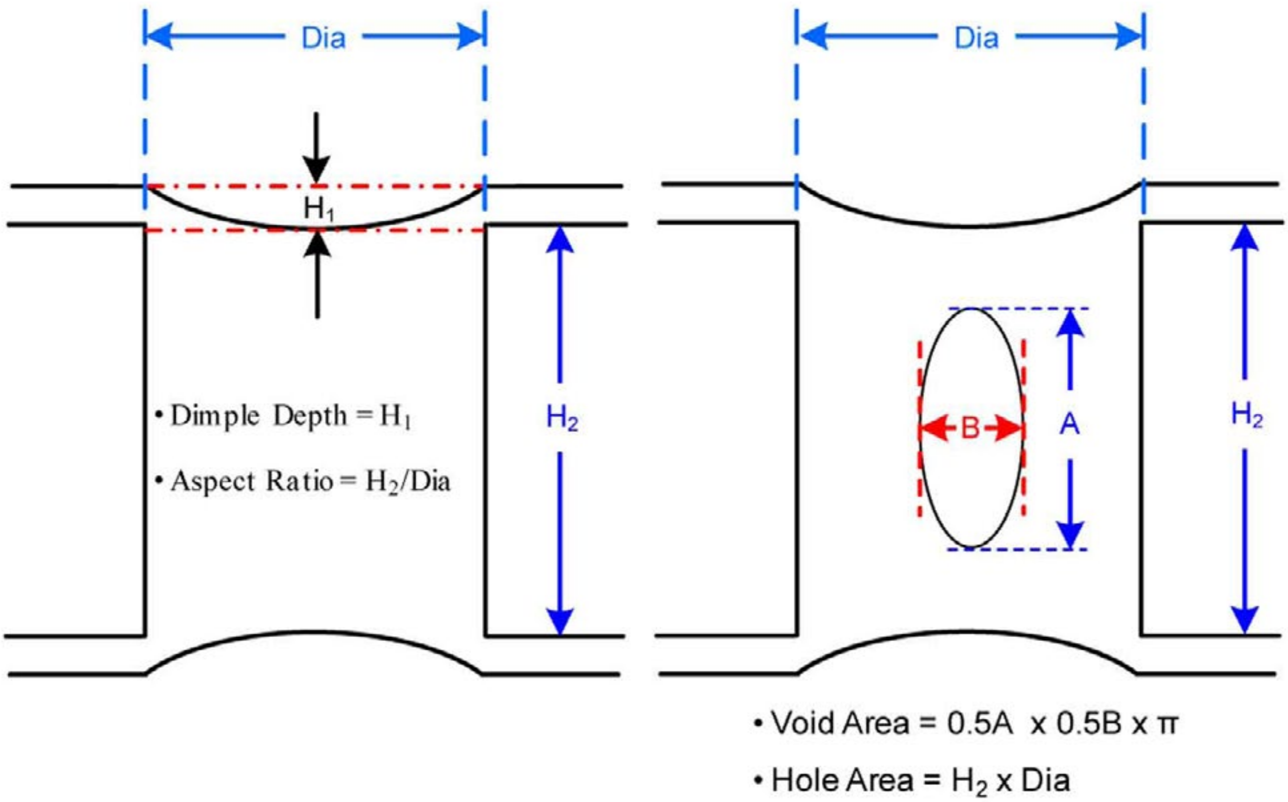


Figure 9: Dimple and void measurements.

Parameters	*(100μmx100μm)*	*Parameters*	*(100μmx100μm)*
CD: 2 ASD Cu: 25μm Electroless Thickness : 45 μinches		CD: 2.5 ASD Cu: 25μm Poor Coverage	
CD: 2 ASD Cu: 25μm Electroless Thickness : 20 μinches		CD: 2.5 ASD Cu: 25μm Good Coverage	

Figure 10: Plating performance as a function of electroless type and quality.

Impact of Substrate Condition and Pretreatment

The thickness, coverage and surface condition of the electroless copper metallization layer applied to the panel prior to the through-hole filling process has a profound impact on through-hole filling and plating capability. Discontinuous or overly thin electroless copper deposits will not electroplate as reliably as thicker, more uniform deposits. Oxidation of electroless copper can also adversely affect filling performance. Internal data has shown that, in particular, aged electroless copper has an unfavorable impact on process consistency. Proper control of pretreatment processes also plays an important role in achieving good hole filling. A typical process sequence uses acid cleaner and acid dip steps to ensure that copper surfaces are completely wetted and free of contamination prior to the subsequent copper plating step.

Impact of Process Agitation and Current Density on Hole Filling

Fluid delivery and flow agitation have a significant impact on hole filling performance, particularly in the presence of a leveler components. To understand the effect of agitation on hole filling, solution flow rate was varied in a

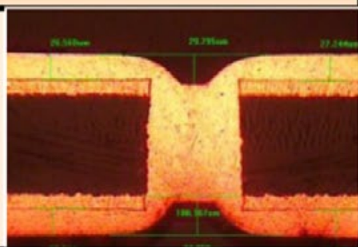
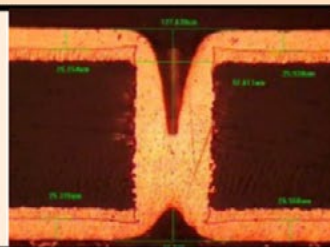
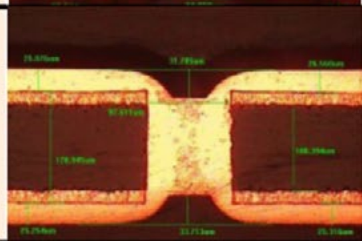
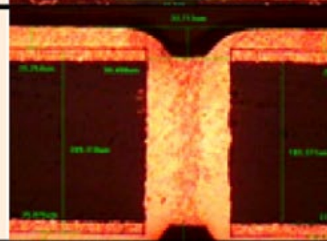
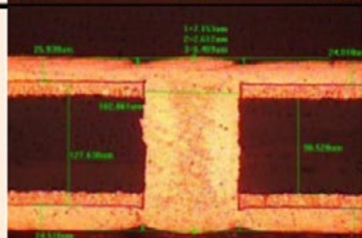
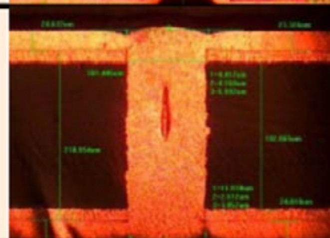
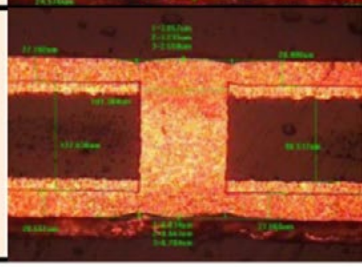
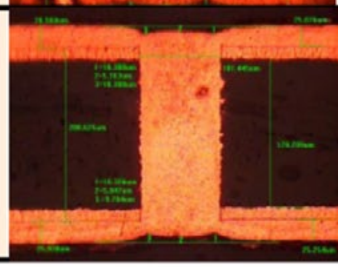
Flow Setting	100 mm x 100 mm	100 mm x 200 mm
High Flow		
Medium Flow		
Low Flow		
Flow Ramp		

Table 2: Plating performance as a function of flow conditions.

series of plating experiments performed in vertical continuous pilot plant plating equipment at Applied Equipment Limited (AEL) and NanYa (Taiwan).

The effects of both these parameters on filling performance were significant, with the results showing that the impact of solution flow rate is the strongest. While lower levels of solution flow rates were found to improve hole filling performance; depending on application, this improvement sometimes came at the price of seam void formation. A flow ramp scheme, accompanied by good wetting during pre-cleaning, reduced void formation while maintaining good hole filling performance. It is imperative that agitation parameters be carefully chosen to match plating cell design and application. It is also important to note the positive value of current density ramp accompanied by flow ramp on reducing void formation.

A similar test was then conducted in which current density (CD) was varied.

The intention of this test was to demonstrate the broad capability of the process that has been developed. Table 3 shows the effect of current density on through-hole filling performance. Consistent filling was achieved across a wide range of current density.

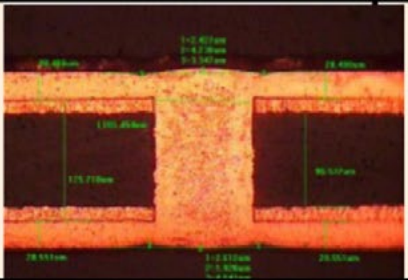
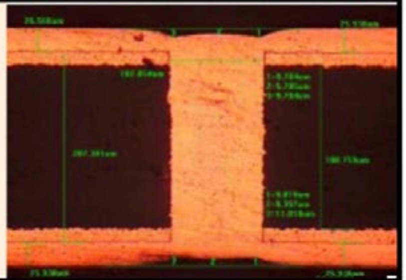
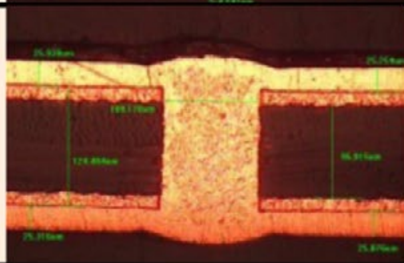
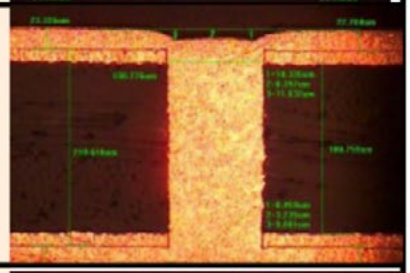
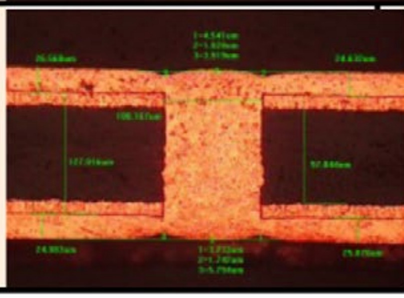
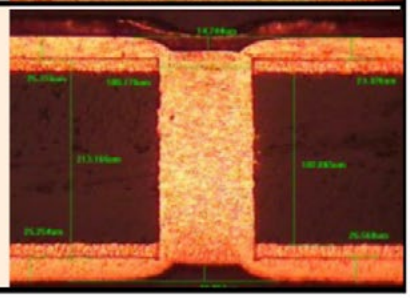
CD (ASD)	100 MM X 100 MM	100 MM X 200 MM
CD = 1.5		
CD = 2.0		
CD = 2.5		

Table 3: Plating performance as a function of CD.

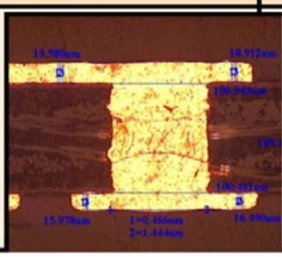
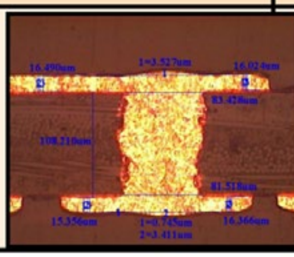
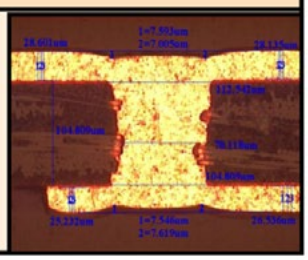
100µm x 100µm Mechanical Drilled Through Hole	80µm x 100µm DSLTH	100µm x 100µm DSLTH
		

Table 4: Pattern plate through-hole fill.

Process Performance

Applications using the finalized Microfill THF bath require excellent through-hole filling performance combined with good surface appearance. These targets must be achieved and maintained as the bath is cycled. To evaluate aged bath performance, test panels were processed in a vertical batch pilot scale plating

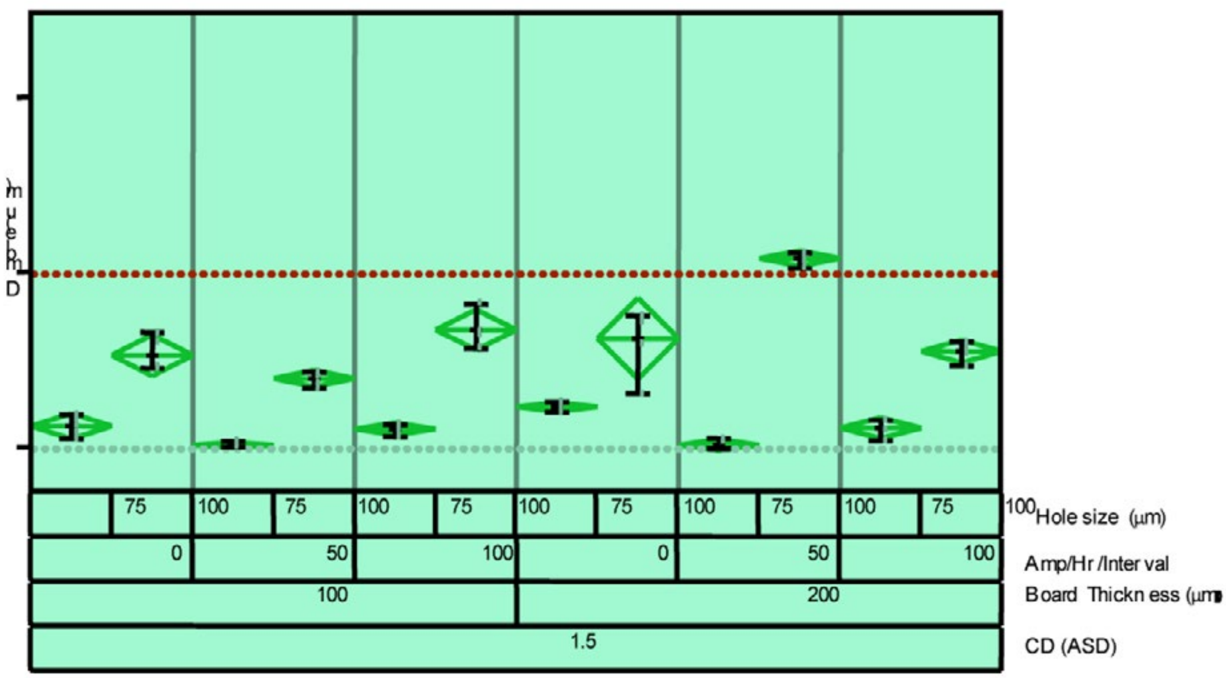


Figure 11: Through-hole dimple depth as a function of bath age and panel thickness in vertical batch plating cell.

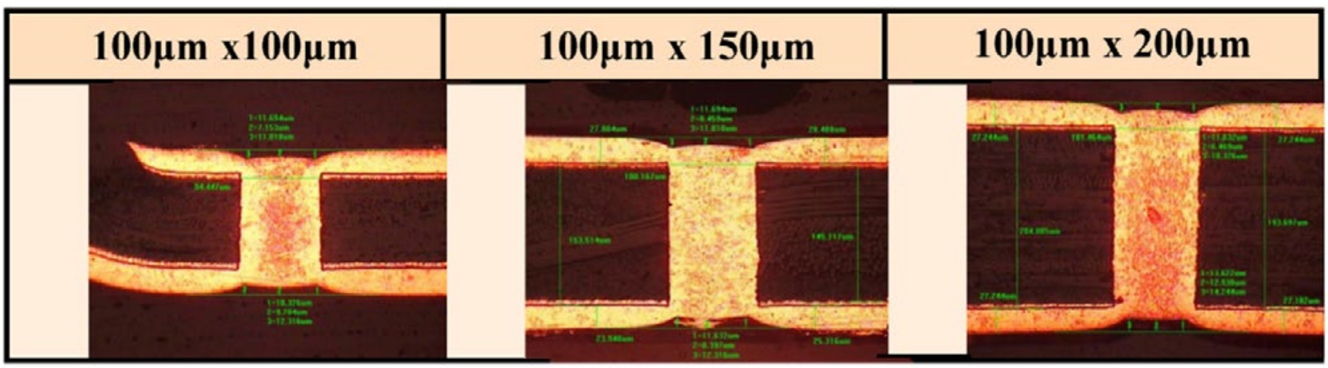


Table 5: Deep holes filled using the Microfill THF bath.

cell at bath ages from 0 to more than 100A.h/L. Consistent dimple depth of less than 10 µm was maintained with board thickness of 100 µm and 200 µm.

This process may be used in either panel or pattern plate processes. Table 4 demonstrates the capability of the process to fill through-holes when used in a pattern plate mode.

Table 5 shows results of tests performed in AEL equipment of deep through-hole filling, which reveal the capability of the Microfill THF process. This test was performed at 2.5 ASD with a copper surface deposition target of 25 µm. All holes were fully filled with copper with an acceptable dimple depth of < 12.0 µm.

Table 6 also demonstrates that the bath can also be utilized for the metallization of blind microvia (BMV) with surface copper thickness of less than 15 µm. Bump formation on top of the blind microvias can be minimized by modifying such plating parameters as solution agita-

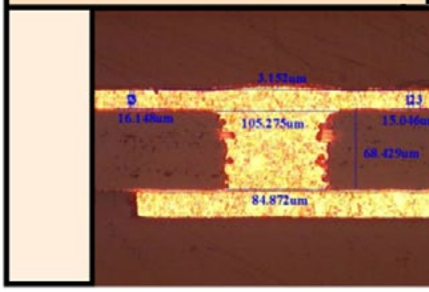
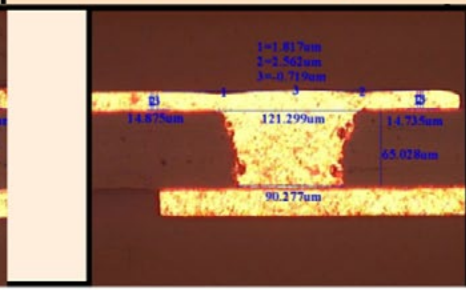
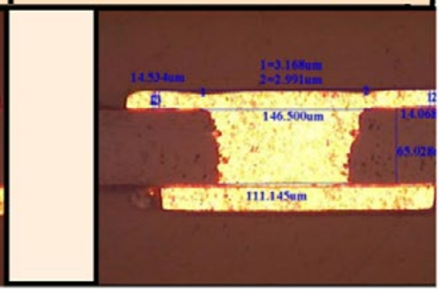
80µm x 65µm 1.5ASD / 15.0 µm	100µm x 65µm 1.5ASD / 18.0 µm	125µm x 65µm 1.5ASD / 15.0 µm
		

Table 6: BMV performance of Microfill THF bath.

CD (ASD) / Panel Thickness	Defects/ Total Holes Inspected	Cross Section
2.5 / 100µm	0 / 220	
2.5 / 200µm	0 / 220	

Table 7: Filled through-hole interconnect reliability.

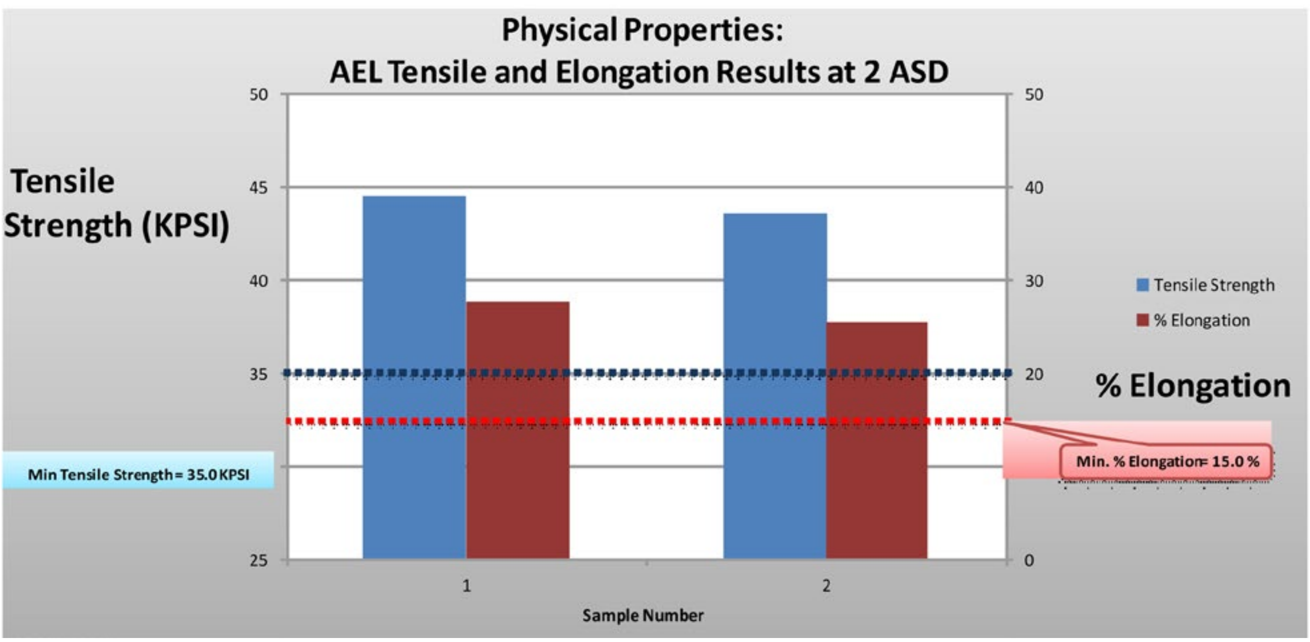


Figure 12: Deposit physical properties at 2 ASD.

tion and current density. Based on these results, this system could be utilized for BMV plating for flip chip application.

Process Reliability and Physical Properties

To establish through-hole fill reliability, cross sections were prepared after solder floating six times at 288°C per IPC procedure. The holes were then inspected. No cracks in the copper deposit or other defects were detected.

The Microfill THF bath provides consistent deposit physical properties from a bath cycled up to 100 A.hr/L. Tensile strengths above 35 kpsi and elongations in the range of 20–30% were measured for deposits plated over a range of bath ages.

Summary

A novel DC through-hole filling process was formulated for high-volume HDI and substrate core layer metallization production. The process yields high quality results over a wide current density range. The process has already been commercialized at a number of customers and it is anticipated that there will be substantial future growth in adoption of this technology to fill through-holes. This 'single chemistry does it all,' in combination with optimized plating conditions and plating equipment, is compatible with all though-hole geometries. The plated copper has excellent physical and mechanical properties, with a bright and leveled surface. This formulation is intended to be used with either vertical or horizontal inline jet impingement equipment in both panel and pattern modes. All organic additives can be monitored and controlled by conventional CVS analysis techniques. Moreover, Dow Electronic Materials is currently working with ECI Technology and AEL to introduce ECI's online chemical monitoring systems. This will provide analysis capabilities for front-end plating applications in high-volume manufacturing fabs. The analytical techniques incorporated in the on-line analysis will provide complete chemical metrology solutions to meet the stringent specifications necessary for such applications. This approach allows for reduction of chemical reagent consumption, drastically decreases maintenance and waste generation, while increasing overall operational efficiency and reliability. **PCB**

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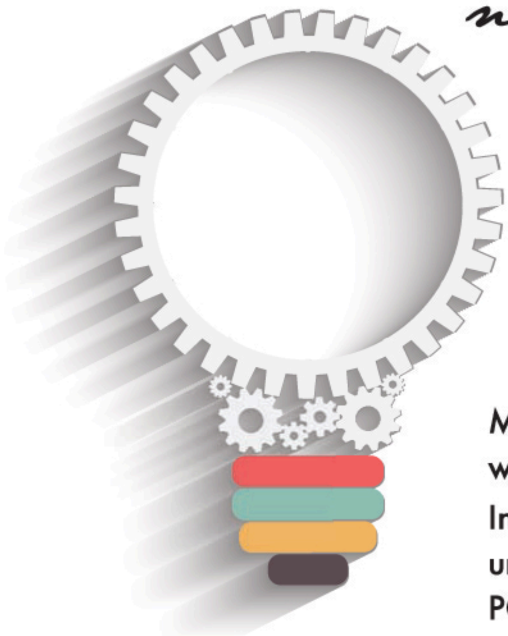

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Market Highlights

Optical Components Market Growth Picking up Again in 2015

LightCounting's analysis shows that optical components market has been growing at 8–12% per year on average over the past five years, but slowed during the second half of 2014. Recent reports from leading suppliers indicate that market growth picked up in Q1 2015, and LightCounting expects that the market will reach a new record in Q2 2015.

Smart Grid Sensors Market to Hit $350M in 2021

The market for smart grid sensors is set to rapidly expand in the coming decade, with revenues growing nearly ten-fold, from 2014–2021, according to IHS Inc. Based on information in a new study from IHS Technology, the market for smart grid sensors is centered in North America.

State of U.S. Manufacturing After the Recession

Since the economic recovery started in 2009, the U.S. manufacturing sector generally maintained a 12% share of GDP over the five years ending in 2013. The sector's performance was impressive when compared with other major advanced countries that experienced similar declines and early recoveries in manufacturing production.

Flexible Batteries Market Attracts New Investments

After years of slow progress from small companies, flexible batteries now have the attention of big brands such as Apple, Samsung, LG Chemical, Nokia and STMicroelectronics, who are set to drive the flexible battery market from US$ 6.9 million in 2015 to over US$ 400 million in 2025 according to IDTechEx.

Next-Gen Smart Lighting Systems Revenues to Hit $1B by 2020

In a new report, "Smart Lighting Market Opportunities: Smart Bulbs and the Rise of Local Lighting Intelligence," NanoMarkets concludes that the market for these new systems will reach just over $1 billion by 2020.

Gartner Reveals Vertical Industry Trends in SEA's Thriving Markets

"Some might argue that given recent political, financial and climate challenges, Southeast Asia is a risky proposition," said Venecia Liu, research vice president at Gartner. "However, Gartner believes that Southeast Asia's economic development and growing consumer demand mean that its growth potential outweighs the risk."

Flexible Display Market to Hit $30B by 2025

In the newly published "Flexible, Curved, and Bendable Display Technologies and Market Forecast 2015 Report," (Second Edition), Touch Display Research analyzed more than 10 display technologies and more than 14 applications of flexible displays, and the report shows how the flexible display market is accelerating.

Smart Wearable Healthcare Devices Market to See Significant Growth

The Technavio report emphasizes the increased use of smart wearable devices for tele-home healthcare. Monitoring many patients in hospitals can be a tedious process because of the lack of adequate resources. Smart wearable devices enhance treatment and monitoring processes by saving time and reducing healthcare costs.

IoT Data to Exceed 1.6ZB in 2020

A new report from ABI Research estimates that the volume of data captured by IoT-connected devices exceeded 200 exabytes in 2014. The annual total is forecast to grow seven-fold by the decade's end, surpassing 1,600 exabytes—or 1.6 zettabytes—in 2020.

Tech Transfer Provided $1.8T to US Economy

The report, "The Economic Contribution of University/Non-profit Inventions in the United States: 1996–2013," estimates that, during this 18-year time period, academia-industry patent licensing bolstered U.S. gross industry output by up to $1.18 trillion, U.S. gross domestic product (GDP) by up to $518 billion, and supported up to 3,824,000 U.S. jobs.

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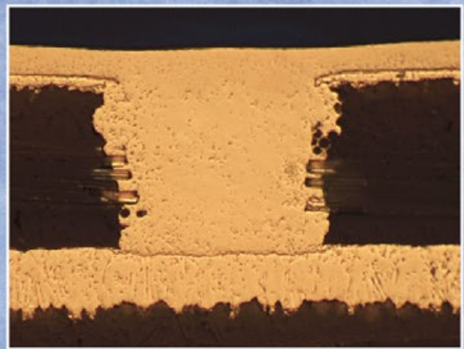

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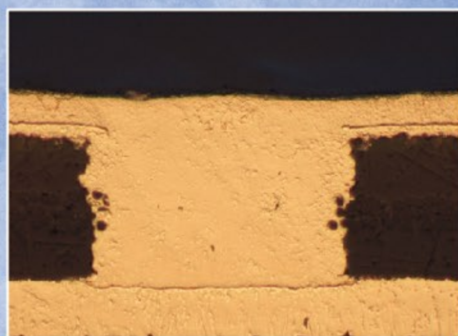

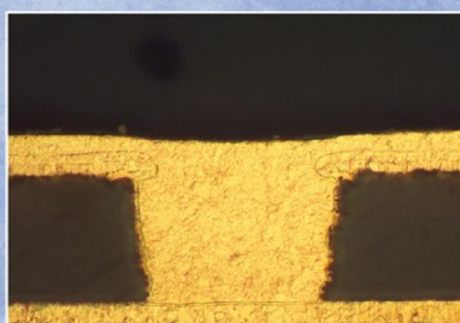

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by George Milad
UYEMURA INTERNATIONAL CORPORATION

Electroless nickel/electroless palladium/immersion gold (ENEPIG) is sometimes referred to as the universal finish, because of the versatility of its applications. It is a multifunctional surface finish, applicable to soldering and wire bonding (gold, aluminum, copper and palladium clad copper). In addition, it is also suitable as the mating surface for soft membrane and steel dome contacts, low insertion force (LIF) and zero insertion force (ZIF) edge connectors, and for press-fit applications. ENEPIG is formed by the sequential deposition of electroless Ni (120–240 µin) followed by 2–12 µin of electroless Pd with an immersion gold flash (1–2 µin) on top.

Chemical Definitions

Electroless Process: This chemical process promotes sustained deposition of a metal or metal alloy onto the PWB surface through an oxidation-reduction chemical reaction, without the application of an external electrical potential. Reducing agents, such as sodium hypophosphite or sodium formate, react at catalytic surfaces to release electrons, which immediately reduce the positively charged metal ions (e.g., nickel ions in ENIG and ENEPIG and palladium ions in ENEPIG), promoting their deposition onto the PWB.

This type of reaction is described as autocatalytic, as the deposition process will continue even after the substrate is completely covered by a continuous layer of the plated deposit. The deposit thickness will therefore continue to rise in the presence of source metal ions and a reducing agent, until the board is removed from the plating bath. The thickness of plated deposits will vary depending on the bath temperature, chemical parameters (such as solution pH) and the amount of time spent in the plating bath.

Immersion Process: This chemical process uses a chemical displacement reaction to deposit a layer of a second metal onto a base metal surface. In this reaction, the base metal dissolves,

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releasing the electrons that reduce the positively charged ions of the second metal present in solution. Driven by the electrochemical potential difference, the metal ions in solution (e.g., gold ions in ENIG or ENEPIG process) are deposited onto the surface of the board, simultaneously displacing ions of the surface metal into solution.

This type of reaction will continue as long as the base metal is available to supply electrons to the displacement reaction.

ENEPIG has the advantage over ENIG of being a gold wire bondable surface. ENIG is not an ideal gold wire bonding surface because over time the electroless nickel will diffuse through to the surface along the crystal boundaries of the immersion gold and the wire would not stick. ENEPIG's palladium layer is a diffusion barrier to the nickel, the gold remains unadulterated and is bondable with gold thickness as low as 1.2 µin or 0.03 microns.

A gold coating as thick as 0.1–0.2 microns or 4–8 µin would open the wire bonding operating window. Thicker gold is beyond the capability of standard immersion gold. If a thicker gold is specified, then modified immersion gold, such as reduction-assisted immersion gold, would be the preferred choice.

The electroless palladium requires a reducing agent. The most commonly used reducing agent is sodium hypophosphite, which produces a phos-palladium deposit with 4–5% phosphorous in the deposit. The presence of phosphorous renders the palladium deposit amorphous (non-crystalline), making it the ideal diffusion barrier. Other reducing agents may produce a non-phos palladium, which tends to be crystalline in structure.

The ENEPIG IPC-4556 Specification 2013

For ENEPIG thickness, IPC-4556 states:

Nickel: *3–6 µm [118.1–236.2 µin] at ± 4 sigma (standard deviations) from the mean.*

Palladium: *0.05–0.15 µm [2–12 µin] at ± 4 sigma (standard deviations) from the mean.*

Gold: *Minimum thickness of 0.025 µm [1.2 µin] at - 4 sigma (standard deviations) below the mean.*

All measurements to be taken on a nominal pad size of 1.5 mm x 1.5 mm [0.060 in x 0.060 in] or equivalent area.

An amendment that sets an upper limit for gold thickness for ENEPIG at 2.8 µin (0.7 µm) is presently in final draft for peer review. The amendment was necessary because too many designers were specifying a much higher immersion gold value. The higher thickness involved increased dwell time in the gold bath, resulting in nickel corrosion under the palladium layer.

"Soldermask application involves cleaning and roughening the copper surface, the application of a photoimageable mask, tack drying, imaging, developing and curing. Attention to the details of processing soldermask is paramount to achieving the desired ENEPIG deposit."

ENEPIG Fabrication

The copper surface coming to the ENEPIG line in most cases follows tin stripping and the application of soldermask. Residual tin left on the surface will interfere with catalyzation of the copper surface. Soldermask application involves cleaning and roughening the copper surface, the application of a photoimageable mask, tack drying, imaging, developing and curing. Attention to the details of processing soldermask is paramount to achieving the desired ENEPIG deposit. The proper adhesion between the mask and the copper surface has to be achieved. After development there should be no organic residues left on the pad surfaces, and the side wall should be straight with no signs of negative or positive foot. This is particularly important if the design includes soldermask defined pads.

Process Sequence

1. Cleaner: The purpose of this step is to clean the copper surface in preparation for pro-

cessing. The cleaner removes oxides and light surface contaminants, and ensures that the surface will be in a condition allowing it to be uniformly micro-etched. Vendor specifications for temperature, dwell time, agitation and bath chemical control should be followed.

2. Micro-etch: This step produces a surface that may be uniformly catalyzed and plated with good deposit adhesion by removing some copper from the surface. A variety of different etchant types may be used (e.g., sodium persulfate, peroxide/sulfuric). Vendor specifications for temperature, dwell time, agitation and bath chemical control should be followed.

3. Catalyst: The step deposits a material that is catalytic to electroless nickel plating on the copper surface. The catalyst lowers the activation energy for nickel deposition and allows plating to initiate on the copper surface. Examples of metal catalysts include palladium and ruthenium (deposited by an immersion reaction with the copper surface). Vendor specifications for temperature, dwell time, agitation and bath chemical control should be followed.

"The catalyst lowers the activation energy for nickel deposition and allows plating to initiate on the copper surface. Examples of metal catalysts include palladium and ruthenium (deposited by an immersion reaction with the copper surface)"

4. Electroless Nickel: The purpose of this bath is to deposit the required thickness of electroless nickel on the catalyzed copper surface. The nickel thickness should be adequate to cover the copper with a substantially pore-free coating, to create a diffusion barrier to copper migration, and also serve as a solderable surface, depending on the intended application.

The nickel bath has a relatively high deposition rate and its active chemical components must be maintained in balance on a continuous basis, by addition of appropriate replenishment components. Electroless nickel baths typically run at high temperatures and extended dwell times to achieve the required deposit thickness. It is therefore important to ensure that compatible PWB substrate and solder mask materials are used. Vendor specifications for temperature, dwell time, agitation and bath chemical control should be followed.

5. Electroless Palladium: This bath deposits the desired thickness of electroless palladium on the freshly deposited nickel surface. It is mainly composed of a source of palladium metal ion and a reducing agent. In addition, it has proprietary stabilizers, surfactants and chelating agents. The solution requires replenishment of all of its components to maintain its activity. Vendor specifications for temperature, bath life, dwell time, agitation and bath chemical control should be adhered to.

6. Immersion Gold: The purpose of this step is to deposit a thin, continuous layer of immersion gold.

$$Pd^0 \longrightarrow Pd^{++} + 2e$$
$$2Au^+ + 2e \longrightarrow 2Au^0$$
$$2Au^+ + Pd^0 \longrightarrow 2Au^0 + Pd^{++}$$

This is a displacement reaction. Note: As a result of their respective position in the electromotive series, the exchange rate of gold with the palladium substrate is not as efficient as gold with the nickel substrate.

The gold protects the underlying electroless palladium layer from reacting with the ambient environment and also serves as a contact surface, depending on the intended application. This bath runs at relatively high temperatures and dwell times. Vendor specifications for temperature, dwell time, agitation, bath life and bath chemical control should be followed.

2015 Programs

May 13–14
IPC Technical Education
Fort Worth, TX, USA
Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting
- SMT Problem Solving

June 9
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
Fort Lee, NJ, USA

June 9–10
IPC Technical Education
Chicago, IL, USA
Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting
- SMT Problem Solving

June 10
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
Des Plaines, IL, USA

June 12
ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
Milpitas, CA, USA (San Jose area)

September 27–October 1
IPC Fall Standards Development Committee Meetings
Rosemont, IL, USA
Co-located with SMTA International

September 28
IPC EMS Management Meeting
Rosemont, IL, USA

October 13
IPC Conference on Government Regulation
Essen, Germany
Discussion with international experts on regulatory issues

October 13–15
IPC Europe Forum: Innovation for Reliability
Essen, Germany
Practical applications for meeting reliability challenges like tin whiskers, with special focus on military-aerospace and automotive sectors

October 26–27
IPC Technical Education
Minneapolis, MN, USA
Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting
- SMT Problem Solving

October 28–29
IPC Flexible Circuits-HDI Conference
Minneapolis, MN, USA
Presentations will address Flex and HDI challenges in methodology, materials, and technology.

November 2–6
IPC EMS Program Management Training and Certification
Chicago, IL, USA

November 4
PCB Carolina 2015
Raleigh, NC, USA

December 2–3
IPC Technical Education
Raleigh, NC, USA
Professional development courses for engineering staff and managers:
- DFX-Design For Excellence (DFM, DFA, DFT and more)
- Best Practices in Fabrication
- Advanced Troubleshooting
- SMT Problem Solving

December 2–4
International Printed Circuit and APEX South China Fair (HKPCA & IPC Show)
Shenzhen, China

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7. Rinsing: These steps remove residual process chemicals from the PWB surface after each chemical processing step. This may be achieved in either a single step or with multiple rinses. In some instances, pre-dip and/or post-dip process steps may also be required for optimum process performance. Vendor specifications for temperature, dwell time, agitation and turn-over rate should be followed.

8. Drying: Ensure the boards are completely dry may be achieved by use of either in-line vertical, or off-line horizontal drying. Off-line horizontal drying should be preceded by a horizontal rinsing step and should be dedicated to the boards from the ENIG/ENEPIG processes. The time and temperature should be optimized to suit the type of product.

The ENEPIG line is the most complex chemical process in a board shop. It requires a good understanding of how the process works and the critical parameters that must be maintained. The ENEPIG line has little tolerance for deviations, particularly to extending the bath life of any of the process steps. Shops that have good engineering and documentation of the manufacturing process, coupled with a dedicated, experienced ENEPIG operator that is backed by a capable analytical laboratory, run defect-free ENEPIG day in and day out, to a consistent product that meets customer requirements. **PCB**

George Milad is the national accounts manager of technology at Uyemura International Corporation. To reach the author, click here.

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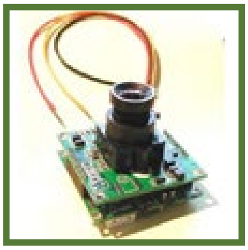

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PCB007 Supplier/New Product News Highlights

Atotech's Uwe Hauf's View of the Global Electronics Manufacturing Market

Uwe Hauf, VP of electronics for Atotech, and I-Connect007 Publisher Barry Matties sat down at CPCA 2015 for an illuminating discussion of the global market—what's happening now, what is going to happen tomorrow, and a few things that won't happen for at least 10 years, according to Hauf.

Isola Launches Low-loss Laminate for 100 GB Ethernet Apps

I-Connect007 Technical Editor Pete Starkey and Isola's Fred Hickman, senior director of high-speed digital products, spent time at IPC APEX EXPO 2015 talking about Isola's recent launch of a low-loss, low-skew laminate prepreg. Hickman explains that the new material, Chronon, will be one of the enablers of 100GB Ethernet applications.

Hitachi Chemical America Hosted HDP's Member Meeting

Hitachi Chemical America hosted HDP User Group International Inc.'s first 2015 member meeting at its Plumwood House Research Center, located on the campus of the University of California, Irvine.

Benefits of Soldering with Vacuum Profiles

Requirements for void-free solder joints are continuously increasing in the field of electronics manufacturing, bringing new challenges that are evolving on a daily basis due to the relentless introduction of new variants of so-called bottom-terminated components (BTCs). Connector geometries alone are not decisive—numerous pitfalls are of greater significance.

Candor Industries Becomes Approved Vendor for Microsoft

Candor Industries, an advanced technology circuit board fabricator based in Toronto, Ontario announces their acceptance to the Microsoft Preferred Supplier Program.

Mass Design Acquires Electropac

"Like Mass Design, Electropac has served commercial, medical, military and aerospace industries with custom design and manufacturing as well as large-volume production. The company's key people, expertise, product mix and markets mesh perfectly with our corporate environment," said Tony Bourassa, president of Mass Design, in making the announcement.

Amitron Earns UL Certification for Aismalibar IMS Materials

Amitron Corporation has received their UL listing for Aismalibar's full range of insulated metal substrate materials. The certification allows Amitron to UL stamp their products using the entire line of Aismalibar materials which includes ALCUP-G 1.3w, ALCUP 1.8w, HTC 2.2w, HTC 3.2w, HTC Ultrathin and Flextherm.

Royal Circuits Acquires Second Maskless LDI Machine

Milan Shah, president and owner of Royal Circuits Solutions announced that his company has recently acquired their second Maskless Lithography direct imaging machine. Royal is one of the first PCB fabricators to own two of these units.

Material Witness: Low-Flow Prepregs—Taming the Beast!

In this installment of Material Witness, Chet Guiles continues his discussion around low-flow prepregs, with good advice about how to actually use these materials.

atg Luther & Maelzer Launches Flying Probe Tester for Substrates

atg Luther & Maelzer has delivered the first flying probe system for substrate test to a major customer in Korea. The S3 10 μm substrate tester is the first system of a new atg Luther & Maelzer product line.

The Importance of Harmonized Standards that Benefit All

I-Connect007 Technical Editor Pete Starkey caught up with Amphenol's Applications Engineer, Sean Keating, at IPC APEX EXPO in San Diego. Keating explains his company's commitment to proactive participation in the establishment of standards, his personal experience working on standards committees, and his view on the importance of harmonised global standards.

Pete Starkey: It's nice to see you here at IPC APEX. I understand Amphenol is strongly interested in standards and that you are personally active on some committees. Start by telling us about that.

Sean Keating: Amphenol UK is very proactive in a number of the standards, in particular the certification standards. I have been working closely with IPC for about six or seven years now. My secondary reason for being here is that this is a fantastic forum for problem solving. Any problems that have cropped up over the weeks or months prior to the show can often be resolved using the immense technological think tank that's here on the show floor, in the meetings, or even in the bar!

I'm on nine committees right now, from low pressure overmoulding to electronics in space, and I would say we're probably working 10+ hours a day. It's a busy week for a number of the standards; much of my focus is on the IPC/WHMAA-620 cable and harness training committee, which is meeting on Thursday to discuss training. We are looking at having a more robust practical course that will be certifiable. This will mean that when you certify to that standard you have demonstrated the skills and proven ability to actually build a harness—not just inspect it. Perhaps, depending on how the committee decides, there will be different levels of harness ability or skill, but we will have to wait and see on that one!

Starkey: IPC and IEC are really recognized as the world's standards authorities, but do you notice that some of the standards are originating from Asia and taking some prominence?

Keating: Certainly not with anything we're doing in Europe, but I cannot answer for the whole group as we have facilities in more than 40 countries, worldwide. IPC, without doubt, has the lion's share of standards, which are imposed on us by our major customers. As a design and manufacturing facility we get standards imposed on us as well as what we pass onto our subcontractors. Virtually all of our major customers now have IPC standards of one type or another noted on their drawings. I've been with Amphenol for 26 years and for the last 10–12 years this has grown from occasionally seeing an IPC standard called out to the point now where nearly every single callout references an IPC standard.

Starkey: Provided that there is some international cooperation and our colleagues in Asia are prepared to recognize Western standards and cooperate with them, there is worldwide harmony.

Keating: Absolutely, and with Amphenol being a global company, we actually help train and facilitate at our India and China locations, so that within Amphenol worldwide, we're working to the same standard. And that harmony is absolutely imperative. It also means that when we talk to them, when we look at them as low cost manufacturers, we can talk at exactly the same level and about the same things. So it really has been helpful.

Starkey: Sean, thanks very much for your time.

Keating: Thank you, Pete. **PCB**

Interested in participating in an interview for *The PCB Magazine?* Click here for more information!

Best Practices 101: Part 7

by Steve Williams
STEVE WILLIAMS CONSULTING LLC

Management by Walking Around

Tom Peters, author of the "Excellence" series of books and one of my favorite management visionaries, coined the phrase MBWA (Management by Walking Around). This is another concept that seems so obvious, but how many of us actually do this? This is a rhetorical question, of course, but really, how often do we go out on the shop floor and just observe what is going on? I don't mean tracking down orders and making sure people are working, but more along the lines of, how does the facility look? Do the workers look happy? Are we working smart or overcompensating by working hard? What would I think if I were the customer? You can't answer these questions sitting in your office!

Gemba

Peters was on to something with his MBWA; in fact, the Japanese have a similar term for this, and that is "gemba." Roughly translated as "the real place," gemba means getting off your butt and going to see where the work is actually being done. Like many Lean buzzwords such as kaizen, gemba has transitioned from obscure to ubiquitous across our industry. I love gemba, but like anything worthwhile, you get out of it what you put into it. Gemba demands a few things from the user to be successful.

First, it requires a deep curiosity to know what is really going on in your organization. Not what you think is going on, or what you heard is going on, but what is actually going on. Next, gemba demands a skill set that includes the ability to actively observe and understand the work that's being done. While this may seem obvious, doing a drive-by surface observation won't accomplish anything, and may actually do some damage by providing a false sense of process well-being. The last demand is per-

haps the most important: an inherent respect for the people actually doing the work. These are your process experts that have the practical experience and tribal knowledge of the process. Gemba walks need to be approached from a place of mutual respect and overriding desire to make things better, faster, cheaper, easier, etc. Gemba means going to where the work is being done and engaging the people directly, not assuming you have solved all the problems from your office.

The Gemba Walk

The gemba walk provides company leaders, managers and supervisors a simple, easy means of supporting overall continuous improvement while directly engaging with the folks responsible for the key business processes. The best approach to a gemba walk is to start at the last process and work upstream. Why? This will highlight how well your process is operating from a high level in terms of pull vs. push, bottlenecks, inventory and other production control issues. Depending on the level of personnel participating and/or circumstances, gemba walks can be daily, weekly or monthly. Another suggestion is to focus on a different aspect (theme) for each gemba walk. For example, one day might focus on 5S in the facility; another may be on WIP inventory, etc. It is important to limit the focus because if you look for everything, you will accomplish nothing!

Instituting regular gemba walks into the culture will consistently demonstrate to employees a leadership commitment, alignment and support of the continuous improvement process. There are a couple of keys to a successful gemba walk, such as active and attentive listening, sharing what you learned during the gemba walk with the entire organization, discussing with department leaders conditions observed, and following up/monitoring the process where necessary.

What the Gemba Walk is Not

A gemba walk is not an opportunity to point fingers and find fault in employees while they are being observed. It is not punitive; employees will shut down and not openly engage at the first whiff of this. It is not a time to be the policy police; internal audits or other tools are appropriate for this. Finally, a gemba walk is not the time to solve; it is a time of observation, input and reflection. That does not mean disregarding operator ideas for improvements, but rather to physically go and see what is really happening. Any ideas or complaints should be noted and followed-up with after the walk. Be mindful not

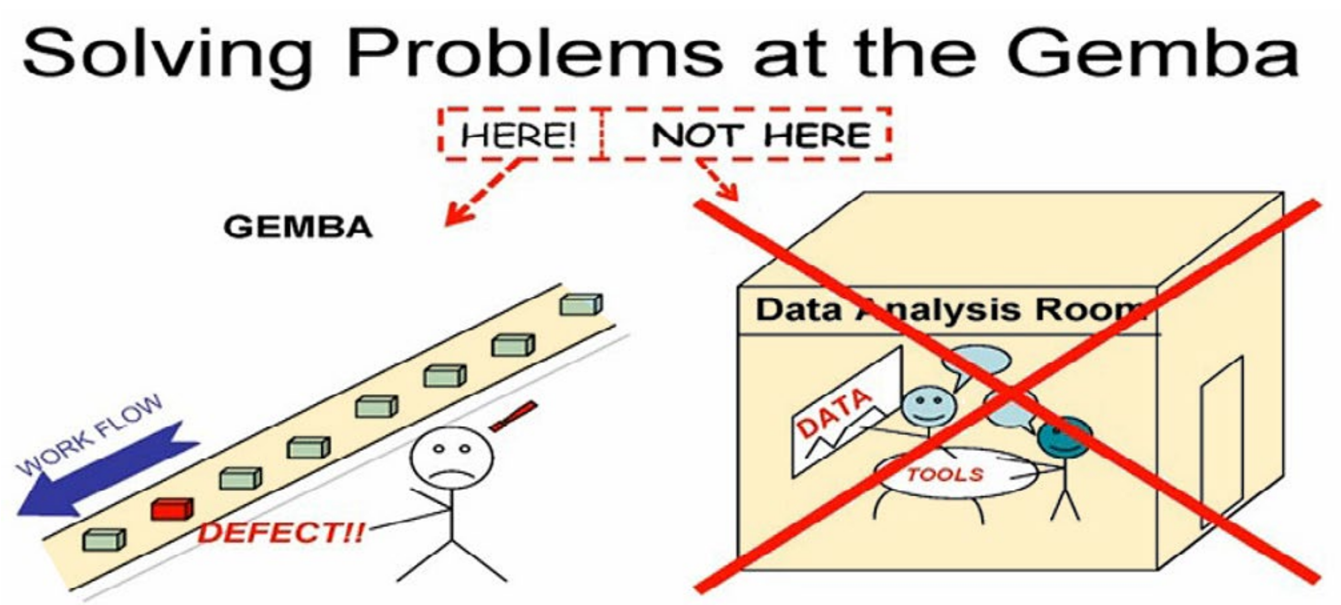

Figure 1.

to “miss the forest because of the trees,” as the saying goes.

Visual Management

I am a big fan of meaningful visual management everywhere possible to keep employees engaged, informed and foster a culture of ownership. Noticed my emphasis of the word “meaningful” when talking about visual management; what I mean by this is avoiding at all costs a wallpaper strategy of posting gratuitous charts, graphs, reports, etc., on walls to impress customers. The gemba walk provides a great opportunity to notice and question posted measures and charts and ask the following questions:

- What is this chart telling me?
- Who is responsible for updating them?
- Do the employees look at the charts? How often?
- What value do the charts have for employees?
- Do customers and/or suppliers ever look at the charts?
- Do the charts have an overall effect on operations?

The key to any process improvement is to question everything; do not just accept the status quo. Whether you manage by walking around, engage in gemba walks, or utilize some other method of going to where the work is done, the key is to get out of your office and go and see. **PCB**

Steve Williams is the president of Steve Williams Consulting LLC and the former strategic sourcing manager for Plexus Corp. He is the author of the books, Quality 101 Handbook and Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean. To read past columns, or to contact Williams, click here.

VIDEO INTERVIEW

Five Keys for Success in PCB Manufacturing

by Real Time with... IPC APEX EXPO 2015

All Flex VP of Sales and Marketing, Dave Becker, tells Kelly Dack, “It’s not about the technology.” He discusses the five core values that are part of the culture at All Flex, and as a final point, Becker explains how “culture beats strategy.”

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Mil/Aero007
News Highlights

Zentech's John Vaughan on the Mil/Aero Sector: "It's Headed Up"

I-Connect007 Publisher Barry Matties and Zentech's John Vaughan had a chance to discuss industry concerns within the mil/aero segment at IPC APEX EXPO 2015. The two also shared thoughts on the space industry, and Vaughan detailed Zentech's involvement with National Manufacturing Day, a nationwide effort focused on STEM (Science, Technology, Engineering and Math).

PNC Announces Latest Add-on Qualification to MIL-PRF-31032

PNC is proud to announce the latest add-on qualification of product testing to Military Performance Specification MIL-PRF-31032, CAGE Code 66766. The newest capabilities stem from PNC's continuous improvement of capital equipment.

Exception PCB Earns AS9100 Certification

Exception PCB Solutions Ltd, one of Europe's leading PCB producers, recently secured their AS9100 approval following a recent assessment by BSI (March 2015). AS9100 is the internationally recognised quality management system specialised to the aerospace industry.

FTG Circuits Earns DoD Certification for Flex PCB

Firan Technology Group Corporation announced that its Circuits—Toronto facility has added flexible and rigid-flex printed circuit boards to its qualification under Military Specification MIL-PRF-31032. This certification is in addition to the multiple existing certifications for a wide range of technologies already held by the facility.

Key PCB Makers Strategize to Meet Industry Demands

The computer/peripheral application is expected to witness the highest growth followed by the communication applications. Nippon Mektron, Zhen Ding Technology Holding Limited, Young Poong Electronics Co. Ltd., Unimicron Technology Corp., and Samsung Electro-Mechanics are among the major suppliers of PCBs. The industry players are going for partnership and strategic alliances to deliver unique solutions and to meet the constantly changing industry demands of customers.

Battelle Unveils Breakthrough Anti-Counterfeiting Detection for ICs

"As counterfeiting continues to be a growing issue for both suppliers and manufacturers, ensuring that all components are effectively and accurately verified for authenticity has become an increasingly time consuming and expensive task," said Larry J. House, Cyber Technical Director, of Battelle.

DARPA Programs Simultaneously Test Limits of Technology

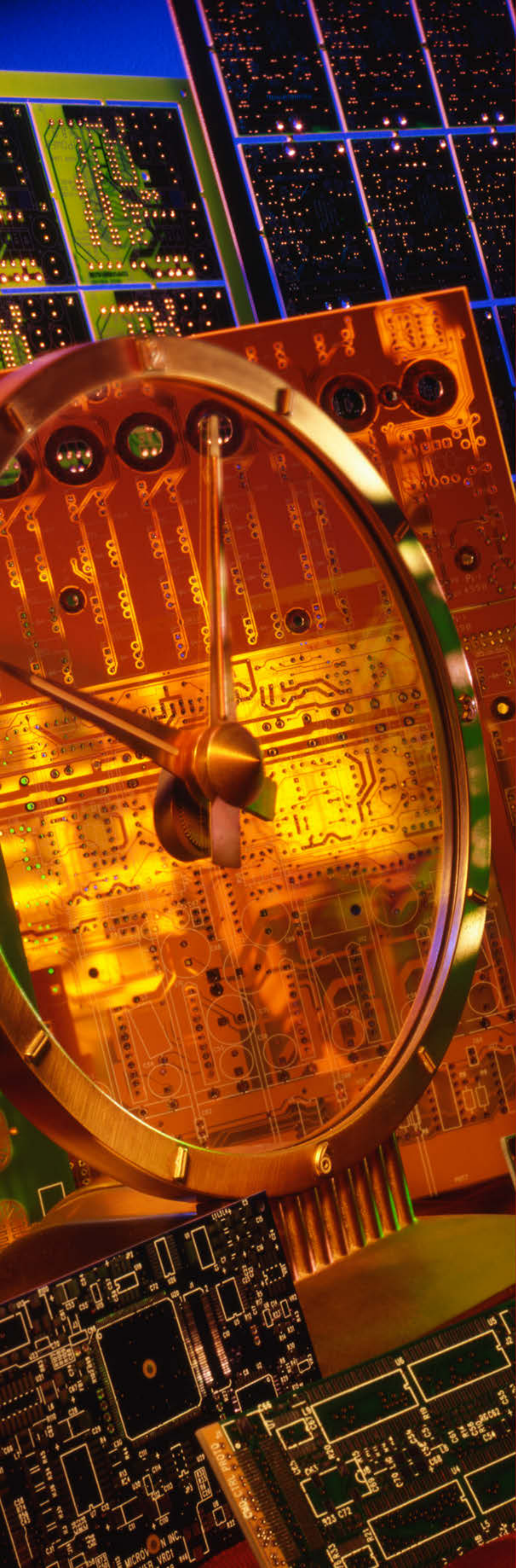
Less than one week after releasing Breakthrough Technologies for National Security, DARPA's latest summary of the agency's mission, accomplishments and funding priorities for extending its legacy of technological disruption, the agency today announced four major new programs—evidence of DARPA's commitment to pursuing high-risk/high-reward research and making the impossible possible.

DARPA Shares Vision for the Future

New biennial report describes the agency's mission in the context of today's fast-changing world, and current and upcoming areas of focused investment

Boeing Boosts Imaging, Intelligence Services; Acquires 2d3 Sensing

Boeing has acquired 2d3 Sensing, a wholly owned subsidiary of OMG plc specializing in motion imagery processing of critical intelligence, surveillance and reconnaissance data generated from aerial platforms.



Quick-Turn Circuit Board Shops

by Karl Dietz
KARL DIETZ CONSULTING LLC

Quick-turn circuit board shops specialize in the speedy delivery of small lots or prototype boards. Thus, they value any processing technique and technologies that reduce the time of the critical path between receiving the CAD data and shipping the finished boards. Some of the technologies that enable fast delivery are also suitable for mass production. The following are some examples of quick-turn processing.

Phototooling

The creation of a silver halide phototool involves a number of time-consuming steps such as plotting, development, fixing, drying, and equilibrating the phototool to the temperature and humidity of the working environment. Equilibration is particularly time-consuming (Figure 1).

Some quick-turn shops have tried to shortcut the equilibration step with limited success.

	50% Equilibration	75-80% Equilibrium*	95% Equilibration
■ 4-mil products	12-15 minutes	1-2 hours	2-4 hours
■ 7-mil products	1-2 hours	3-4 hours	6-8 hours

Figure 1: Humidity pre-conditioning times.

The target dimensions of the phototool features are those of a damp phototool. Typically, the dryer temperature of the processor is set lower than normal so that the film exits the processor just a little damp and relatively cool[1]. The film is measured within minutes after processing and sent directly to the imaging area. A film processed and used this way will slowly change size over the next several hours while it is in use, but when used quickly after processing and measuring, and if the tolerances are fairly forgiving, this approach can be viable in reducing overall processing time.

Digital Imaging

Laser direct imaging, or other digital imaging processes, has been first adopted by prototype and quick-turn shops for the obvious reason that they eliminate all phototool processing steps. The other big advantage of LDI is its ability to scale the image (i.e., change the dimensions slightly, for best fit to image features

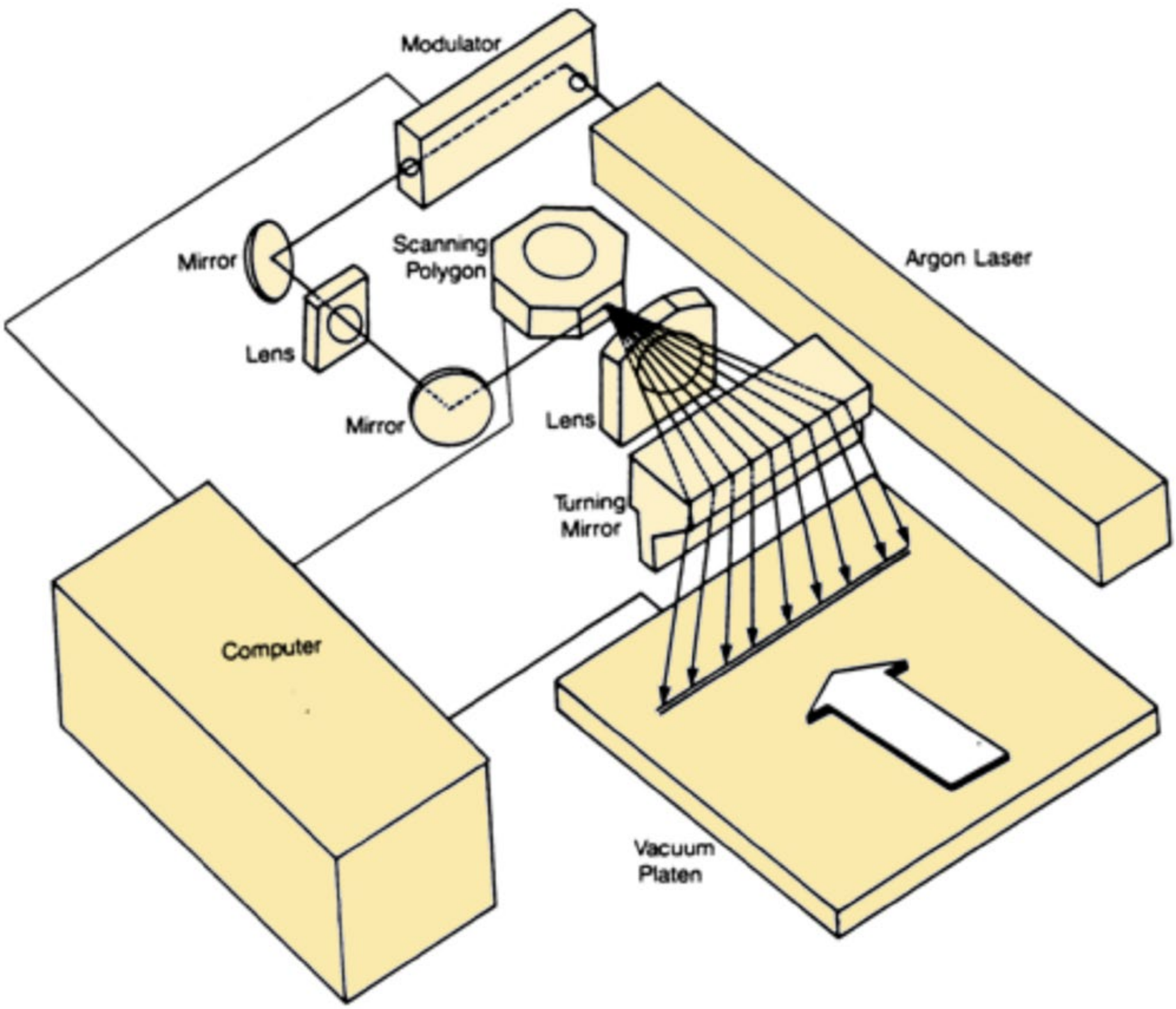


Figure 2: Schematic of a laser imaging tool.

on another layer). Figure 2 shows the elements of a typical laser imaging tool.

Direct Metallization Processes

Direct metallization processes allow copper plating in through-holes without having to go the lengthy electroless copper process. Direct metallization process uses either carbon, graphite, or palladium catalyst, or a conductive polymer to initiate copper electroplating on the dielectric hole wall. These processes avoid the use of problematic chemicals that are part of the electroless copper formulation; they use less water, typically have a smaller equipment footprint, and use fewer processing steps, which allow the quick-turn shop to reduce processing time. Table 1 compares a graphite-based direct metallization process with the sequence of steps that make up the electroless copper process.

Multilayer Bonder

A multilayer bonder treatment (oxide or oxide alternative) is typically applied after innerlayer print and etch. Some quick-turn shops have had success with a process flow whereby the multilayer bonder is applied to the innerlayer copper surface before resist lamination, exposure and development. In this process, the resist adheres to the multilayer coating, not to the copper. Dry film compatibility with this process sequence needs to be checked in terms of resist adhesion to such a surface, which is normally very good, and clean resist stripping needs to be established. This processing sequence takes the bonder treatment out of the critical time path for the board manufacture since the multilayer treatment can be done off line, in advance of the board manufacture. The bonder can also be beneficial as an anti-halation layer that prevents unwanted reflection of UV light from the board surface into non-exposure areas.

Legend Print

Legend print is traditionally done by screen printing, which involves the time-consuming screen preparation. In recent years, legend print-

Direct Metallization Process[3]	Electroless Copper Plating Sequence[2]
1. Cleaner/conditioner	7. Rack boards
2. Rinse	8. Cleaner/conditioner
3. Apply conductive colloid (graphite)	9. Rinse
4. Dry	10. Microetch
5. Microetch (to lift graphite off copper)	11. Rinse
6. Dry	12. Sulfuric acid (optional)
	13. Rinse
	14. Pre-activator
	15. Activator (catalyst)
	16. Rinse
	17. Post-activator (accelerator)
	18. Rinse
	19. Electroless copper
	20. Rinse
	21. Sulfuric acid or anti-tarnish (optional)
	22. Rinse
	23. Scrub (optional)
	24. Rinse
	25. Copper flash plate (optional)
	26. Dry

Table 1: Comparison of direct metallization process sequence with electroless copper plating.

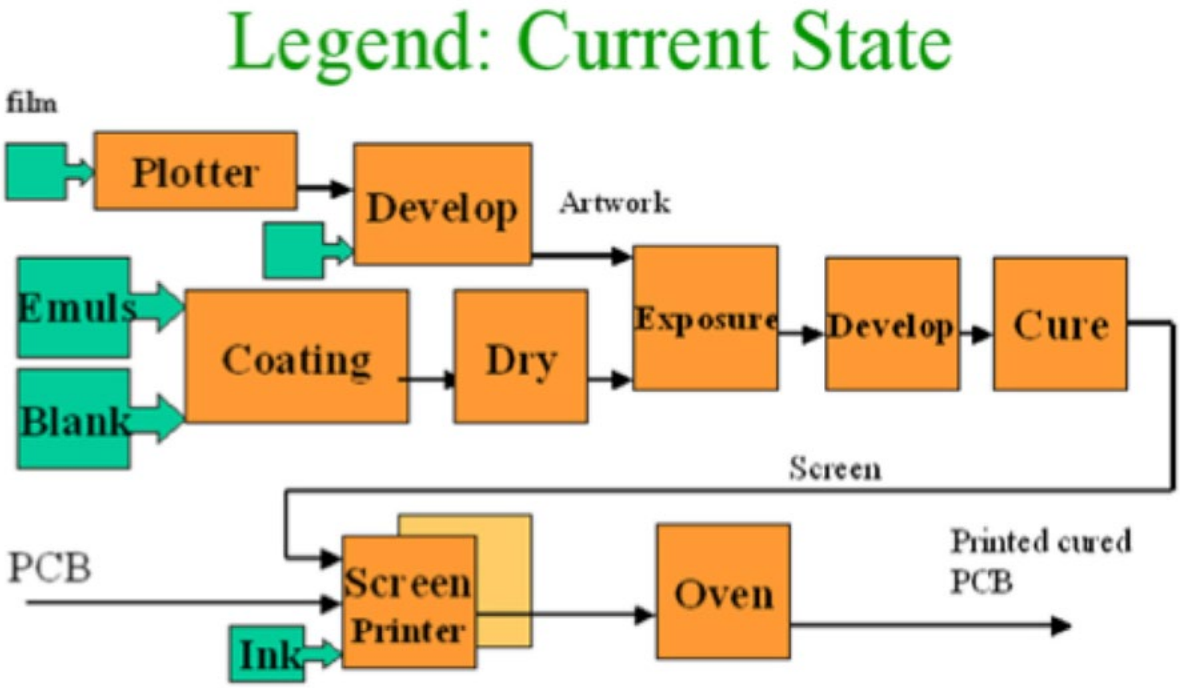


Figure 3: Screen printing of legend ink. (source: Printar)

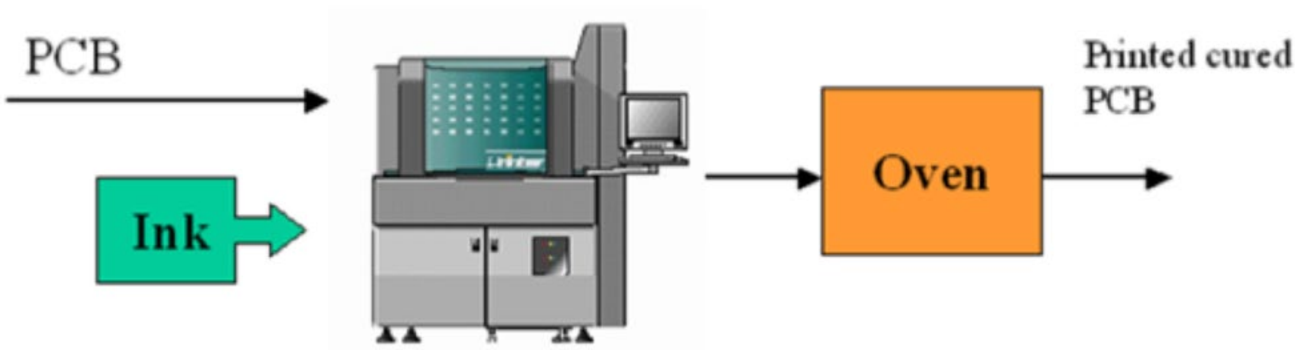


Figure 4: Ink-jetting of legend ink. (source: Printar)

ing by ink-jetting has become quite popular. Figure 3 shows the screen printing process while Figure 4 illustrates the simplicity of ink-jetting. **PCB**

References

1. Private communication, Robert Seyfert.
2. Printed Circuit Handbook, 6th Edition, Clyde F. Coombs, Jr.
3. "Shadow" process by OMGI (formerly Electrochemicals).

Karl Dietz is president of Karl Dietz Consulting LLC. He offers consulting services and tutorials in the field of circuit board & substrate fabrication technology. To view past columns or to reach Dietz, click here. Dietz may also be reached by phone at (001) 919-870-6230.

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Recent Highlights from PCB007

1 Multek CTO Excited about the Challenges of the Fast-Moving Wearables Market

I-Connect007 Publisher Barry Matties and recently-appointed Multek CTO Dr. Joan Vrtis sat down at IPC APEX EXPO to discuss the rapidly evolving wearables market, especially for medical, and the myriad questions that must be addressed. Other topics include Multek's contribution to the wearables industry and what it sees as the main challenges to putting their circuits into various applications.

2 Raising a Unified Voice for an Advanced Manufacturing Economy

The electronics manufacturing industry is an important sector in the global economy, and John Hasselmann, VP of Government Relations at IPC, is an advocate for policies that will help our industry as well as the prosperity and welfare of billions of people.

3 Reliability and Harmonization of Global Standards at Forefront of EIPC Efforts

At IPC APEX EXPO 2015, I-Connect007 Technical Editor Pete Starkey caught up with EIPC's Michael Weinhold and Alun Morgan, who were happy to discuss both recent and ongoing focuses for EIPC. Also touched on was the importance of the alignment of global standardization processes, especially for Asia.

4 Are There Advantages to Changing Your Registration System?

I-Connect007 Publisher Barry Matties recently had a conversation with DIS's Tony Faraci at IPC APEX EXPO 2015, to learn more about their pinless registration system. What was most interesting to Matties was the potential advantages a pinless system offers and why the process has not been widely adopted.

5 Schmoll Keeping an Eye on the Future—and on LDI

In this interview, Thomas Kunz, who has been at the helm of Schmoll Maschinen as president since 1993, discusses the company's lengthy history in mechanical engineering (more than 70 years), current global scope, and what he sees as a steady progression in directions that make the most sense to customers, which includes laser direct imaging.

6 Bernie Kessler: Pioneering Spirit Then and Now

I-Connect007's Patty Goldman sat down with long time friend and IPC Hall of Famer Bernie Kessler at IPC APEX EXPO 2015 in San Diego. Among other things, the two discussed the early days of IPC and the origins of APEX EXPO.

7 Manz: A Total Process Solution

At the recent CPCA Show in China, I-Connect007 Publisher Barry Matties had a chance to speak with Alex Liu, the deputy general manager of the PCB business unit for Manz. Manz has focused on creating a process from direct imaging to wet processing. With more entrants into the direct imaging arena, Liu feels that this approach gives Manz and their customers an advantage.

8 ESI's New Gemstone Changing the Rules for Laser

I-Connect007 Publisher Barry Matties sat down at CPCA 2015 with ESI's Mike Jennings, who explained the company's newest addition: Gemstone, an ESI-designed and manufactured laser system with 10,000 guaranteed hours, which is poised to change the rules in flex and other printed circuit processing.

9 Key PCB Makers Strategize to Meet Industry Demands

The computer/peripheral application is expected to witness the highest growth followed by the communication applications. Nippon Mektron, Zhen Ding Technology Holding Limited, Young Poong Electronics Co. Ltd., Unimicron Technology Corp., and Samsung Electro-Mechanics are among the major suppliers of PCBs.

10 N.A. PCB Book-to-Bill Ratio Strengthens

"Although North American PCB sales continued slightly below last year's levels in February, bookings strengthened," said Sharon Starr, IPC's director of market research. "This increased the book-to-bill ratio…it has been in positive territory for the past five months, which is a positive indicator for sales growth in the first half of 2015."

EVENTS

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar of Events, click here.

For the complete PCB007 Calendar of Events, click here.

Puget Sound Expo & Tech Forum
May 7, 2015
Bellevue, Washington, USA

Wisconsin Expo & Tech Forum
May 12, 2015
Milwaukee, Wisconsin, USA

IPC Technical Education
May 13–14, 2015
Fort Worth, Texas, USA

International Conference on Soldering & Reliability 2015
May 19–21, 2015
Markham, Ontario, Canada

Toronto SMTA Expo & Tech Forum
May 21, 2015
Markham, Ontario, Canada

Huntsville Expo & Tech Forum
June 4, 2015
Huntsville, Alabama, USA

ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
June 9, 2015
Fort Lee, New Jersey, USA

ITI & IPC Conference on Emerging & Critical Environmental Product Requirements
June 12, 2015
Milpitas, California, USA

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Flexibles, Stretchables and Wearables

July:
Supply Chain Management

August:
The War on Process Failure