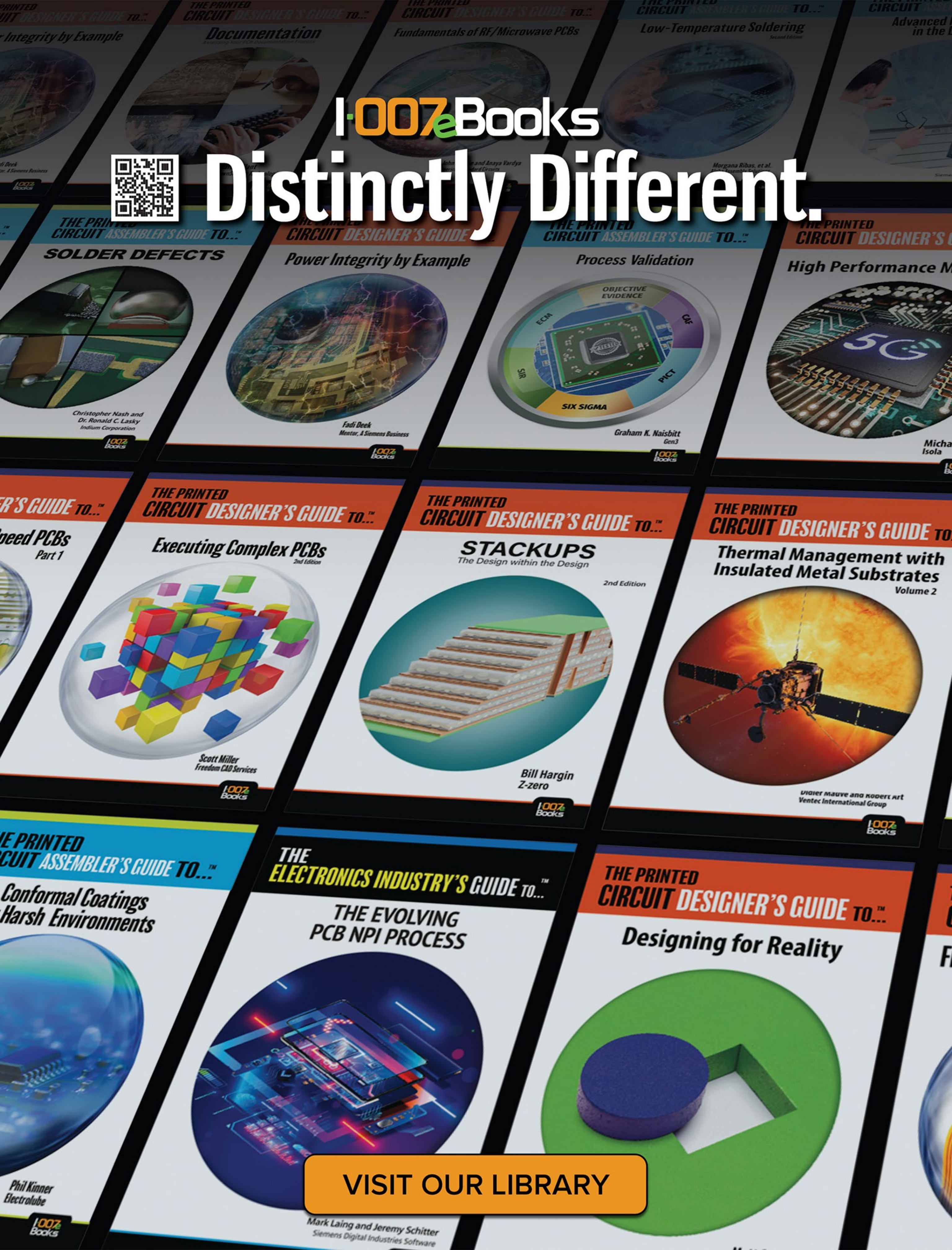
I-Connect007 GOOD FOR THE INDUSTRY

JANUARY 2023

PCB007 MAGAZINE



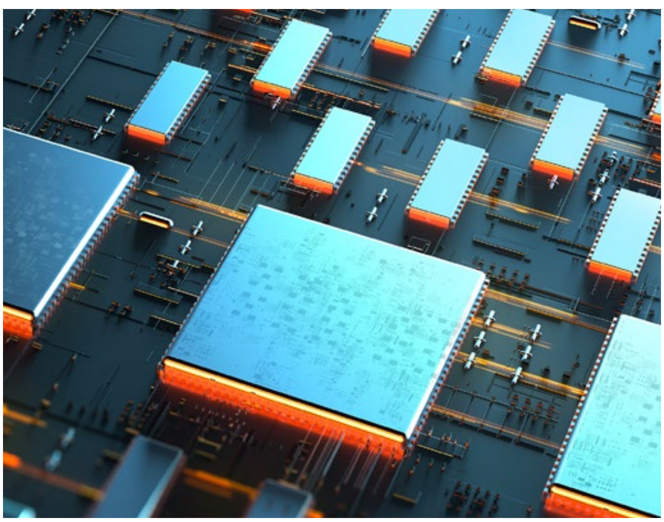
I-007eBooks
Distinctly Different.
THE PRINTED CIRCUIT DESIGNER'S GUIDE TO...™
Documentation
THE PRINTED CIRCUIT DESIGNER'S GUIDE TO...™
Fundamentals of RF/Microwave PCBs
THE PRINTED CIRCUIT ASSEMBLER'S GUIDE TO...™
Low-Temperature Soldering
THE PRINTED CIRCUIT ASSEMBLER'S GUIDE TO...™
SOLDER DEFECTS
Christopher Nash and Dr. Ronald C. Lasky
Indium Corporation
THE PRINTED CIRCUIT DESIGNER'S GUIDE TO...™
Power Integrity by Example
Fadi Deek
Mentor, A Siemens Business
THE PRINTED CIRCUIT ASSEMBLER'S GUIDE TO...™
Process Validation
Graham K. Naisbitt
Gen3
THE PRINTED CIRCUIT DESIGNER'S GUIDE TO...™
High Performance M
THE PRINTED CIRCUIT DESIGNER'S GUIDE TO...™
Executing Complex PCBs
2nd Edition
Scott Miller
Freedom CAD Services
THE PRINTED CIRCUIT DESIGNER'S GUIDE TO...™
STACKUPS
The Design within the Design
2nd Edition
Bill Hargin
Z-zero
THE PRINTED CIRCUIT DESIGNER'S GUIDE TO...™
Thermal Management with Insulated Metal Substrates
Volume 2
Ventec International Group
THE PRINTED CIRCUIT ASSEMBLER'S GUIDE TO...™
Conformal Coatings
Harsh Environments
Phil Kinner
Electrolube
THE ELECTRONICS INDUSTRY'S GUIDE TO...™
THE EVOLVING PCB NPI PROCESS
Mark Laing and Jeremy Schitter
Siemens Digital Industries Software
THE PRINTED CIRCUIT DESIGNER'S GUIDE TO...™
Designing for Reality
VISIT OUR LIBRARY

PCB007 MAGAZINE

The Advanced Move

As semiconductor companies seek ways to prolong Moore's Law, new advanced component packaging techniques and in-package substrates are blurring the boundaries between printed circuit and semiconductor fabrication. Are there strategic opportunities—new directions in which to shift your business—in this new space? In this issue, we open the discussion about how advanced packaging will change the structure of our industry.

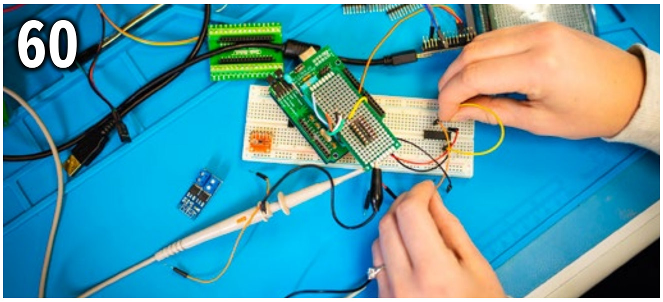
FEATURE ARTICLES



FEATURE INTERVIEWS

FEATURE COLUMNS

PCB007 MAGAZINE



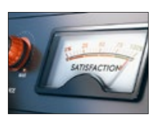
SHORTS

DEPARTMENTS

HIGHLIGHTS

COLUMNS

REAL TIME WITH... SPECIAL SECTION

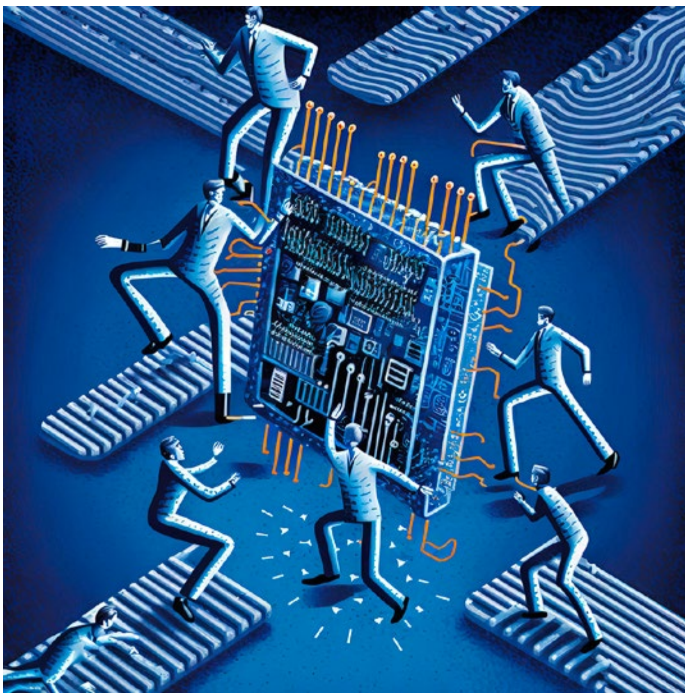


An Evolution

Nolan's Notes

by Nolan Johnson, I-CONNECT007

This month, *PCB007 Magazine* looks at the evolution of advanced packaging from the fabricator's perspective. This is, as you're aware, a global topic. Asia harbors nearly all the manufacturing capabilities for the packaging and interposer substrates required for the latest packaging technologies. North America and Europe, buoyed by their respective chip technologies legislation, are working to bring packaging capability back to their home shores. How this plays out remains to be seen.



This is such an important topic that our January issue of *SMT007 Magazine* focused on it from an assembler's perspective. In my column for that issue, I cited mainstream media coverage of President Biden's mid-December visit to the Arizona TSMC semiconductor foundry. In further research, I gained a new perspective from Chinese and Taiwanese voices covering the same visit.

An online piece published by Fortune.com, for example, reported, "TSMC is now building plants in Arizona and Japan amid growing concerns from customers and major governments that the world's chip production is too centralized in Taiwan."[1] The pressure for this move off the island is attributed primarily to TSMC's customers. It's a true statement. Perhaps not the only true statement, but true, nonetheless.

Now, there are some situations wherein a globally centralized production chain makes sense. In physics class, that would be a lesson starting with, "In a frictionless environment," and in economics, I suppose the corollary would be, "In an economy without political borders." For example, the southern portion of the African continent is heavy with diamond deposits, so it makes sense to refine a rare mineral close to that mineral deposit—cut and create finished diamonds close the source. That's efficient.

Yet that isn't how it's done. The world's finest diamond cutters don't live near the mines. The skilled staff who know how to turn the raw material into a high value finished product may not be willing to work next to the raw material's source. They may prefer to be closer to one of several commercial centers, which eases the sale and delivery of the finished product. The production experts move closer to the customer, not to the raw material.

At the moment, it's true that semiconductor companies are going where the customers are. *Fortune* reports, "TSMC is constructing new fabs to satisfy its customers' demand rather than fulfill requests from foreign governments." Behind the thinly veiled defiant attitude is a concession that getting close to the customer is a very high priority.

Nikkei Asia reports that, in the preceding three decades, "TSMC focused on building up cutting-edge chip production capacity in its home market, a strategy that helped the company keep costs down while continually honing its technological know-how."[2] That centralized model worked through economies of scale to deliver goods. But unpackaged semiconductor die are like diamonds in the rough. They're not yet in the form needed to deliver their greatest value.

I found one of the most impactful comments in the *Fortune* article was this: "It's not easy to replicate Taiwan's chip industry in another country as TSMC's success was built over more than 30 years with help from its suppliers." This perspective aligns with the U.S. CHIPS Act and HR 7677 proponents: rebuilding that expertise in this region will be the tricky part.

TSMC offers a case study in how difficult it can be to launch production without sufficient expertise. *Nikkei Asia,* referring to TSMC's first plant in Camas, Washington, reports, "'It was, I thought, a dream fulfilled,' Chang said. 'But it [the first plant] ran into cost problems. We ran into people problems, we ran into cultural problems. The dream fulfilled became a nightmare fulfilled. It took us several years to untangle ourselves from my nightmare, and I decided that I needed to postpone the dream.'"

However, geopolitical factors are at play here as well. China is in the middle of what appears to be a pressure campaign to reclaim Taiwan as Chinese territory. For the U.S- and European-backed semiconductor companies in Taiwan, this is a risk to their very existence. It seems like a solid survival tactic to start "mining" semiconductors in more stable environments.

Korea is speaking up on the topic. In an online piece published by *Fortune* (again), a senior Samsung official, Yang Hyang-ja, said: "We're in a chip war. Technology supremacy is a way that our country can take the lead in any security-related agenda, such as diplomatic and defense issues, without being swayed by other nations."[3]

Even *inside Asia,* efforts are being made to maintain strategic advantage in semiconductor manufacturing.

But to successfully diversify production of semiconductors, printed circuit manufacturing must tuck in right behind. Semiconductors, packaging, board fabrication and assembly services are all equally important to the delivery of a diversified supply chain—independent of any political situations. That is the reasoning behind this issue devoted to the topic of advanced packaging and substrates.

As we publish this issue, IPC APEX EXPO 2023 is just around the corner. We hope to see you there! **PCB007**

References

1. "TSMC CEO warns of weakening trust among countries after U.S. blacklists Chinese companies in computer chips tussle," by Debby Wu and Bloomberg, Fortune.com, Dec. 17, 2022.
2. "TSMC founder Morris Chang says globalization 'almost dead,'" by Cheng Ting-Fang, *Nikkei Asia,* Dec. 7, 2022.
3. "'We're in a chip war' Korea's lead on semiconductors is worried about the country losing chip manufacturing to the U.S.," by Sohee Kim and Bloomberg, Fortune.com, Jan. 3, 2023.

Nolan Johnson is managing editor of *PCB007 Magazine.* Nolan brings 30 years of career experience focused almost entirely on electronics design and manufacturing. To read other columns or to contact Johnson, click here.


Photo credit: John Harrington

Substrate Manufacturing: What Does it Take?

Feature Interview by Nolan Johnson
I-CONNECT007

Jan Vardaman is president at TechSearch International and was a keynote speaker at the IPC Advanced Packaging Symposium in October, where she laid out the problems and challenges ahead for new technology. To follow up, Nolan Johnson asks Jan to speak about implementation details to bring substrate manufacturing to regions outside Asia.

Nolan Johnson: Jan, would you provide a short overview of the IPC report on advanced packaging?

Jan Vardaman: The IPC report outlines why you need to have an ecosystem in the U.S. to support the next level in packaging. What you do after you fabricate it on a semiconductor chip doesn't do much good. To have a semiconductor chip and send it back over to Asia for assembly doesn't shorten your supply chain.

Johnson: That's why this is so strategically important for the U.S.?

Vardaman: You could certainly use your existing supply chain, but it doesn't address the problem of making the supply chain shorter. Cycle time concerns were the whole reason this got started. Historically, we like to use our existing supply chains. Currently, most seem to be planning just to fab the silicon here and ship it back to Asia for assembly.

Johnson: At least until such time as there's an alternative?


Jan Vardaman

Vardaman: An alternative that a set of customers agree to. In other words, you must have customers that line up and agree to use whatever you will put in place.

Johnson: What are some of the technical considerations?

Vardaman: Based on the demand, we talk about finer and finer bump pitch. If you look at a printed circuit board, it's large dimension with respect to line and space. Printed circuit boards often are measured in mils (1/1,000 of an inch). A mil is 25.4 microns, so printed circuit boards are a long way from the density that you need to put a bare die semiconductor on.

Johnson: Yet some part of your product needs to be in dimensions that will fit a human finger. It seems that the sorts of dimensions we need in substrate interposers match with the semiconductor fabs of, say, 20 years ago. Those fabs have been decommissioned.

Vardaman: To your point, a substrate facility is not the same as a semiconductor fab. The semiconductor fab is ultra clean, it's processing on silicon, and we're using a wide variety of process equipment. There are some similarities between printed circuit boards and substrates, but as we go forward, the feature sizes are getting increasingly smaller. If you talk to Intel about the future of the substrates they'll need, they will tell you they need finer features and equipment that is more like fab equipment—which is certainly not what is used in the printed circuit board business today.

In a high-end build-up substrate today, they're made with the Ajinomoto film, which is likely very different from what the substrate of tomorrow will be with even finer feature sizes. I hear talk about going down to 2-micron line and space. There's no way that a printed circuit board operation could build anything like that without a clean room and different equipment.

We interviewed a lot of substrate companies, and a single production line could be in the range of $300 million. Intel says that in a facility with multiple production lines doing high volume, you wouldn't be spending less than $1 billion.

R&D Altanova, a test head company in New Jersey, has added some prototype substrate capability, and they certainly can prototype using the Ajinomoto film. It's not like you can't do this in the U.S., but you must recognize what's involved, the equipment that's needed, and the budget you need to do it.

Johnson: What I'm hearing is that substrate manufacturing is neither a PCB nor a semiconductor opportunity. You're not pivoting into this with your existing equipment; you may be investing in a brand-new facility to do this kind of work.

Vardaman: You couldn't do it in an existing printed circuit board facility unless it already has the necessary clean room because when you do fine feature sizes, you can't have particles that would cause failures or yield loss. If you're doing a real production line you need to have it highly automated.

Johnson: Most everything that we're talking about hinges on producing substrates in very large production volumes. So how do OEMs prototype?

Vardaman: It depends on what your market is; defense is not a huge volume. Fujitsu has a very small-scale operation that they do internally for some high-density stuff; it's very small volume. R&D Altanova, as I mentioned, does some prototypes, but the level of investment is not trivial.

This is just for today's requirements, by the way. If you want to scale to the next generation, there are many more considerations on the kind of equipment you need, and what the process is. I see package substrate of the future very different from the PCB production line of today. This means you must approach it with a completely different mindset.

I see package substrate of the future very different from the PCB production line of today. This means you must approach it with a completely different mindset.

Johnson: What does that substrate facility of tomorrow look like? How is it different from the typical PCB fab?

Vardaman: That facility is in a clean room. It has a large amount of automated equipment, metrology to improve process yield, and other capabilities that you may not have in a printed circuit board company today. It's not likely a completely different set of equipment—you might still do some lamination—but your plating and dielectric materials will probably be different.

Johnson: If someone funded and built a facility here in the United States, where will they find the talent to operate it?

Vardaman: You've hit on another problem. As we've seen, the talent pool is somewhat limited. You have to find new people to go into this area, and I'm not sure that the skill set is exactly the same to operate the tools as in printed circuit boards, so you would need to have some training.

Johnson: Where would that facility get their equipment?

Vardaman: They order it from overseas. There are some people in the U.S. planning to make equipment for future production possibilities—glass, for example. I hear a lot of talk about glass. A company just broke ground in Georgia, and I think they're getting most of their equipment from Korea to do a glass panel that you can embed things in, which is an alternative to these laminate substrates. But most people are still looking at laminate substrates, and the lithography equipment, for example, comes from Japan. There are also European equipment suppliers and a few U.S. companies in the market.

It's worth mentioning as well that much of that equipment is backordered for a couple of years. But if you're developing something new—and this is happening—then maybe that equipment set is more like fab equipment that's made by someone here in the United States, like LAM or Applied Materials. But that process is yet to be determined.

People are mostly using steppers for the lithography part; that's Ushio, Inc., a Japanese company. Some have looked at maskless lithography—laser direct imaging—but that's limited with respect to how small your line and space can go. There are plating systems from Atotech, and laser drilling that you probably could use from the printed circuit board side.

First, you would need to select the process for these advanced substrates. Next, you would see what equipment is available, including plating chemistries.

Johnson: If a U.S. company wanted to move into this area, would it make sense to do it in small steps, small volumes first?

Vardaman: Yes, you would first build a prototype line. But a production line will cost at least $300 million—I don't think you can do it for much less, given the equipment cost. To do this properly, an inspection system for metrology alone will be $1 million, and another $1.2 million for the lithography equipment. What's the total once you list out everything from the ground to the building to the equipment?

Johnson: Is there room for the typical U.S. PCB fabricator to get into this business?

> Historically, some printed circuit board suppliers have moved into IC substrate fabrication, but it's been a process over time.

Vardaman: TTM bought the Endicott line and moved it to Wisconsin, so certainly they're pursuing that. Obviously, you could do this. Historically, some printed circuit board suppliers have moved into IC substrate fabrication, but it's been a process over time. Remember, for the next generation of interconnect, it is not clear what level of commitment you must have.

Johnson: It seems to me like this is an opportunity for some of those large OEMs, who need this technology, to put together a consortium and build their own facility.

Vardaman: Those companies design stuff and have it fabricated at high margin. Substrate fab is a low margin business. They're not interested in lowering their gross margins by investing in a low margin business. TSMC doesn't make substrates; they want to establish long-term agreements with people to supply the substrate. They won't make their own and they won't put together a group to do it.

Johnson: Funding a low margin business that allows you to reliably produce your high margin product is one way to look at it.

Vardaman: The numbers just aren't adding up. If you make a new process to make an advanced substrate process, maybe there's a different set of equipment that wouldn't be using this other set of equipment. We'll have to see what players bring that equipment to market. You also need to qualify it all, and it's very complicated. This hasn't happened because it's a very complicated process and procedure.

Johnson: Right now, there is some government funding to help with this, if you put together the right proposal.

Vardaman: There's some government funding, but it's only for a fixed period, so there's a question there. Fundamentally, we don't like to exit our existing supply chain; that's one of the problems we face.

Johnson: Jan, thank you. This has been very helpful.

Vardaman: You're welcome, glad we could chat. **PCB007**

An Advanced Packaging Year in Review

One World, One Industry

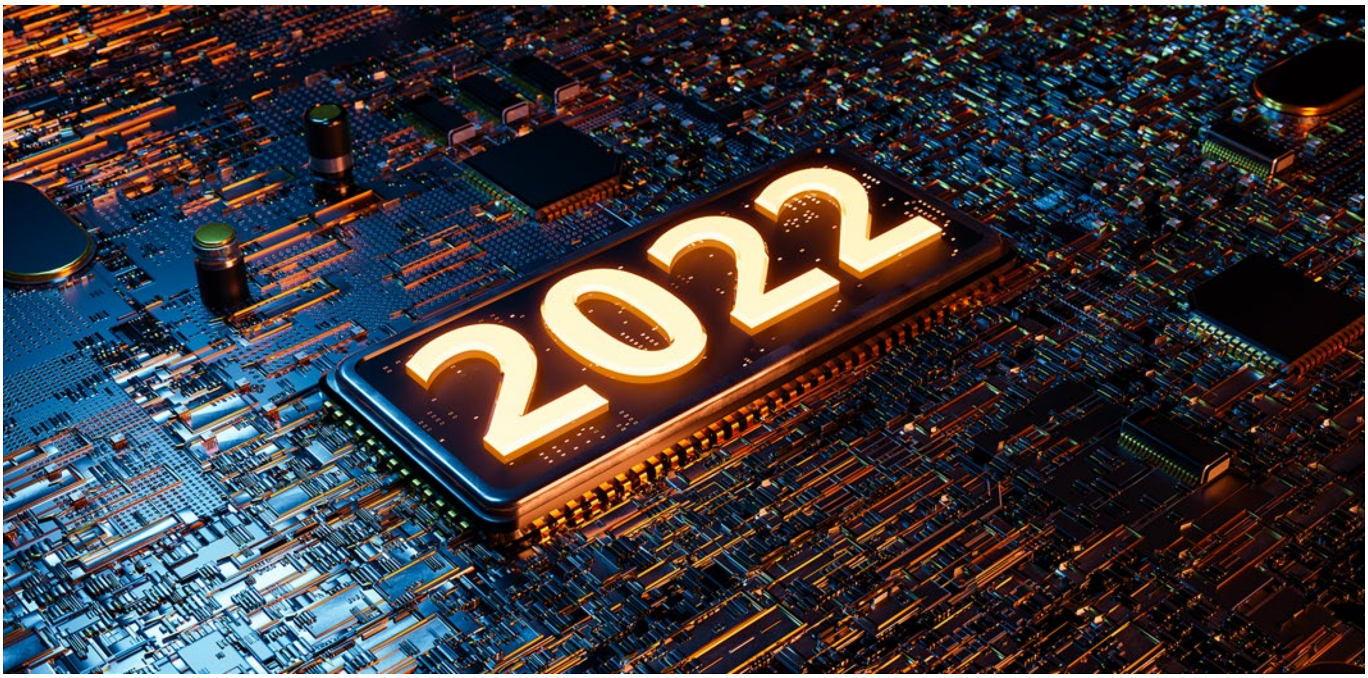
Feature Column by Dr. John W. Mitchell, IPC PRESIDENT AND CEO

Over the past year, IPC has stepped up its efforts to educate policymakers and other key audiences on the importance of investing in the entire semiconductor supply chain to achieve the goals of the recently enacted CHIPS and Science Act, including in advanced packaging and printed circuit boards.

For example, an IPC report last winter found the U.S. has only just begun to invest in advanced packaging, while nations in Asia have sprinted ahead to develop the lion's share of capabilities and capacity[1]. A more recent report by IPC, based on a survey of nearly 100 industry leaders in semiconductors and related fields, revealed that only 29% think government policymakers understand the importance of advanced packaging in driving innovation, and 84% believe government initiatives to bolster the semiconductor supply chain require significant investment in advanced packaging capabilities[2].

An IPC-convened symposium on the topic in October in Washington, D.C., was well attended by representatives of the U.S. government and all sectors of the electronics industry[3].

Progress is also being made on the policymaking front, although much work remains to be done. Most notably, the CHIPS Act includes IPC-backed provisions to invest at least $2.5 billion in advanced packaging capabilities in the U.S. in 2023, and we are continuing to advocate for that objective as the new law is implemented. IPC succeeded in nominating several advanced packaging experts to a new U.S. government advisory panel on microelectron-



ics[4]. IPC also submitted official comments on the issue to both the U.S. Department of Commerce and the European Commission, both of which are planning major investments in the semiconductor supply chain in 2023. Finally, IPC and our colleagues at the Printed Circuit Board Association of America (PCBAA) and the U.S. Partnership for Assured Electronics (USPAE) are working to persuade President Biden to issue a determination that PCBs and IC substrates deserve priority U.S. government action under Title III of the Defense Production Act.

Our message to policymakers is that building a more robust, domestic ecosystem for advanced electronics will require four key policy decisions:

1. Invest in advanced packaging capacity. The CHIPS Act makes $39 billion available over five years for government investments in manufacturing capacity. Much of this funding will go to silicon fabricators, but at least nine figures should be earmarked for advanced packaging segments, including integrated circuit (IC) substrate fabrication and final component assembly and test, with a focus on building short-term capacity both organically and through foreign investment or partnerships.

2. Invest in research and development. The U.S. is 10 to 20 years behind its peers in advanced packaging, especially IC substrate fabrication. Playing catch-up is a losing strategy, so the U.S. needs to invest in leapfrogging technological advancements. Fortunately, the CHIPS Act allocates $2.5 billion for advanced packaging R&D, funds that should be used to support innovations in equipment, materials, and processes that support advanced electronic interconnection.

3. Promote supply chain partnerships over supplier relationships. Component makers and their suppliers need to see each other as partners rather than as customers and suppliers. Partners support each other's success; customers too often seek the lowest price, regardless of whether that decision weakens a supplier's ability to remain solvent and invest in new capabilities. In the context of rising geopolitical tensions and global supply chain risks, customers and suppliers are dependent upon each other's success, and business relationships should reflect this fact.

4. Make strategic decisions on what we are building and for whom. The global electronics supply chain has largely moved out of the United States and allied European nations; bringing the supply chain back to these regions is highly unlikely. Instead, the U.S. government needs to determine what items need to be made in the U.S. and allied countries—either for strategic autonomy or security purposes—and then focus on building capabilities accordingly.

Looking ahead to 2023, IPC will continue to advocate for the entire semiconductor supply chain in every policy-making arena. If you're interested in supporting our efforts, please contact myself or Chris Mitchell, IPC's vice president of global government relations. PCB007

References

1. "An Analysis of the North American Semiconductor and Advanced Packaging Ecosystem: Rebuilding U.S. Capabilities for the 21st Century," IPC.org, November 2021.
2. "Towards a Robust Advanced Packaging Ecosystem," with a forward by John Mitchell, IPC.org, 2022.
3. "IPC Advanced Packaging Symposium: Building the IC-Substrate and Package Assembly Ecosystem," IPC.org, October 2022.
4. "Industry Well Represented on New U.S. Government Advisory Committee on Microelectronics," IPC.org, Sept. 30, 2022.

Dr. John W. Mitchell is president and CEO of IPC. To read past columns, click here.

Heterogeneous Integration Technologies Driving Advanced Packaging Solutions

Feature Article by Charles Woychik
SKYWATER TECHNOLOGY FOUNDRY

The future of the semiconductor industry is to disaggregate a large system-on-chip (SoC) device into smaller cells, called chiplets. This is where each cell will utilize the semiconductor node that maximizes its performance. In this scenario, some chiplets will continue to use mature legacy node technologies to ensure optimum performance along with lower cost. Other cells will require finer nodes to achieve performance objectives, which will be more costly. By using this approach, node scaling will continue, but only for cells (or chiplets) that require it. This is a much more cost-effective approach for delivering state-of-the-art semiconductor solutions, referred to as heterogeneous integration (HI).

A benefit of HI packaging is the ability to integrate multiple chiplet functions to achieve enhanced performance as compared to a monolithic SoC. This approach can reduce the time to market and cost but requires a robust and reliable method to package these chiplets. Figure 1 lists the pros and cons for HI. One of the major obstacles to implementing HI is the need to develop an integrated ecosystem for manufacturing, especially a domestic source.

HI packaging technology is revolutionizing the world of microelectronics. By combining

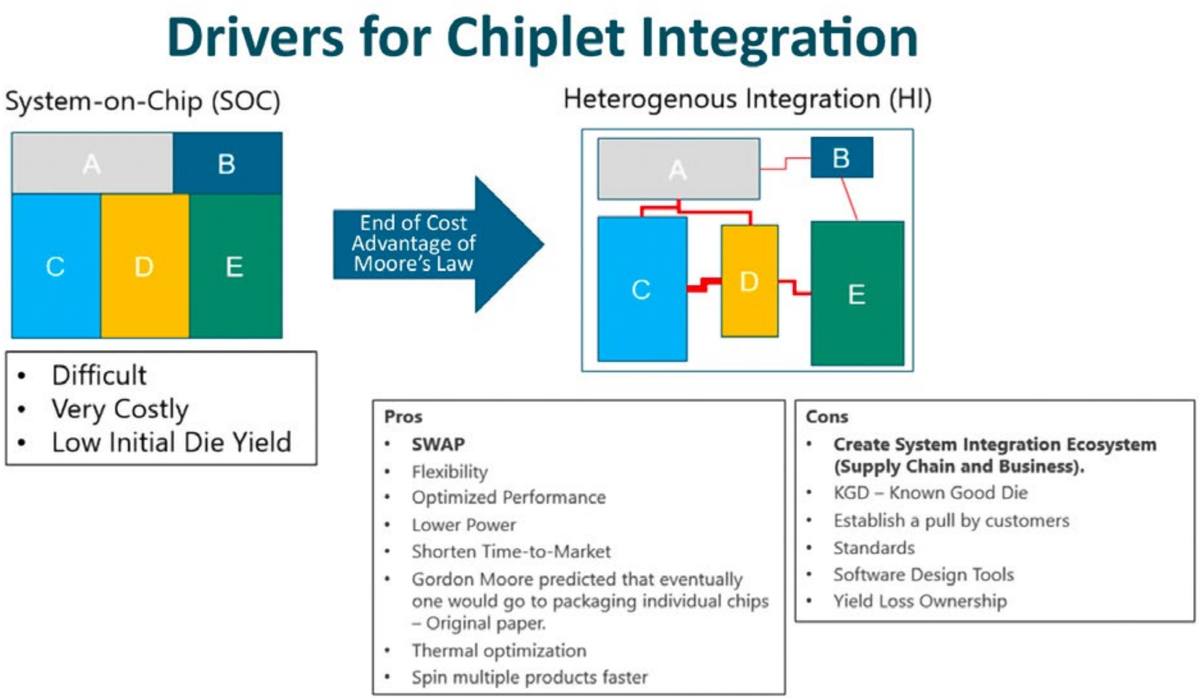


Figure 1: HI using chiplets offers many advantages over conventional SoC, but creating a viable HI ecosystem requires overcoming several challenges.

different types of chips and components into a single package, manufacturers can create more powerful and efficient devices than ever before.

One of the challenges of advanced HI is the complexity of designing and manufacturing these packages. The process requires advanced technologies and specialized equipment, making it necessary for manufacturers to invest in research and development to stay at the forefront of this technology.

One of the challenges of advanced HI is the complexity of designing and manufacturing these packages.

HI utilizes technologies and architectures that allow chiplets to be interconnected in very close proximity to one another, achieving a reduced package area and faster electrical interconnections between the components. Current HI package structures that are widely implemented in the industry include silicon (Si) interposers; fan-out wafer level packages (FOWLP) on build-up substrate; and FOWLP packages without substrates, as shown in Figure 2.

Silicon interposers provide high-density electrical routing between interconnected chiplets. In Figure 2a, the Si interposer acts as a lateral bridge between the processor die and the stacked memory die. In addition, it provides routing from the high-density chiplets assembled on the top of the interposer to the build-up substrate below using through silicon vias (TSVs). In this package configuration, a build-up substrate is required to provide vertical routing between the higher density Si interposer and the PCB. Challenges for this package are a reliable source for the Si interposer, a complex assembly process requiring underfill and high-accuracy chip attach, and managing the stresses due to the coefficient of thermal expansion differences between multiple stacking levels. For Si interposers, the CTE will be around 3-4 ppm/°C, while an organic build-up substrate will have CTE ranging from 8-11 ppm/°C; this CTE mismatch will have to be resolved with materials selection and package design.

Another solution is to integrate chiplets in a FOWLP package stacked on a build-up substrate, which is then mounted to the device PCB (Figure 2b). This package has the advantage of eliminating the Si interposer. Now the CTE of the FOWLP package is closer to that of the organic build-up substrate.

In addition to eliminating the need for a Si interposer, FOWLP enables the reduction of build-up layers in the substrate. FOWLP

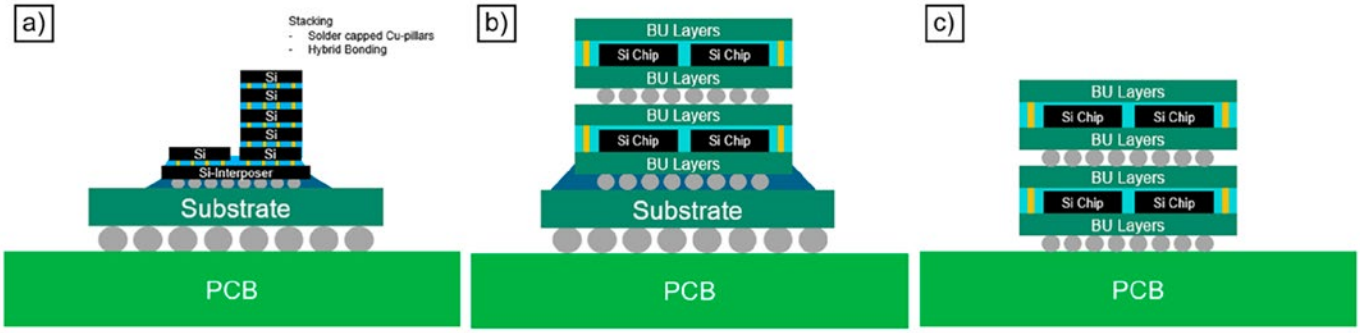
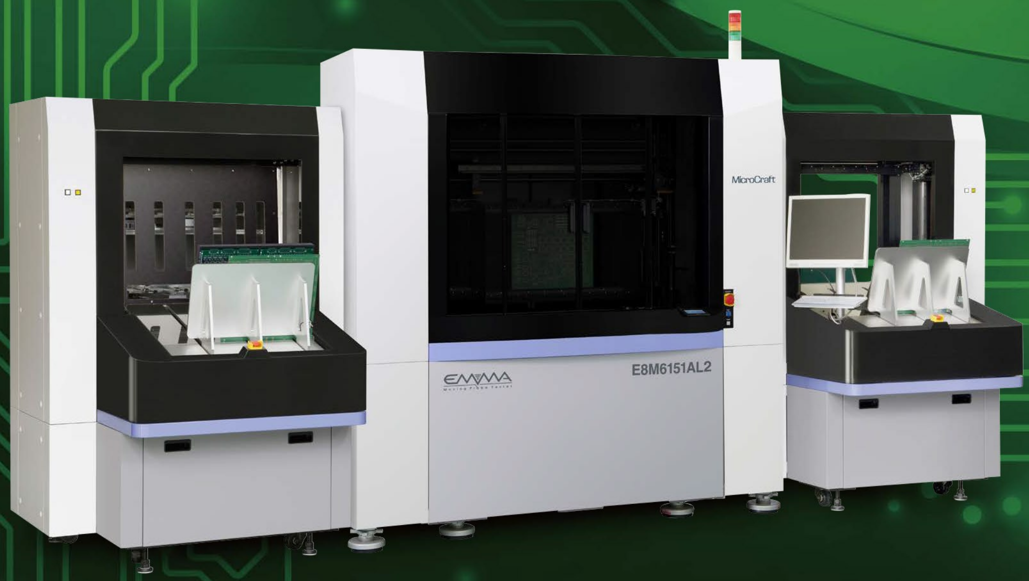


Figure 2: Pathways to advanced heterogenous integration using a) silicon interposer; b) fan-out wafer level packaging on build-up substrate; and c) fan-out wafer level packaging without substrates.

Fully Automated Unattended Operation

Over 1,900
Machines Installed Worldwide
(as of March 2020)
EMMA Series
★★★★★



EMMA
Moving Probe Tester

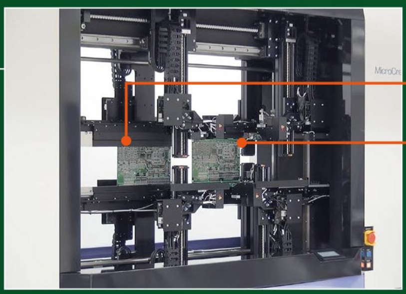
10,000
Test Points/mins.

Load up to
200 pcs

E8M6151AL2

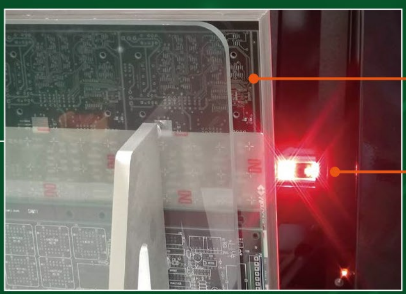
Increased Throughput

Transfer speed reduced by **37**%



Built-in Scanner for Seamless Job Changeover

Improved Efficiency for high-mix boards



MicroCraft

USA MicroCraft, Inc.
1247 N Tustin Ave, Anaheim, CA 92807
TEL (714) 482-2550
www.usamicrocraft.com
sales@usamicrocraft.com

Visit Our Website

Watch Video

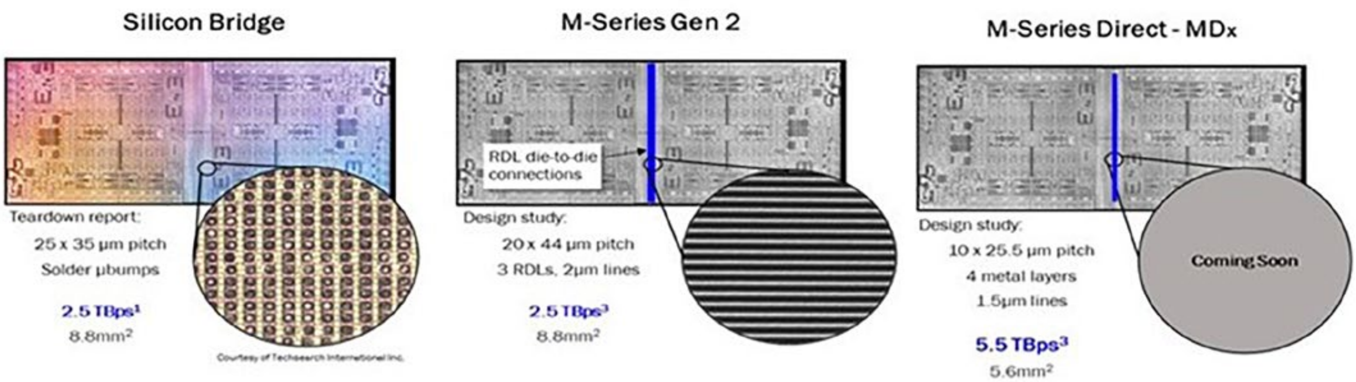


Figure 3: Comparison between heterogenous integration packages using a) an embedded silicon bridge die; b) M-Series Gen 2; and c) M-Series Direct (MDx).

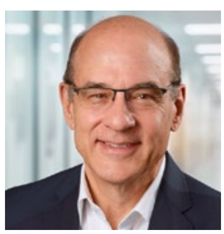
can reduce the number of build-up layers in the substrate by embedding active components and bridge die directly into the FOWLP structure, and by using through mold copper posts that allow direct vertical interconnection between different layers. These structural features allow elimination of additional routing layers in the build-up substrate.

Furthermore, FOWLP can be directly assembled to the PCB without the use of a build-up substrate (Figure 2c). In this package, advanced high-density interconnect in the RDL build-up layers of the FOWLP can provide interconnection between the high-density chiplets to the low-density device PCB. Another advantage of this package configuration is the ability to commit only known good modules (KGMs), of the high-density chiplets to the fan-out package in the build-up process. FOWLP can provide a simpler vertical package build-up structure with less interfacial stress and a lower package cost, resulting in better overall package reliability.

Deca Technologies' M-Series is a key technology that enables FOWLP to act as an organic high-density interposer to provide lateral and vertical interconnect between chiplets without the use of a silicon interposer or a build-up substrate. M-Series Gen 1 RDL build-up has 10 µm L/S and can accommodate 50 µm bond pad pitch. M-Series Gen 2 scales down to 2 µm L/S with 20 µm bond pad pitch. Deca's roadmap will drive down the interconnect scaling to 1.5 µm L/S and beyond for the succeeding M-Series generations. M-Series Gen 2 will enable a high-density fan-out technology solution for many applications. Figure 3 makes a comparison of M-Series Gen1 with silicon bridge technology and shows how future M-Series Direct (MDx) with 1.5 µm L/S can further improve the circuit density and performance.

Skywater is currently working with Deca Technologies to bring M-Series Gen 2 and future technologies to our advanced packaging facility in Kissimmee, Florida, to drive the next generation of advanced packaging onshore. FOWLP technology eliminates the use of a Si interposer and build-up substrate, simplifying the structure of future 3D solutions.

The benefits of FOWLP make it a promising technology for the future of microelectronics. As this technology continues to evolve, we can expect to see more powerful and efficient devices that offer improved performance and functionality at a lower cost. **PCB007**



Charles Woychik is senior director of advanced packaging platforms at SkyWater Technology Foundry.


NEW!
Community
MAGAZINE
WINTER 2023
IPC
BUILD ELECTRONICS BETTER

Advanced Packaging Not a Passing Fad

Elementary, Mr. Watson

Feature Column by John Watson, CID, ALTIUM

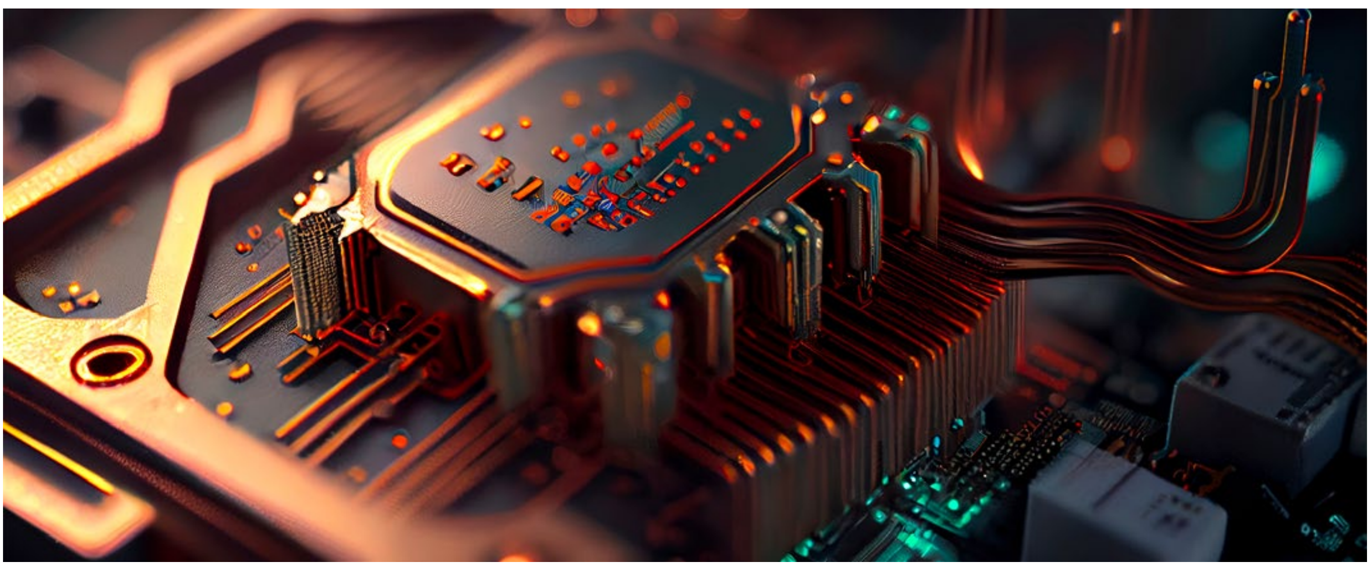
We live in what can only be described as the golden age of electronics. Advancements and innovations grow by leaps and bounds, and never in history has the field of electronics grown at such a fantastic rate. Yet necessity is the mother of invention when discussing the PCB design industry and the advanced integration packages field is one of the fastest-growing and most exciting.

In 2020, the advanced packaging market was worth $24 billion and it's expected to grow as the estimated compound annual growth rate (CAGR) is 8%[1]—phenomenal growth resulting from consumer demand. It's an insatiable appetite for something bigger and better, not only with higher speeds in a smaller package, but to be inexpensive; this is what drives our industry and keeps us employed. This demand is on full display when Apple releases its latest and greatest, and folks are camped out for days waiting for the release. This trend shows no signs of slowing down. One solution to high demand? Advanced packaging. As legislation with the CHIPS Act focuses on domestic semiconductor fabrication, the aim should be to increase the advanced package industry into the mainstream.

Challenges with Advanced Interconnect

Ever since Jack Kilby of Texas Instruments created the first hybrid IC made of germanium in 1958, and Robert Noyce created the first monolithic IC in 1959, the IC has generally remained the same—except for one significant difference in reducing the size of the transistors that make up every IC. When Kilby and Noyce created the first ICs, the size of the transistors was 11 nm. With today's smaller transistors, more nodes, as they are called, are now inside each IC.

By 1965, Gordon Moore estimated that a computer's speed and capability could expect



to double every two years because of increases in the number of transistors a microchip can contain. It was a shocking statement when Moore announced that a single IC would someday hold 65,000 transistors. The size of IC nodes is now being mass-produced at 5 nm, which was commercially released in the Apple A14 Bionic chip. The transistor count now sits at a staggering 11.8 billion, a 38.8% increase from the A13's transistor count of 8.5 billion.

By 2024, the expectation is to be even smaller at 2 nm. For perspective, that is smaller than human DNA and could hold over 50 billion transistors on a chip the size of a fingernail.

But before we pop the cork on the champagne, I believe we have reached or are very close to reaching the limits of our capability to produce chips reasonably and reliably. As things shrink, simply controlling the current flow in such a small area is very difficult. In other words, we are now getting so small that we can no longer control the electrons.

As things shrink, simply controlling the current flow in such a small area is very difficult.

We are simply running out of room. Many believe that Moore's Law is dead, particularly NVIDIA CEO Jensen Huang, who proudly announced his belief in this idea last year. I am not at that point yet, but it does feel like Moore's Law is on life support. Although we call it a law, even Moore agreed it was more of an observation. In his 1965 publication, *Cramming More Components onto Integrated Circuits,* he admits "including micro-assembly techniques for individual components, thin film structures, and semiconductor integrated circuits. Each approached evolved and rapidly and converged." In an interview in April 2005[2], Gordon Moore stated that the projection could not be sustained indefinitely: "It can't continue forever. The nature of exponentials is that you push them out, and eventually disaster happens." He also noted that transistors eventually would reach the limits of miniaturization at atomic levels:

In terms of size [of transistors], you can see that we're approaching the size of atoms which is a fundamental barrier, but it'll be two or three generations before we get that far—but that's as far out as we've ever been able to see. We have another 10 to 20 years before we reach a fundamental limit. By then, they'll be able to make bigger chips and have transistor budgets in the billions.

Another major problem we face is making all the interconnects to a high-density device so that it's a functional item on a PCB design. Conventionally it's done through wire bonds, which have not scaled down at the same pace as the transistor. With 11.8 billion transistors in a single chip, that is more processing power than wires can carry. Getting signals from the silicon out to the real world, which connects to the PCB, is a significant issue.

Frankly, we are reaching the industry limitations in more ways than one.

A Paradigm Shift of Advanced Packaging

Occasionally it's good practice to examine how we do things. Advanced packaging technology (APT) is a paradigm shift for the entire industry. It promises to solve the challenges we face. We can define APT as the aggregation and interconnection of components before traditional electronics packaging. Advanced packaging allows multiple devices (electrical, mechanical, or semiconductor) to be merged and packaged as a single electronic device. They are taking different circuits that were separate chips on the PCB design before and placing them all in a single chip.

Although we are not specifically talking about applications when speaking of APT, we will find

Congress Needs to Support American Made Printed Circuit Boards

OUR FOCUS

TO CREATE A MORE RESILIENT AND SECURE SUPPLY CHAIN, WE NEED TO BRING PCB MANUFACTURING BACK TO AMERICA. PASSING H.R.7677, THE SUPPORTING AMERICAN PRINTED CIRCUIT BOARDS ACT, WILL REINVIGORATE OUR INDUSTRY AND MAKE US MORE COMPETITIVE.

PCBAA advocates, educates, and champions legislation and policies that support this critical American industry.

JOIN US TODAY

PCBAA.ORG

PCBAA

that particular packaging methods are popular with various industries. For example, high-end AI products such as smartphones and graphic processing units lean more toward 2.5D technology. The industry demands target specific applications and markets with how the various individual circuits are combined with the packaging methods.

The various methods of advanced packaging are listed below.

- Wafer level packaging
- 5D and 3D
- System-in-package
- Bumping and flip-chips
- Chip scale packages
- Redistribution layers
- Embedded die substrate
- MESM and microsystem packaging

Inherent Problems With APT

The APT comes with several inherent problems. First is power dissipation and power use; directly connected to that is the increase and necessity of heat dissipation. Traditionally, silicon generates a lot of heat and is not thermally efficient. It is now seeing a decrease in voltages, but to maintain or increase the power means an increase in current. How is this power migrated through the package and the heat dissipated? Even just a single chip can have problems with power consumption and heat. Now we combine them with other items such as in a system-in-package (SiP) that also holds the microprocessor, the flash, and the SRAM all in a single chip. We've just increased the issue exponentially.

Known Good Die (KGD)

When combining the various individual parts, especially when designing a SiP design package, It is unknown whether an individual circuit works until it is in the final package configuration. Because specific devices cannot be adequately tested beforehand, the failure rate is high and expensive due to lost production time. That is an issue known to the industry as "known good die." How the individual dies are tested and validated must be solved. Usually, one only finds out about these issues after it's too late.

Cost Issues

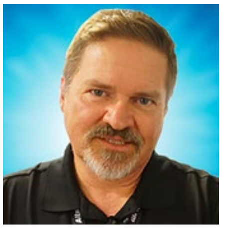
Most integrated circuit manufacturers' equipment is not ready for the onslaught of advanced packaging. The equipment for such a process is highly specialized and expensive. This specialty requirement is driving up the cost of APT devices on the market. In the future, we should expect that costs should come down.

Conclusion

Advanced packaging technologies have a bright future. The insatiable appetite that the everyday consumer is looking for and expecting from their devices is increasing. It drives this new technology—one that is now mainstream as we finally put to rest Moore's Law and change how we look at the semiconductor industry with a major paradigm shift. Instead of simply looking at increasing node density, we can now customize based on entire sections of circuits for a specific industry and application. It's an exciting time. **PCB007**

References

1. Advanced Packaging Market Size to Hit Around US$41.8 Bn by 2030," Nov. 10, 2021, GlobeNewswire.
2. "'Moore's Law is dead,' says Gordon Moore, by Manek Dubash, Techworld, April 13, 2005.



John Watson, CID, is customer success manager at Altium, a professor at Palomar College, and an I-Connect007 columnist. To read past columns, click here.

MilAero007 Highlights

Defense Speak Interpreted: SWaPing Nanosatellites for Defense Systems ▶

When I say "SWaP," you might be thinking: A swap for what? What's in the trade? SWaP, in fact, stands for size, weight, and power—the holy grail of technical performance for defense systems.

Essemtec: Manufacturing Moves In-house ▶

Pete Starkey talks with Kevin Domancich at Essemtec about the company integration within Nano Dimension and how the two companies have pioneered an exciting new end-to-end manufacturing solution that helps customers speed up production, cut costs, and keep their proprietary materials secure. In a world where time to market has become a priority consideration, this universal system has the potential to revolutionize the industry.

Collins Aerospace Opens New Engineering and Global Operations Centers in India ▶

As part of a significant investment to expand its engineering, digital technology, and manufacturing operations in India, Collins Aerospace, a unit of Raytheon Technologies Corp., has officially inaugurated its new Global Engineering and Technology Center (GETC) and Collins India Operations Center in Bengaluru.

Polar Instruments: Simulating PCB Potentialities ▶

Nolan Johnson checks in with Polar's Martyn Gaudion on the evolving needs of global PCB manufacturing markets in a post-pandemic world, where generating accurate PCB specification documentation is essential to successfully navigating today's rampant supply chain constraints.

Raytheon Missiles & Defense, TTM Technologies Reach Agreement to Purchase SPY-6 Radar Components ▶

TTM Technologies, Inc. and Raytheon Missiles & Defense, a Raytheon Technologies business, have reached a multi-year agreement to provide radio frequency assemblies, electronic hardware, and printed circuit boards for the SPY-6 family of radars. The agreement has the potential to reach $500 million over five years.

NextFlex Announces Over $8M in Funding for Flexible Hybrid Electronics ▶

NextFlex, America's Flexible Hybrid Electronics (FHE) Manufacturing Institute, announced $8.45 million in funding (including $4.25M in cost-share contribution from participants) for nine new projects as part of its Project Call 7.0 to further promote FHE development and adoption throughout the U.S. advanced manufacturing sector.

NASA, SpaceX to Study Hubble Telescope Reboost Possibility ▶

The non-exclusive SpaceX study regarding the possibilities of reboosting the Hubble Space Telescope is ongoing. Last month, NASA issued a Request for Information to seek additional information about commercial capabilities available to reboost a satellite in orbit, using Hubble as a demonstration, at no cost to the government.

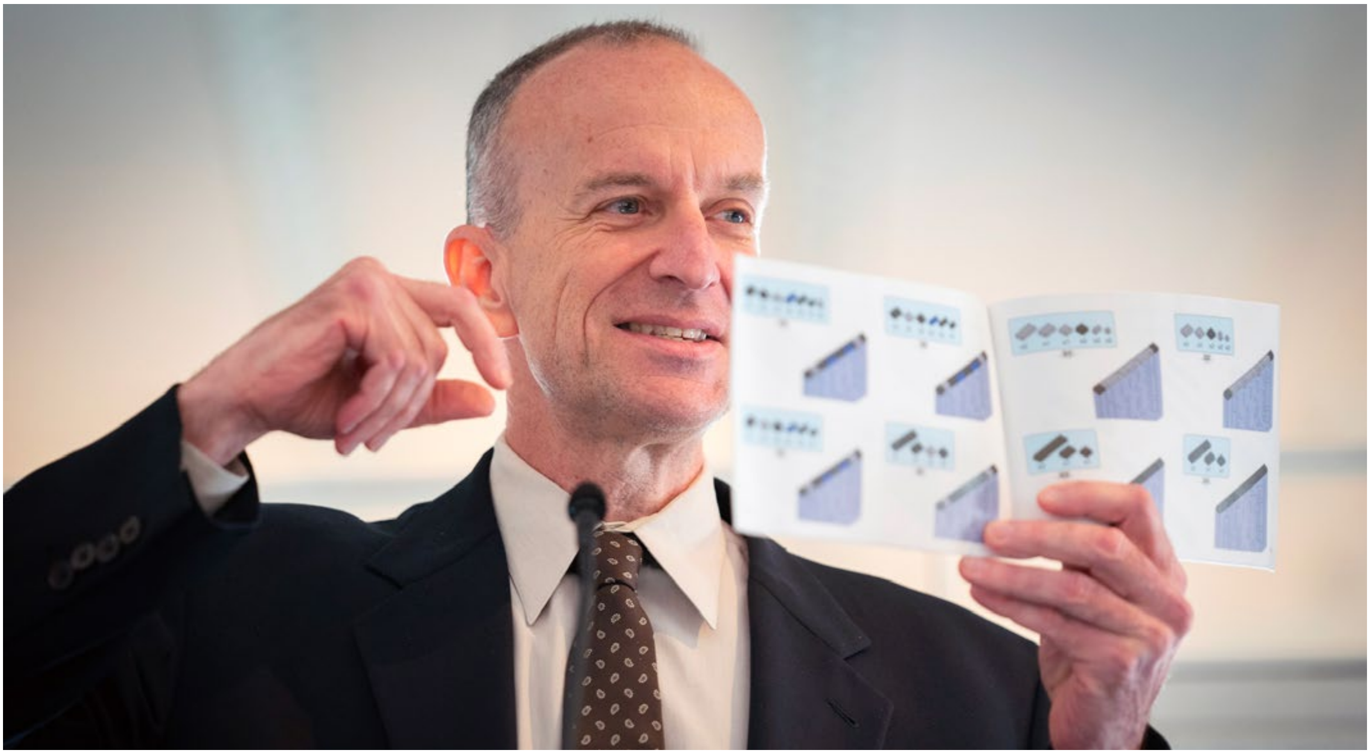


Photo credit: John Harrington

Advanced Packaging Beyond the Zetabyte Era

Feature Article by Tom Rucker
INTEL

As the industry continues to aggressively pursue Moore's Law, the technology envelope and solution space has grown to include packaging. Historically, the role of the package was to protect the die from the environment and to scale the small geometries of the die to the significantly larger pitches of the system board. Moving forward, the package is also being used to interconnect multiple die in one unit. This facilitates assembling die from different technology nodes into overall smaller form factors with higher performance. The industry refers to this approach generally as "advanced packaging," or heterogeneous 3D integration. Across market segments, from computing to communications to defense, products that use advanced packaging technologies are becoming more prevalent.

The importance of packaging technology is reflected in its prominent inclusion in the U.S. CHIPS and Science Act. The law establishes the National Advanced Packaging Manufacturing Program (NAPMP), which seeks to "strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem." These provisions demonstrate that the importance of packaging technologies has spread beyond the technology industry into the realm of policymaking. Programs funded in the CHIPS Act ensure that the U.S. will continue to drive important advances in packaging technologies, supporting efforts to rebalance global chipmaking capability and capacity. This onshoring will both strengthen the overall supply chain and ensure the fulfillment of critical domestic market require-


METALS
TRI-CORE
AN ALL AMERICAN PRODUCT
ROSIN
SOLDER WIRE
FILLED

ments. The funding will allow the U.S. to accelerate the development of innovative packaging technologies that will support new revolutionary and evolutionary end products. The Department of Commerce is currently working on the details of the NAPMP implementation plan, with more details expected in early 2023.

Delivering on the goals set by the CHIPS Act requires development in a wide variety of technical domains and the integration of these diverse building blocks. The processing components can be separated into three general functional areas: wafer-, panel-, and unit-level processing.

Delivering on the goals set by the CHIPS Act requires development in a wide variety of technical domains and the integration of these diverse building blocks.

Wafer processing steps, which follow the manufacturing flow of building and interconnecting the transistors on a die, involves electrically connecting multiple die. These die can be side by side and connected through a polymer/metallization structure, or they can be stacked on top of each other with connections composed of solder or copper. A multitude of architectures have been developed by the industry, each optimized for the final product performance and cost targets. These wafer-based processing steps take advantage of the tools and extensive experience of the wafer fabrication industry.

Panel-based processing steps support a variety of use cases, from building substrates (packages) where one die is attached, to being an alternate approach for interconnecting multiple die in the same unit through different process flows. Based on package body size, die count, and total die area, panel-based processing can offer a lower-cost alternative to wafer-based processing. Panel-based processing benefits from higher panel utilization for larger package sizes relative to wafers and a higher number of units per panel. Like the economies of scale the semiconductor industry achieved in the transition from 200 mm to 300 mm wafers, panel processing achieves equivalent benefit over wafer processing. In addition, advances in panel-based technologies and materials enable unique solutions for a variety of market segments such as communications and computation.

However, there are challenges that need to be overcome to proliferate panel-based processing. For example, the materials, process equipment, and facilities to build advanced substrates is becoming closer to wafer fab equipment, and so equipment development is needed. The smaller geometries of panel-based processing require clean environments, advanced lithography, and higher performance dielectrics, among other materials. Panel handling needs to improve to increase line yield. These capabilities can be applied to other industries such as display and board manufacturing, which further incentivizes scaling these technologies to the level required to overcome the unique defect, quality, and reliability challenges facing the panel testing industry. Packaging provisions from the CHIPS Act may accelerate these efforts.

Unit-based processing can be viewed as the continued evolution of what is commonly referred to as assembly and test. This manufacturing stage also requires technical advances to support higher thermal loads and tighter pitches.

Many products require processing using all three advanced flows—wafer, panel, and unit. For example, the Intel® Data Center GPU Max Series product has approximately 100 billion transistors in a 47 tiles/die package. These

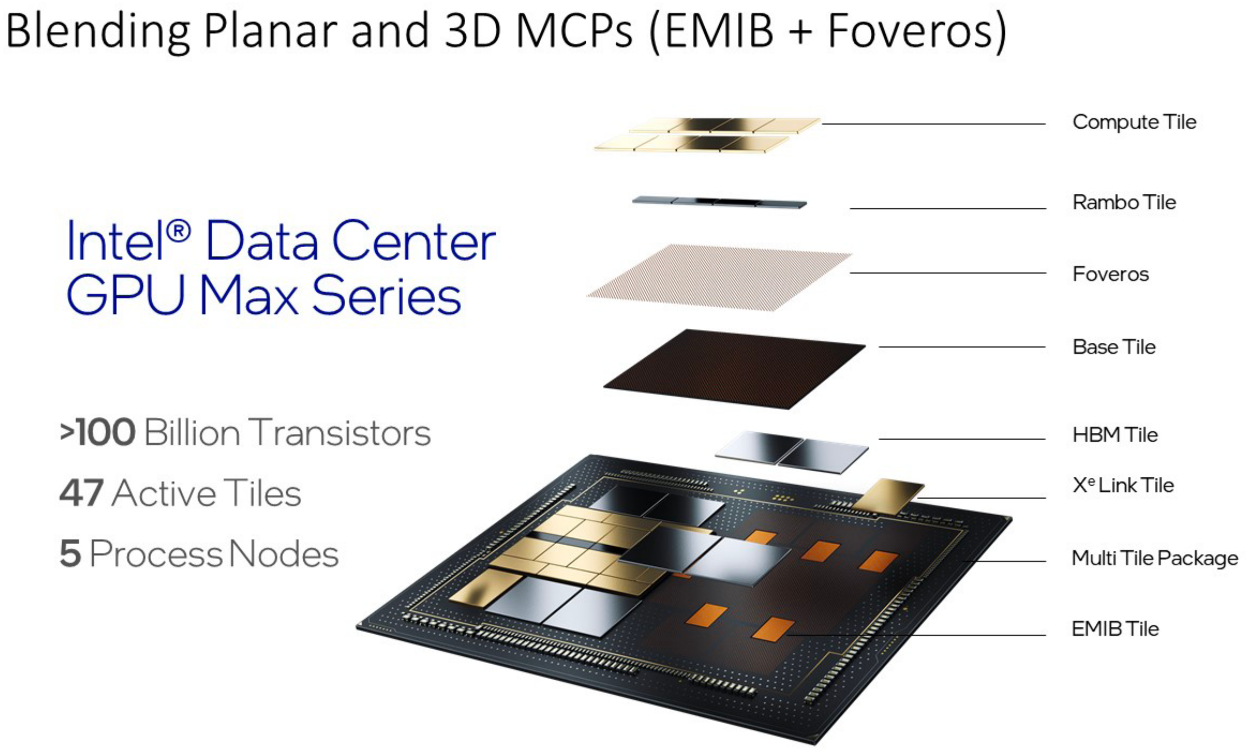


Figure 1: The Intel® Data Center GPU Max Series, an example of a complex advanced package product.

products feature multiple advanced packaging technologies, including die stacked on different die, die embedded into the package, multiple die stacks attached to the package, and an advanced thermal solution. This "mix and match" architecture gives product designers the flexibility to deliver the best products.

Across all these manufacturing stages, demonstrating economic viability for domestic manufacturing will require dramatic changes to how factories and process tools are designed. Output per tool must improve significantly, while labor content needs to decrease significantly—each by an order of magnitude. This represents both a challenge and an opportunity for the industry and should become an area of focus for programs launched under the CHIPS Act.

Ensuring the final packaged products meet the stringent quality and defect levels requires significant testing—both in-line and at end of line. With current products requiring 100 billion transistors and projections calling for 1-trillion-transistor products around 2030, the challenge is large. These products have tight performance targets and must be able to perform under broad use conditions.

Yield management with multiple die in one unit requires performing high levels of test coverage and defect management within the process flow. The cost impact of yield loss is significant. Testing for advanced packaging has the unique characteristic of needing to test and verify the performance and reliability of all die ahead of package assembly. Rather than simply sorting wafers to look for gross fab defects, die testing needs to test for both fab defects and some performance characteristics; further, this process needs to stress not only individual die, but stacks of die as well. Post-assembly, devices must be tested for assembly defects, stressed, classified, and run at the system level for optimal performance characterization, as well as quality and reliability verification.

In addition, if the final unit is composed of mixed technology node components such as digital, analog, optical, and/or MEMs, the testing methodology is further complicated

by different test requirements and capabilities needed for each subcomponent, in addition to verifying that the complete, integrated units perform to specifications. A further challenge with advanced packaging is determining the optimum locations in the process flow for the different testing steps, to balance costs and yield management, as well as the scalability of the test and measurement solutions themselves.

The world is moving to zeta-scale computing, driven by the exponential growth of data that needs to be collected, stored, and analyzed. As this trend continues, advanced packaging becomes a requirement to meet the performance and dimensional requirements of these systems. Breakthrough technologies across design and manufacturing are needed to successfully deliver innovative products and capabilities. Innovation in computing products requires major advances in advanced packaging over the next few years, a development that promises to usher in a new and exciting era of opportunity for the industry. PCB007

Tom Rucker is vice president of technology development at Intel.

NIST Resources for CHIPS Act Participants

Article by Nolan Johnson

At the recent IPC Advanced Packaging Symposium, Dr. Frank W. Gayle, deputy director of the Advanced Manufacturing National Program Office, an interagency team with core staff hosted at the U.S. National Institute of Standards and Technology (NIST), gave a presentation on the work NIST has recently undertaken in support of both the semiconductor and R&D sectors, and the CHIPS and Science Act.

In Gayle's presentation, he said the vision for the CHIPS and Science Act (also known as the CHIPS Act) is to develop and preserve three key areas: economic security, national security, and future innovation.

He emphasized that the CHIPS Act is about more than just the semiconductor chips, reserving an entire slide for that point alone. While NIST acknowledges that the U.S. holds an impressive 85% stake in the semiconductor design market, only 3% of the global packaging industry resides within the U.S. (Figure 1).

Figure 1: The U.S. has a majority stake in semiconductor design but trails behind the rest of the world in both manufacturing and packaging[1].

In support of this mission, Gayle drew attention to a series of resources that are now available on NIST.gov:

- **Metrology and Standards**
  "Strategic Opportunities for U.S. Semiconductor Manufacturing: Facilitating U.S. Leadership and Competitiveness through Advancements in Measurements and Standards," August 2022.
- **Stakeholder Input on CHIPS Act**
  "Incentives, Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry: Summary of Responses to Request for Information," August 2022.
- **Commerce Strategy for Implementation**
  "A Strategy for the CHIPS for America Fund," September 2022.
- **Semiconductor Supply Chain RFI Findings**
  "Results from Semiconductor Supply Chain Request for Information," January 2022.

Gayle concluded that the Incentives Program application process will be announced in February 2023 with funding proposals considered on a rolling basis. Learn more about the CHIPS Act at nist.gov.

References

1. Data courtesy of the U.S. Department of Defense and IPC.

Protocols for a Smart Factory Future

Happy's Tech Talk #16

by Happy Holden, I-CONNECT007

Introduction

Karl Dietz never wrote on automation and the Smart factory, but these topics have been a priority for larger OEMs since the early 1980s. I became involved in automation planning after designing and building Hewlett-Packard's printed circuit fabrication facility in Sunnyvale, California. This was the first fabrication facility to demonstrate the capability of computer process control and management planning. Soon after, I moved into the role of automation consultant for HP with its introduction of the Manufacturing Productivity Network (MPN) for a product line of computers, software, and data acquisition systems.

Starting the Process

The journey to a Smart factory is evolutionary; it starts with a thorough business plan that charts a roadmap for your enterprise into the future. That roadmap will have six stages (Figure 1):

1. Environmental assessment
2. Program strategy
3. Conceptual design
4. Detailed design and requirement specifications
5. Development
6. Implementation

Mechanization was the primary focus of automation in the 1980s and '90s, with an emphasis on robotics and continuous product flow. The focus of Industry 4.0 has been on sensors, data collection, data aggregation, data analysis/analytics, business intelligence/corrective actions, and predictions (digital twins) or systemization. As seen in Figure 2, the emphasis is now on analytics and optimizations in all forms.

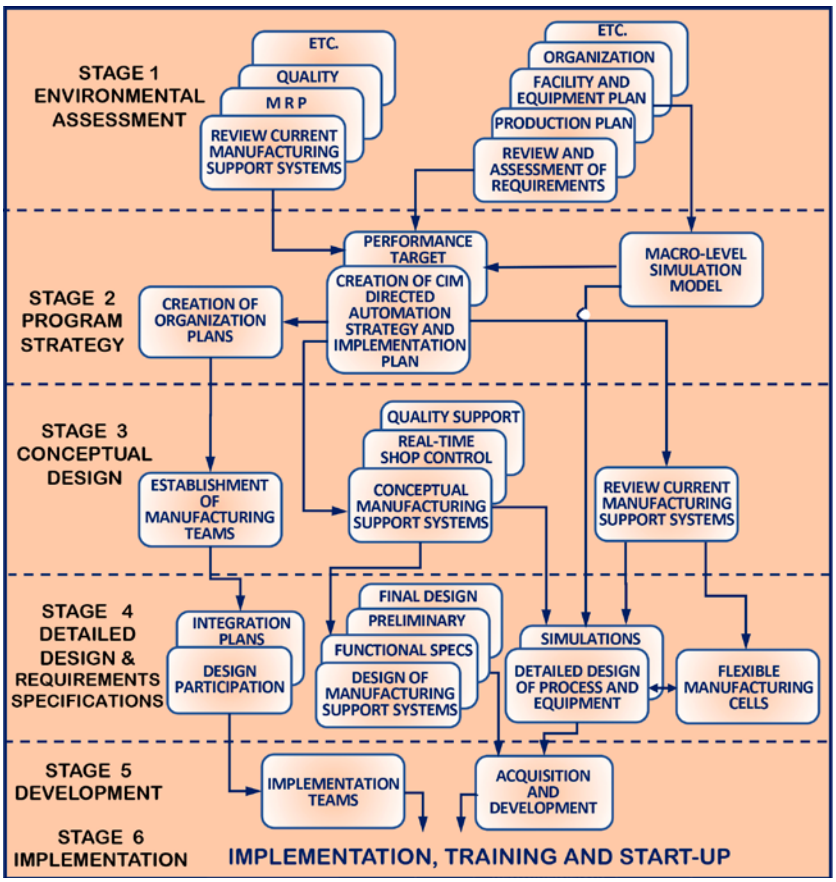


Figure 1: The six stages of planning for a Smart factory[1].

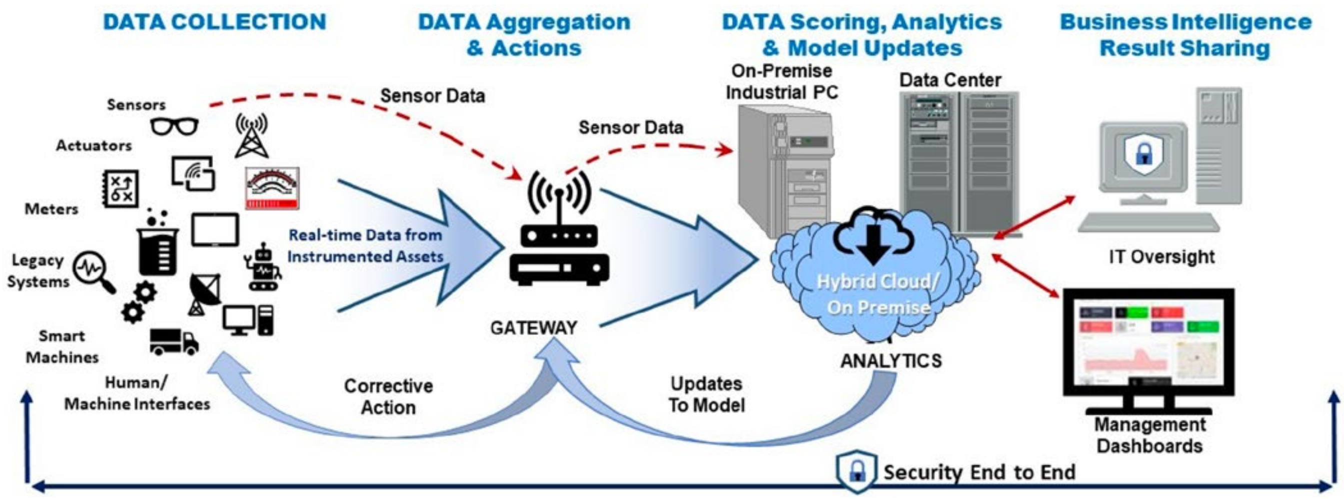


Figure 2: The Smart Factory emphasis is on data collection, aggregation, and analytics[2].

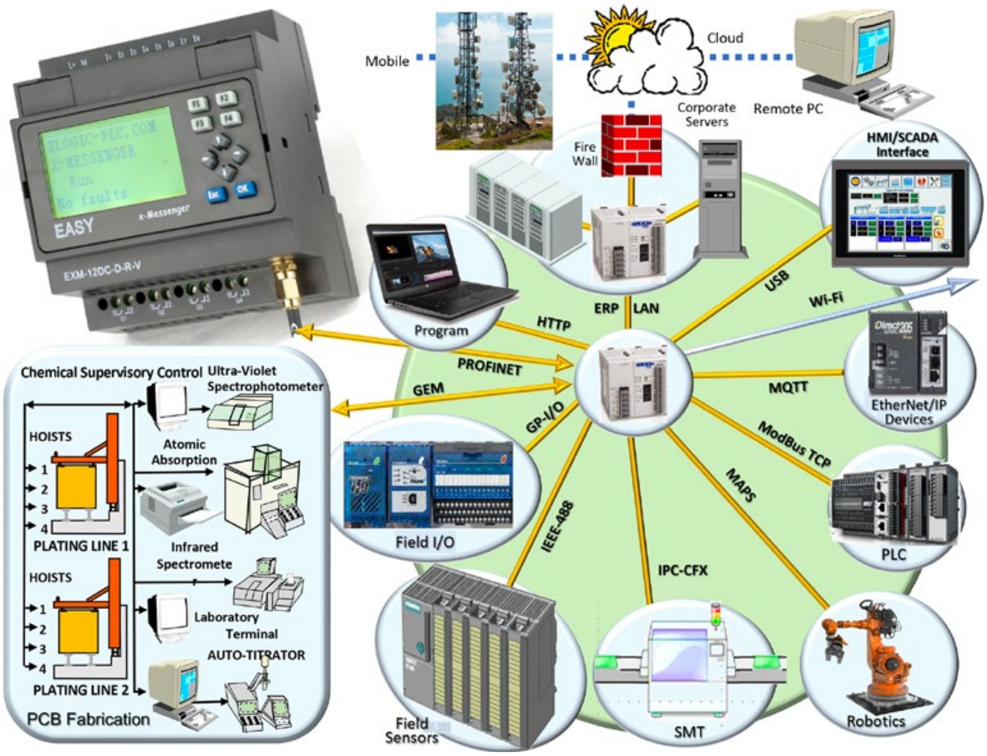


Figure 3: The electronics manufacturing factory floor basically has three standard protocols: PLCs, CFX, and SECS/GEM.

Smart Factory Protocols

When considering automation and data in the electronics manufacturing factory, three protocols stand out as de facto standards (Figure 3):

1. PLC protocols
2. IPC-CFX
3. SEMI SECS/GEM

PLC Protocols

Programmable logic controllers (PLC) came about in the 1960s and have steadily grown in use and popularity.

PLCs, like those produced by Siemens and Allen Bradley, have extensive networking capabilities. There are at least six to eight open, but proprietary, messaging and protocols used by PLCs, with the ModBus TCP

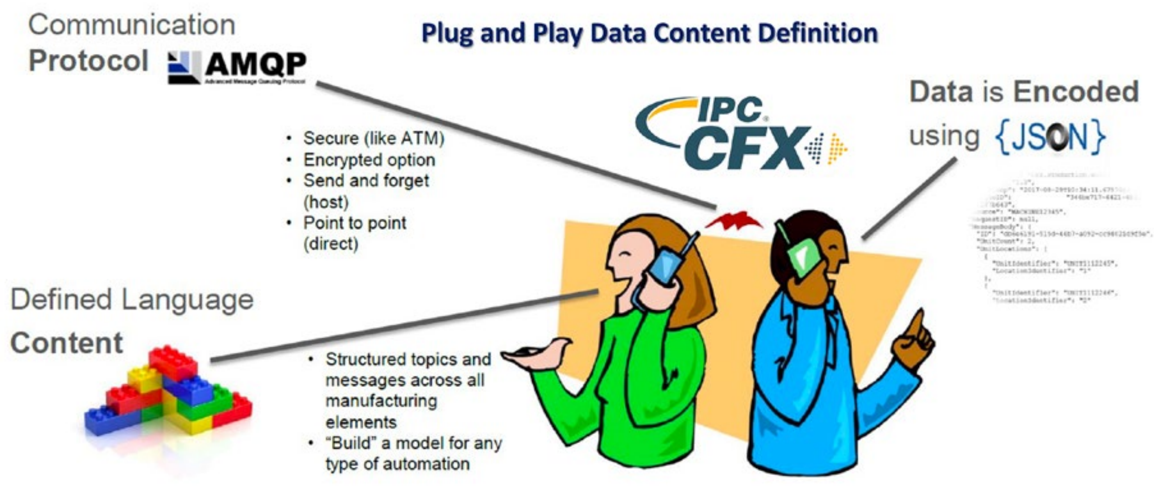


Figure 4: IPC-CFX is an open, free M2M electronic assembly protocol standard[2-3].

being the most popular and largest installed base. These are used in automation protocols as seen in Figure 4.

Four of the most popular protocols for PLCs are:

1. ModBus TCP
2. Profinet
3. OPC-UA
4. MAPS

IPC-CFX/HERMES

For electronics assembly, over 300 corporate IPC members came together to create the connected Factory Exchange (CFX) in 2018. The IPC-2591 is an open-source standard for "plug-and-play" connectivity for electronics assembly.

It establishes three critical elements for plug-and-play industrial IoT:

1. A message protocol using AMQP.
2. An encoding mechanism using JSON.
3. A specific content creation element-structured topics and messages.

These elements allow for the creation of automatic decision making, dashboard displays, alerts, and reports. Applications that improve productivity, efficiency, capacity planning, and quality while lowering costs can be seen in Figure 5. It allows the full traceability of components (IPC-1782) and feedback to design (IPC-2581).

Typical CFX topics and messages are shown in Figure 6. IPC has established the "CFX Message Submission Process," a methodology to add/edit new messages for the CFX standard, which allows the standard to grow and be applied by more machines and processes.

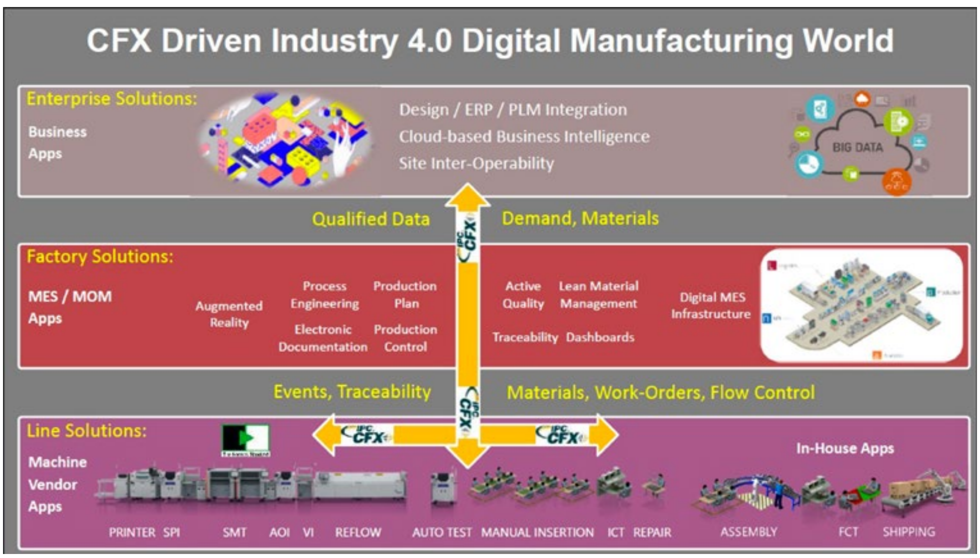


Figure 5: CFX drives Industry 4.0 digital integration for electronics assembly by connecting assembly to factory and enterprise solutions[3].

WORLD-CLASS TOOLS

Insulectro, the largest distributor in North America of materials used in the manufacture of printed circuit boards and printed electronics, provides game-changing precision cutting tools to our customers.

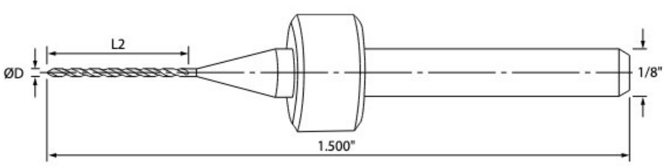
CALL 949.587.3200 FOR MORE INFORMATION

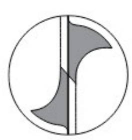
Kyocera designs and manufactures tight tolerance precision carbide cutting tools for PCB applications. Products include drills, routers, end mills, and specialized cutting tools ranging from: 0.05mm to 6.70mm diameters (0.0020" - 0.2638").

Drills, End Mills, Routers, Specialty Tools

Kyocera's renowned array of drills, routers, end mills, and specialty tools offer many benefits and advantages to customers for all their drilling and routing needs. Kyocera's tool reliability and design flexibility are key strengths of their products, along with a complete R&D facility in the US, new tool manufacturing capability, and local technical resources, all available to support customer needs.

REPOINTING will be a new service offered by Insulectro through Kyocera. The company has recently invested in automated, state-of-the-art equipment and all repointing will be done in Southern California.





4 Facet Point Geometry

INSULECTRO 20362 Windrow Drive, Lake Forest CA 92630 • 949.587.3200 • insulectro.com

There is even CFX messaging for hand soldering.

To facilitate adapting machines and applications, there are free software development kits (SDK) available for Windows, .Net, Linux, LabVIEW, JAVA, etc. Already, hundreds of machines have been adapted and demonstrated with native CFX. Figure 6 is an overview of the CFX SDK life cycle. The goal of the IPC committee is to facilitate a fully functioning Industry 4.0 Digital Manufacturing World.

Example (Figure 6)

The IPC-CFX standard allows inspection data (2) and (3) from devices to be uploaded to MEM software where compensation data (2) and correction data (2) are determined and downloaded to the screen printer and pick-and-place machines to improve quality and reduce downtime.

SEMI-SECS/GEM

The third standard protocol is SEMI's SECS/GEM standard. This standard was established in the 1980s and '90s by the semiconductor industry (SEMI) and has been continuously updated. There are over 900 English SEMI standards, with many more in Korean, Japanese, and Chinese. SEMI also has standards for other industries, including photovoltaic and liquid crystal display fabrication. The standards are open and non-proprietary. SEMI's documentation is useful to establish messages and responses for PCB fabrication protocols. Like IC fabrication, the PCB fabrication process is thermodynamic, so the IC fabrication model is very useful for PCB fab and is different from the kinematic PCB assembly model. It has been updated with current wireless networking and security and is a convenient model for additional PCB automation. The PCB fabrication standards are under development by the Taiwan Printed Circuit Association (TPCA); its model is shown in Figure 7.

SEMI has PCB fabrication and assembly advisory boards working to connect the entire electronics supply chain into one digital thread. Because of accessibility, originality, and security, SEMI is looking at "distributed ledger technologies" (blockchain) as a possible technology to include in its General Equipment Model (GEM-E30) protocol. Find the SEMI standards on its website[6].

Conclusion

The automation planning methodology is detailed in Automation and Advanced Procedures in PCB Fabrication[1]. By breaking down all work into time spent by a worker and by the machines for mechanization and systemization at various levels and classes, a plan can easily be prepared for new performance stages. The

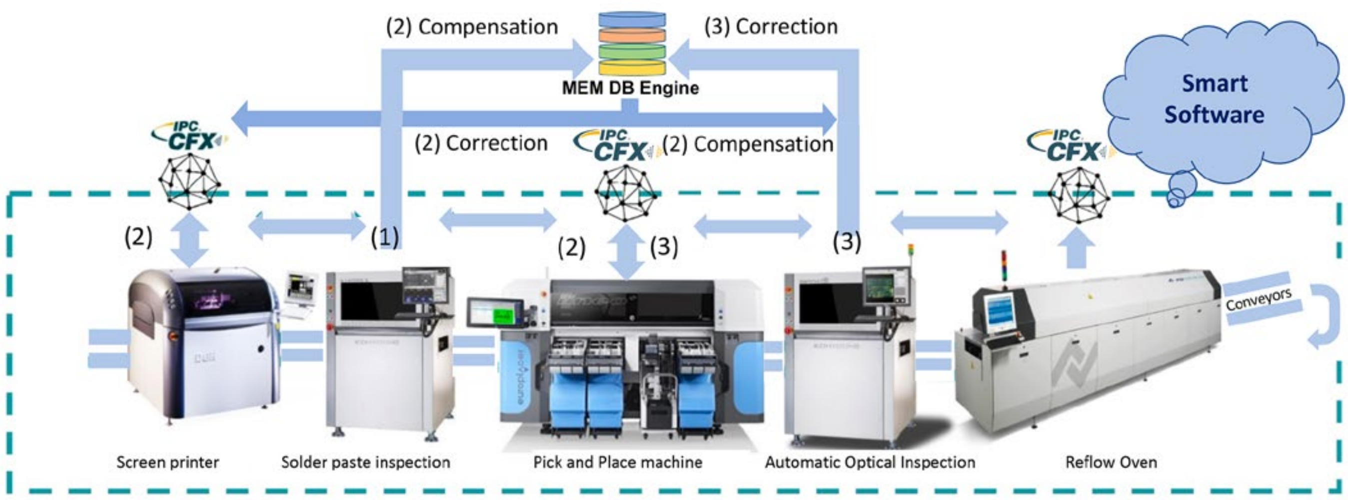


Figure 6: CFX enables assembly machines to talk to each other and pass important data up to management software for higher quality and productivity[4].

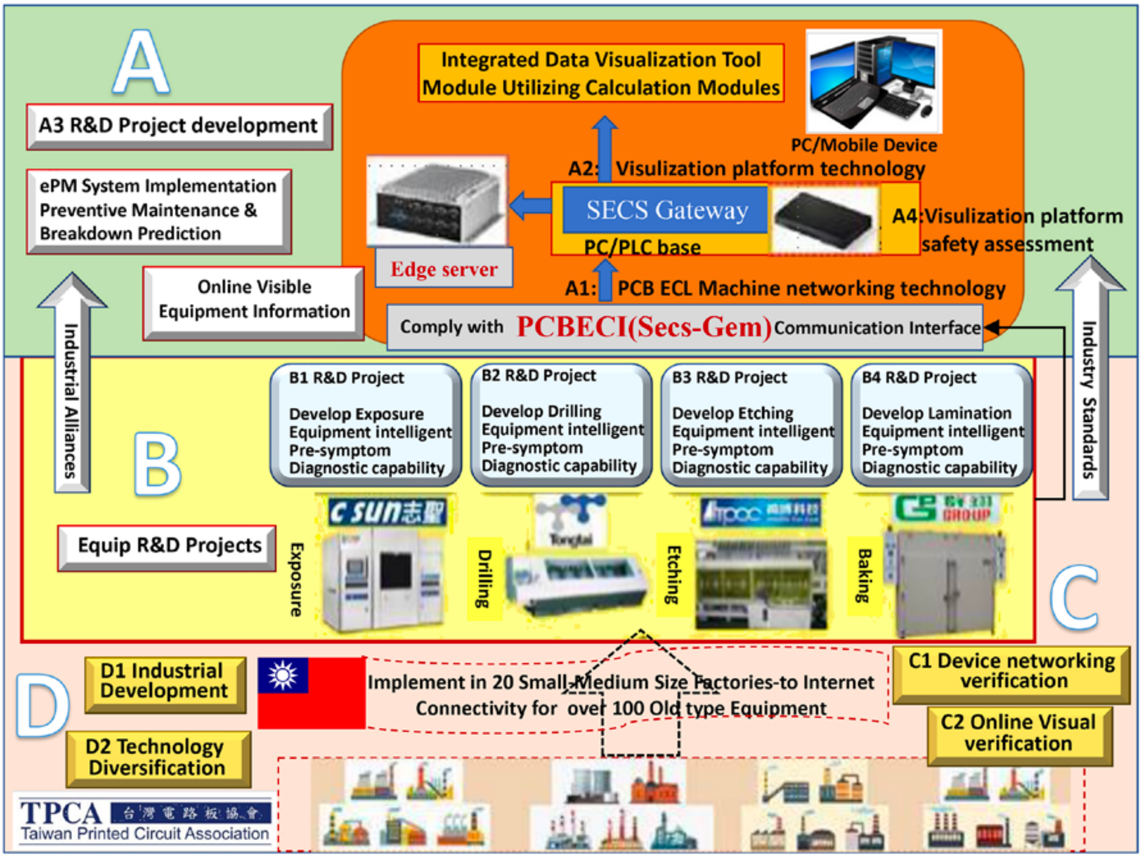


Figure 7: The PCB process protocol standard is being undertaken by TPCA for SEMI[5].

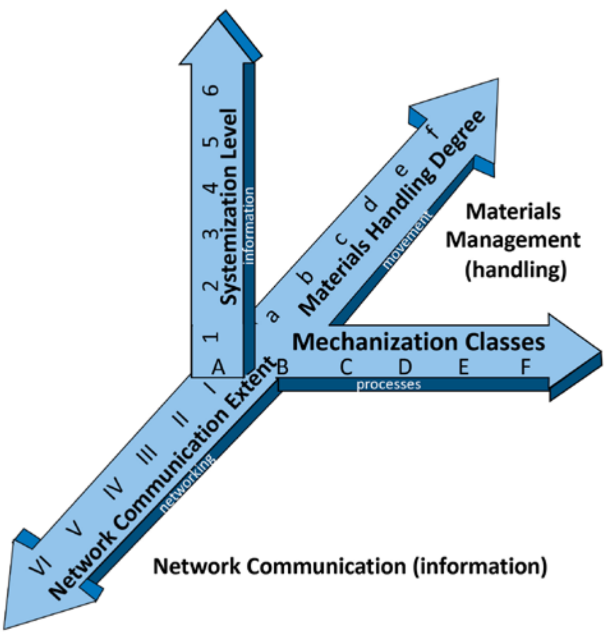
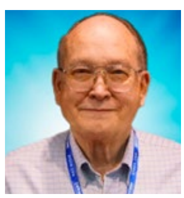


Figure 8: The "automation activities" are broken down into classes, levels, degree, and extents[1].

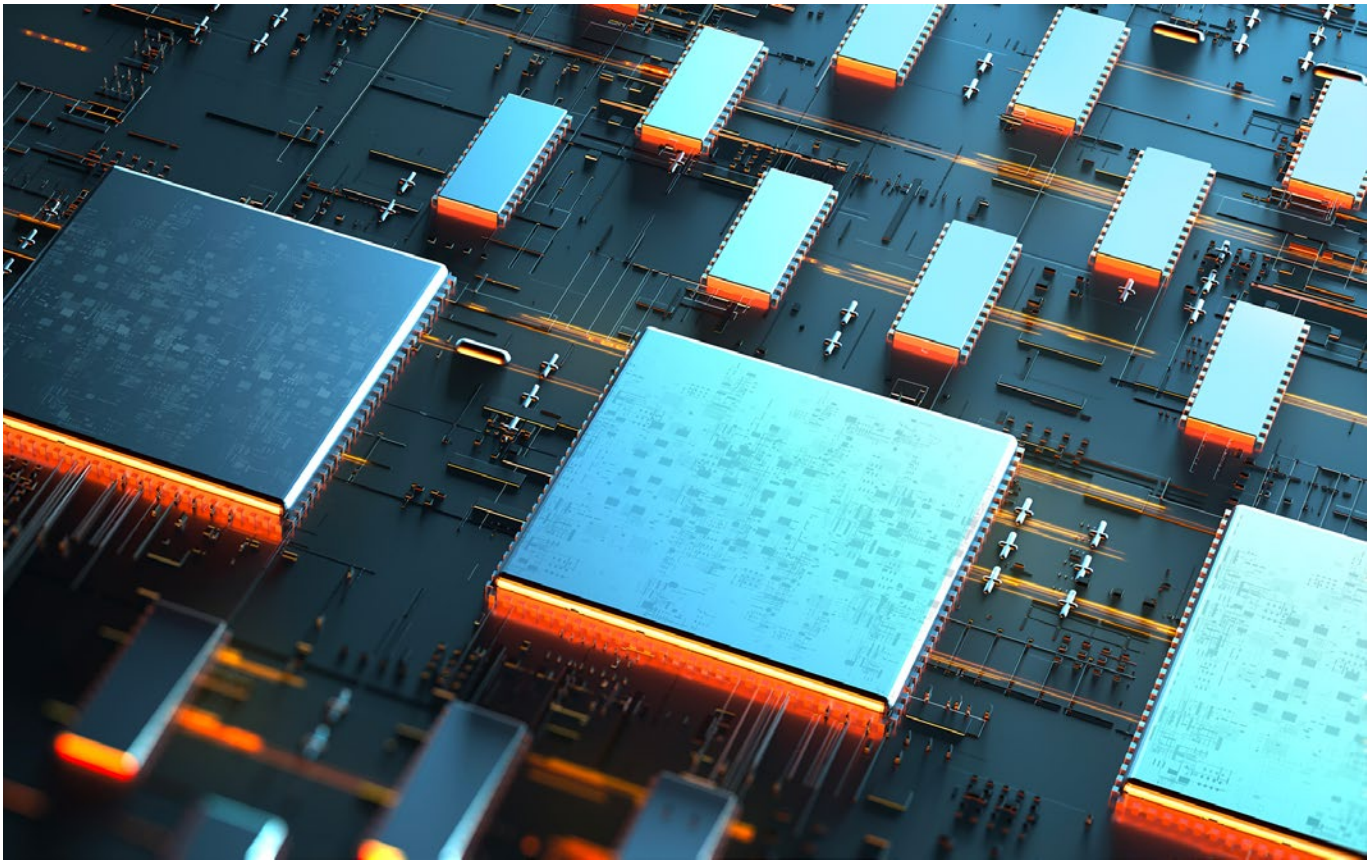
material handling of products from operation to operation (Figure 8) is benchmarked, as well as the networking of information. PCB007

References

1. *Automation and Advanced Procedures in PCB Fabrication,* by Happy Holden, June 2018.
2. "Building An AI Ready Culture," keynote address by Irene Petrick, SMTA eSmart Factory Conference, Detroit, 2019.
3. "IPC CFX: Plug and Play Equipment Messaging Supporting the Factory of the Future," IPC.org, 2022.
4. "The Smart Factory Program," at IPC APEX EXPO in San Diego, CA, 2022.
5. "SEMI SECS/GEM Presentation," translated from Chinese at the TPCA Conference in Taipei, Taiwan, November 2021.
6. SEMI website, www1.semi.org/standards.



Happy Holden has worked in printed circuit technology since 1970 with Hewlett-Packard, NanYa Westwood, Merix, Foxconn, and Gentex. He is currently a contributing technical editor with I-Connect007, and the author of *Automation and Advanced Procedures in PCB Fabrication,* and *24 Essential Skills for Engineers.* To read past



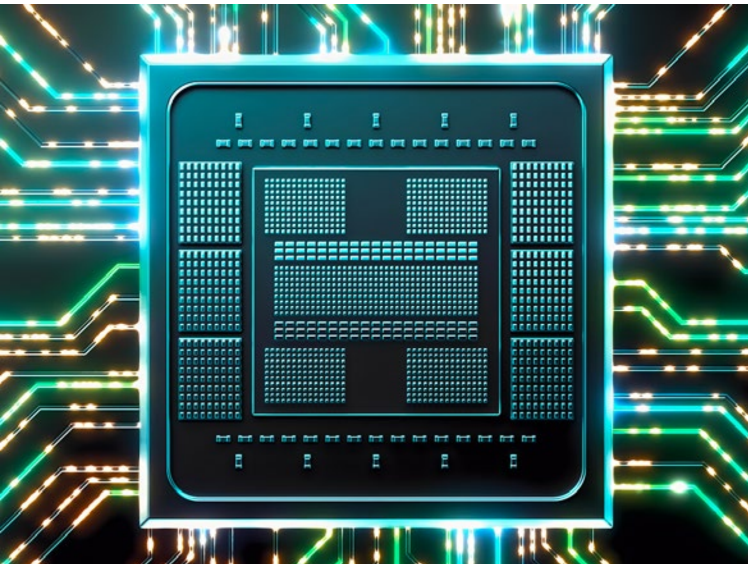
The Impact of Chip Packaging

Feature Article by Charles E. Bauer, Ph.D.
TECHLEAD CORPORATION

When talking about chip packaging impacts on substrates and electronic manufacturing services (EMS) providers, the focus mostly lies on large packages and very high I/O, fine pitch components; rightly so in most cases. However, several current packaging trends offer a new path forward to simplification and, thereby, cost reduction in both the printed wiring board (PWB) and EMS supply chains.

A handful of key technologies support these advances. Through silicon vias (TSV), while tracing their origins back to the invention of the transistor and found in a few supercomputers during the 1980s, really came onto the volume manufacturing scene between 2005 and 2010. Since that time, rapid advances in process control and yield led to very high-density memory implementations. TSV now proves a key enabler in the evolution of chiplet architectures.

The second key technology development came in the form of silicon and glass substrate development. Silicon substrates entered the scene in a significant manner during the 1990s but, until recently, proved too expensive for all but the most esoteric applications. The availability of old node fabrication equipment that flooded the market around 2008–10, opened the door to more reasonably priced Si substrate and provided an easy path to the current chiplet architecture, particularly for large IC OEMs. The advent of glass substrates, driven



by extensive research at the Georgia Tech Packaging Research Center, now provides very high routing capability comparable with silicon substrates at far lower cost. The compatibility between the coefficient of thermal expansion (CTE) of glass and Si chips makes for highly reliable, multichip assembly either in a chiplet or SiP application.

Finally, bonding and interconnection advances greatly facilitate successful assembly employing TSV and very high-density substrates. TechLead first developed and demonstrated nano bonding as a method of very high-density chip-to-chip interconnection at a 32-micron pitch in 2012. IBM Zurich continued this research from 2013 using nano copper for PWB assembly. At the University of Tokyo, Tadatomo Suga Sensei occupies the forefront of surface activation bonding technology, which now finds its place in various assembly configurations ranging from wafer-to-wafer bonding to chiplet assembly.

Consider the implications of the transition from laboratory curiosity to mainstream manufacturing capability of TSV and glass/silicon package substrates. Add the emergence of innovative chip connection technologies, such as nano bonding and surface activation bonding to complement traditional reflow assembly, and the possibilities increase exponentially. Together, these technologies enable chiplet architecture as well as expanding SiP (system in package) options such as mixed-chip technology.

Chiplets allow more complex component designs from the semiconductor houses that incorporate the optimum IC fabrication techniques for each piece of their application. For example, by separating logic, memory, and power distribution into individual chiplets, the designer leverages both layout and fabrication technology to maximize miniaturization as well as performance. Additional gains in thermal management capability, combined with the ultra-high routing density enabled by the combination of TSV and the extremely fine line/space capabilities of glass/Si substrates, reduces the total pin count (and generally thereby I/O density) seen by the PWB. Clearly, this greatly simplifies PWB assembly and therefore increases yields.

Chiplets also facilitate a "gate array" mentality for producing enhanced functionality in these components. Rather than restriction to in-house chiplets, the component designer gains access to the best available design and manufacturing for each piece of their component to further optimize overall functionality and performance. Not only are internal resource requirements (e.g., design, fabrication, test, etc.) dramatically reduced, but ever-critical time to market reduces dramatically as well. Certainly, the matter of known good die (KGD) remains a barrier, but significant progress during the past three decades reduces this concern to a manageable level in most cases. Standardization efforts within the industry seek to enable and stabilize these opportunities.

So, what role does SiP play, the parent of chiplet architecture? Many applications demand mixed device types such as GaAs, SiC, InP, etc., to provide more specialized functionality that remains difficult to implement with a chiplet design. SiP remains the approach of choice for more complex and/or unique applications where specialized requirements

or functionality do not warrant the complex infrastructure investment required for chiplet designs. SiP also serves as a sort of prototyping platform for future chiplet component development. Fine tuning of an application in a SiP can point the way for a successful chiplet implementation in a future generation of products.

Fine tuning of an application in a SiP can point the way for a successful chiplet implementation in a future generation of products.

Viewing SiP as a chiplet precursor, however, belies its major role in and of itself. Appropriate leveraging of the same technologies that enable chiplet architectures extends the applicability of SiP in many different directions and arenas. By using glass substrates, SiP takes advantage of the same routing density advantages leading to improved thermal management capability, lower I/O counts, and high I/O pitch, again resulting in simplified assembly and higher yields at the PWB assembly level.

Ideally suited to rapid creation of customized applications using essentially off-the-shelf chip designs from any fabrication technology and/or supplier, SiP remains the champion in terms of time to market, as well as rapid revision, e.g., a memory shrink implementation for SiP may not even require a substrate re-layout, whereas for a chiplet architecture this remains a significant challenge, to say the least.

Additional SiP advantages include diversity of materials options for both the SiP substrate and the die attachment/interconnection. Down-hole applications, for instance, can employ SiC device technologies on high-temperature substrates bonded with AuSi or AuSn, as appropriate. For implantable medical products, SiP can incorporate substantial passive componentry to frequently allow complete implementation of the electronic functionality for the product in a single SiP configuration.

So, what implications arise from these advances, especially for the PWB and EMS sectors of the industry? The answer, of course, is "it depends." For manufacturers of larger PWBs, the implications are likely lower costs, higher yields, and smaller value-add due to larger geometries (lines/spaces), and fewer layers required by consolidation of circuitry within the package assemblies. The implications are similar for EMS providers working with these boards. However, the EMS folks may retain some value-add due to handling requirements for these more valuable and sensitive components. More specialized segments of the supply chain, such as package substrate suppliers and OSATs (outsourced semiconductor assembly and test), benefit from increased demand for their more specialized capabilities—and at increased volumes to boot.

While PWB assemblies (the grandparent of SiP) and hybrids (the grandparent of chiplets) continue to thrive beyond their prognosticated demise, SiP- and chiplet-based components will revolutionize electronic products in the ways described here as well as many not yet foreseen. Expect accelerated growth in a wide range of applications, especially high-reliability arenas such as IoT, automotive, environmental monitoring, security, mobile communications and military/aerospace. Each of these areas presents unique challenges. PCB007

Charles (Chuck) Bauer is senior managing director and owner at TechLead Corporation.

A Tale of Two Towers

The New Chapter

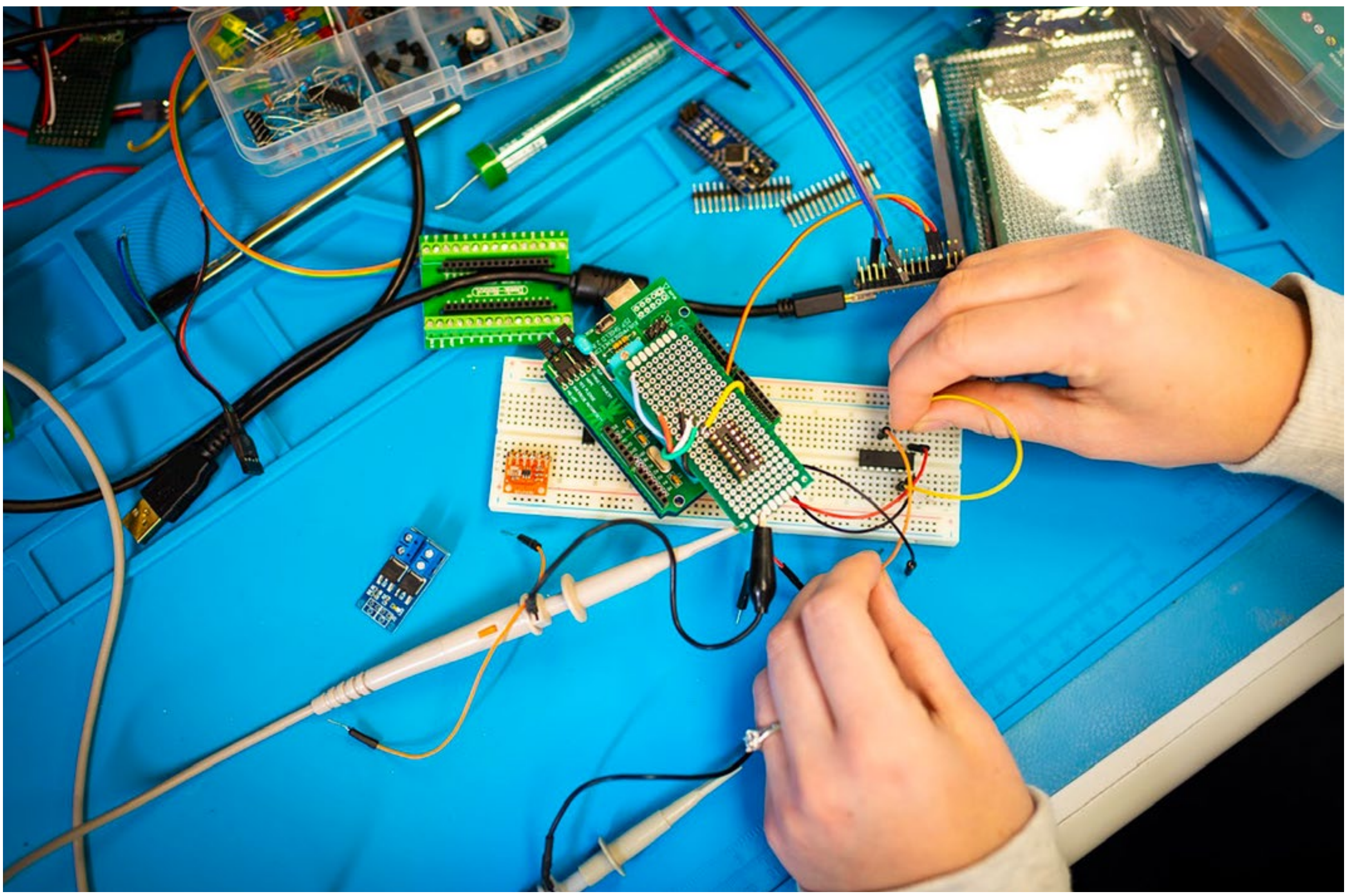
by **Paige Fiet**, TTM-LOGAN

Have you ever played the game where you and your team try to build the tallest tower out of marshmallows and dry spaghetti (and sometimes tape) within a time limit? If you've played this fun game before, you know it's meant to test problem-solving skills and build teamwork.

But what if I told you that you've been playing this game all wrong?

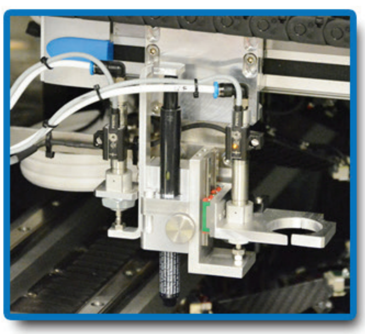
I assume that, if you played this game today, your team would start by brainstorming how to build the best base, as well as the strongest and tallest tower, out of the available materials. Your team would likely spend 50% to 70% of the time limit on brainstorming and the last 30% to 50% building your tower. In contrast, a group of kids given the same challenge will start building their tower right away; when their tower falls, they will start over with a new design. A group of kids will repeatedly test varying prototypes until they achieve the tallest design. They see what most adults don't when the test begins: There is no right answer.

Why do kids tend to succeed at this game better than adults with more life experience? I think it's because we don't work that problem-



Unrivaled Test Speed with Full Automation

Introducing the newly designed atg A9a with 8 test probes and a new high speed “lights out” automation for unrivaled throughput.



Highlights:

- Small footprint (6 square meters)
- Dual shuttle pick & place automation
- High accuracy combined with high test speed
- Pen or label marking option

Watch video

Get more info

atg

LUTHER & MAELZER

MYCRONIC

atg Luther & Maelzer GmbH
Zum Schlag 3 • 97877 Wertheim • Germany
Phone +49-9342-291-0 • Fax +49-9342-395 10
sales@atg-lm.com • www.atg-lm.com

solving "muscle;" anymore. It is in a child's nature, on the other hand, to constantly assess and test boundaries, whether they are learning to walk and talk, or are making friends at school. Adults, especially new college graduates, are conditioned through years of schooling that there is typically one "right" answer to a given question. What is 8 + 8? The answer will always be 16. What is the powerhouse of the cell? It's the mitochondria, of course. After 12 years of schooling (or more), rote learning effectively forces our problem-solving into hibernation deep in our brains.

I always hear from new engineering graduates that the workforce is not what they expected it to be; graduates often express how unprepared they felt at their first internship. Is it because the engineering skills they learned in school failed them, or is it because they fail to see those skills as one of many tools in their skills toolbox? I'll admit that my first internships—and my first few months at my first full-time job—stretched my problem-solving skills as well. Instead of a calculus problem with one right answer that I could solve in 20 minutes, I was faced with problems that did not have a solution manual. I had to think about these problems for days or even weeks to come up with a solution; even then, that sense of immediate success, so familiar to me from my experiences in academia, was missing. I had to learn that my education was just another tool in a larger toolbox of problem-solving skills—ones that I needed to learn about and develop over time.

If a college education is a single "tool," what other tools exist? DOEs, the five whys technique, the problem-definition process, and design sprints are just some of the tools I had to add to my repertoire. Just like a hammer cannot screw in a screw, statistics will not solve every workplace problem. I had to go beyond my education and the quick problem-solving skills I'd relied on in calculus and basic chemistry. Naturally, this learning process was full of growing pains. Each time I tried a new skill, I

Woodworking example.

was met with failure. Again and again. It was frustrating. I had spent the past 15 years solving problems with one right answer. I never really had to learn how to problem-solve like an engineer. Unfortunately, I believe many other students are in the same boat—they haven't had to flex those mental muscles or solve problems that last beyond a class period.

Where do those students go from here? I would argue that these skills can be built by engaging in extra-curriculars or joining clubs. My college had a "Concrete Canoe" club, in which students were tasked with building a canoe out of concrete that could both float in water and hold two people in a paddling race. Other clubs had students use 3D printers to create chess boards and matching pieces. These students had to visualize how each piece would be created in a CAM program, and they had to verify that all the parts would fit together properly. Personally, I took pottery classes and learned basic woodworking. Such hobbies allow us to grow our skills and thought processes outside of the classroom; they aid in

spatial visualization and to see how components move together to create a whole. These activities are no more important than a college education; rather, they expand on skills students have learned in class and help diversify our thinking processes.

Schools can and should offer these types of activities but, for now, it is up to students to seek out these opportunities so that they can expand their problem-solving skills. It is essential for engineers to be able to think outside of the box—to test prototype after prototype until a solution is found. Adults playing the marshmallow game would do well to extend their approach to problem-solving beyond the "right answer" way of thinking. Through practice and time, we can better prepare ourselves for the challenges that lie ahead in both our industry and our personal lives. PCB007

Resources

1. "Build a tower, build a team," by Tom Wujec at TED2010, TED.com, Feb. 2010.

Paige Fiet is a process engineer at TTM-Logan. To read past columns, click here.

The Nuts and Bolts of Advanced Packaging

An Interview with Matt Kelly

The I-Connect007 Editorial Team asked IPC Chief Technologist Matt Kelly: Will you help us understand what advanced packaging means? This informative conversation touched on topics for both assembly and board fabrication. In the January issue of *SMT007 Magazine,* Matt helps define not only what advanced packaging is, but the approach EMS companies must take when looking ahead. Think it's about just adding some new equipment and software? Think again. There are logistics, onboarding, and so much more.

Nolan Johnson: Matt, I was on the exhibition floor at a technical conference recently and heard a lot of questions about advanced packaging: What is it, how does it apply, what does it mean to EMS providers, etc.? Would you help to define and provide a framework about advanced packaging?

Matt Kelly: There are two terms to define. An advanced package is an electronic component; it's as simple as that. It has a few elements—it's comprised of a semiconductor chip (typically silicon) and an interposer and/or substrate—followed by interconnection and assembly of the component. Advanced packaging is the process by which these elements are integrated, assembled, and tested. Advanced packages represent a very specific class of electronic components called active devices. They are called active devices because they contain silicon that provides compute, memory, or other logical device functions. Advanced packaging is critical because the combination of performance, reliability, cost, and functionality that future consumers are demanding can only be met by integrating silicon chips through an advanced packaging process.

To read the entire interview in *SMT007 magazine,* click here.

Interview by Nolan Johnson
I-CONNECT007

Nolan Johnson recently met with Alun Morgan, technology ambassador at Ventec, and Ventec COO Mark Goodwin to discusses the industry's determination to cling to outdated processes and standards, and some potential consequences. To maintain efficiency and keep pace with the market's newest entries in Asia, Alun and Mark believe that legacy companies in the West must be open to challenging conversations that will require questioning old practices and revising those practices toward sustainability.

As Alun points out, everyone says they want change, but no one wants to lead the way.

Nolan Johnson: Would you say that there's an opportunity for innovation right now? Your options are to either stay inside old niches with low margins, or to start looking for new ways to do things. In another conversation, for example, you alluded to thermal management coatings as potential replacements for heat sinks. What other ways can you see this done differently?

Mark Goodwin: I don't have a clear answer to that, but I think we will start seeing management of scarce resources enter the supply chain discussion. People need to consider what they truly need for the performance they're looking for; there is no doubt in my mind there's a huge amount of unnecessary over-engineering happening. For example, you must start considering the scope for using a half-ounce copper foil when you're currently using one ounce, or one ounce where you're using two-ounce—those are the shifts in scope we need to be anticipating.

Alun Morgan: That's right. This is an opportunity to return to the point we've made before. It's critical to understand the end use. You need a clear understanding of both what the customers need and what they really want, then you need to link it all together. Mark, you and I have spent our careers with companies who often don't share information with us, which makes it impossible to offer them anything substantial; on the other hand, when companies share information with us, we can get them access to a fantastic supply chain offering.

Goodwin: Yes, and we've done lots of business over many years. By way of example, let's talk about an issue that's been a bugbear of ours for years. Why is laminate 1.6 mm thick? It's a

waste of glass fabric and of resin. In the old days, it had to be 1.6 mm because it needed to fit into an edge connector. When was the last time you saw an edge connector? Why is it still 1.6 mm thick? A double-sided plated through-hole board of 1.0 mm is rigid enough to support the components. Why not take out two, three, even four pieces of glass fabric?


Alun Morgan

Morgan: It comes to the need. What is the requirement? The user doesn't always know what he needs or what he can get away with. He just says, "Well, it's always been that way." You see this mindset all the time in so many different industries. The first step in designing a solution for someone is understanding what they need. Don't ask them what they need—most of the time, they don't know. They really don't, so you must ask the right questions.

My son's involved in UX—user experience—and so much of that is relevant here. He walks through that process with users. He calls it a "design safari"—pretend you're going on a safari where you must stop at each new thing, think it through, and ask, "Why do we do that?" Until you've done that, you don't know what the customer needs, and they don't know either. You must go through each stage. Once you've identified the real need, you can develop an efficient method to deliver that need.

We've seen so much waste in pursuing this, haven't we, Mark? On a few occasions, we've nailed it down and saved huge amounts of resources. If you can get everyone to be open and have that discussion, get them to genuinely share with you, you can make big gains.

Goodwin: There must be a willingness and openness to move forward, but all too often we've discovered there are too many closed minds in this business.

Morgan: Some people will design something and never change it. The design might have been right when they first did it, but then they don't change or review it, in some cases, for 20 years. This is crazy.

Johnson: We've come to a place where pricing and sustainability are such important factors because we're using copper which is in tremendous demand.

Morgan: Cost—not price—is the issue, though. We can work on the cost.

Johnson: But isn't that the motivating factor? Isn't that where you can turn around and say, "You know, we can save you money if you modify the spec to reduce the resource?"

Morgan: You would have thought so.

Goodwin: I usually hear something like, "That's great, Mark. We'll take the price, but we don't want to do the work involved with the change."

I've been in the circuit board industry since 1983 and in laminates since 1990. In my experience, there is a resistance to change. They want the savings, but they don't want to do the work. They don't want to commit to making changes. The automotive business is particularly focused on cost reduction, but also highly resistant to change. We are running out of road to get one without the other.

Morgan: We all have to work together to make this happen.

Goodwin: I'm not pointing the finger at the printed circuit board market here, either. Usually, they're constrained by somebody upstream or downstream of them. The folks telling them what to do are so far removed from how a printed circuit board or laminate is made. They have no idea what they are or aren't restricting.

Johnson: How do we get out of this?

Morgan: I want to say "education," but as important as that is, the reality is we're operating within the market. The market seems to be self-regulating, so those who are inefficient will end up being uncompetitive and will lose their business. That's the reality.

Mark Goodwin

Goodwin: What's that great presentation slide you always show about change, where people are standing on edge of the cliff?

Morgan: That slide is quite interesting. You've got a guy on a platform saying, "Who wants change?" All the hands go up, but then he asks, "Who wants to change?" Only one hand goes up. The guy presses on: "Who wants to lead the change?" At that point, the audience runs off, and that's the reality. Someone says, "We need to pay more tax," and the answer is always, "Yeah, everybody else but me should pay more tax." That's not going to cut it. We all have to do our part if we want things to change.

Sometimes I step back and reflect on how our business has evolved over the years. Back in the '50s, we had every kind of sheet size imaginable. We had all kinds of stuff going on. We were efficient because there was no other choice in those days. The reality is, in the West, we've continued with a lot of these old practices even though so many new options are available.

For example, Western laminators probably have 10 or 20 standard laminate sizes, three or four different widths of glass fabric. You go to Asia, what have you got, Mark?

Goodwin: A 50-inch width.

Morgan: And two sheet sizes. In Asia, they're efficient from the beginning. We still hold onto the inefficiencies of the old days, and we have yet to fix them.

Goodwin: The old U.S. sheet size was 36" x 48". Depending on which way around or which glass width you use to produce your prepreg, you can have 20% more or 20% less square meter output from your treater.

Morgan: Even more than 20%, by the way—as much as 30%. It's a massive change, and that leads to a better market.

Goodwin: The equipment costs are the same, the processing running costs are the same. It's just more output through better equipment utilization, so real cost benefit.

Morgan: The only reason it's done that way is because in those days, you couldn't buy glass wider than 37 inches. That was it. There was nothing available. Now, you can easily and reliably buy 50-inch.

Goodwin: For the United States, we still have to make narrow widths. We do still treat narrow width fabric because some people will not change the warp direction on their 18" x 24" polyimide panels. This, by the way, is a story that's over 30 years old.

We were trying to drive this change in 1990, swapping warp and weft around, to maximize machine utilization for us and the glass weavers, and that job is still not 100% done.

Johnson: This is something that really goes to the OEM designer, doesn't it?

Morgan: Yes, but it depends where you are in the chain. Commoditization has occurred in a lot of our sectors over the years, and if you're in a commodity business, you need to be efficient. You need to fix these things. You can get away with this for years when you're specialized, but over time, everything becomes commoditized. Even products that you feel were "specialty" at the time end up commoditized. If you don't make those changes fast enough, you lose out to somebody who will make those changes.

We're asking people to think about these things, to look for and actually consider the most efficient solution.

Goodwin: We know that change takes time—it never happens as fast as you'd like. But if you don't start, it never happens at all.

Morgan: The solution is not to say to people at Ventec, "Please hold more stock for me because of the ongoing logistics problem." That's not a solution—that's a stop-gap measure. We need to understand the demand pattern properly. I've reached this step many times with many different customers; it's a big step for many. Some commit, and do it, and do it very successfully.

If they're like, "Just put it on the table and we'll discuss it properly," then we can get somewhere, but this is a conversation we need to keep having. Who makes these changes? Asian producers—because they think fresh and they are fresh. That kind of thinking leads to proper solutions.

Johnson: What would Ventec's portfolio of products look like if you could solve this conundrum; if you could make changes to materials, and get people to specify?

Goodwin: Starting with the scarcity of raw materials, I won't provide two-, three-, and even six-ounce copper foil on a commodity FR-4 when I've got high demand for high-end IMS materials, and high demand for military and aerospace polyimide that requires heavy coppers. I will put those raw materials on my niche specialty products.

Morgan: We'd reserve those for flagship products. Our operations in Asia are pretty optimized because we're supplying a market that understands that. The issue occurs when we're working with legacy businesses. It's very hard to find folks willing to change.

Goodwin: Interestingly, the world thinks that polyimide is a U.S. business. Yes, polyimide in circuit boards is still a very big business in the U.S., but of the five major suppliers of polyimide in the world—Ventec, AGC Nelco, Isola, EMC/Arlon and Hitachi, whichever way you want to call it—four of those five are Taiwanese- or Japanese-owned. The other is American-owned, but its most recent U.S. factory has no treaters, because you can't get environmental permits for treaters—no dirty processes in America anymore.

Morgan: That's a big Asian footprint.

Goodwin: What's American about the polyimide business, if only one of the five suppliers is American-owned—but has no treaters in its newest U.S. factory? It's predominantly an Asian owned business now, and one in that group of five became Taiwanese-owned recently; it just started production of its polyimide in Taiwan.

Morgan: It's very surprising.

Goodwin: They have a product running on a treater in Taiwan. Well, that's great; it's good for the business. But the production has got to be qualified by PCB manufacturers and OEMs, and if the doors are opening for qualification of a new production, they should be open to changing to a more cost- and resource-efficient warp direction and exchange 24" x 18" for 18" x 24".

Johnson: This industry will need to ask itself some hard questions, and we covered quite a few of them here. Gentlemen, always a pleasure speaking with you.

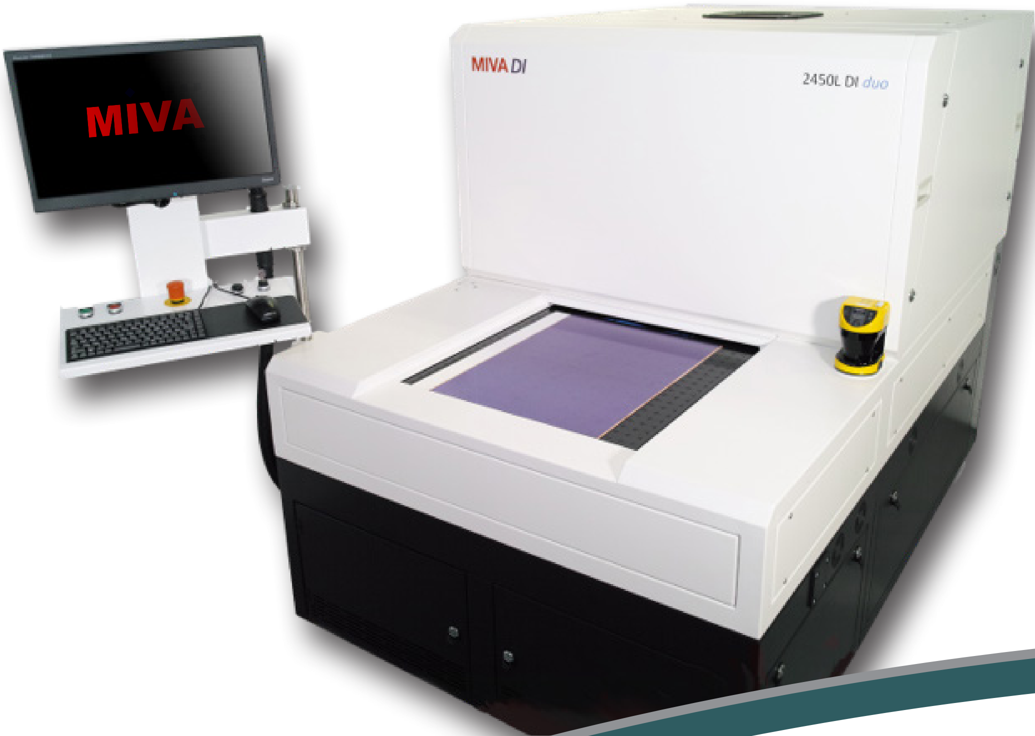
Morgan: Any time at all, Nolan. Great talking with you. **PCB007**

Download Ventec's latest book, *The Printed Circuit Assembler's Guide to Thermal Management with Insulated Metal Substrates, Vol. 2.*

MivaTek Global

APEX EXPO IPC 2023

Come See us! Booth 647



2400NG - Dual Tray Direct Imager

- NextGen™ now provide 30, 15 or 6μ features with dry film.
- DART™ exclusively permits automated precision feature size control.

Standard Features

- NextGen Light Engine Feature Sizes: 6μ,15μ,30μ
- Quad-wave LED DLP: 360, 375, 390, and 405nm
- Worldwide DART™ DLP Patents Issued & Pending
- Panel Sizes: 24” x 30” (up to 42” x 60”)
- Low Operating Costs, Flexible US Based Support
- Automation compatible with third party sources
- Over 60 Machines in North America

Applications

- PCB: IL, OL, SM
- Micro: 1μ features
- Chemical Milling
- Reel to Reel
- Glass Tool
- Electroforming

DART
Digitally Adaptive Rasterization Technology

DART™ permits improved on the fly scaling and feature size control. The result: increased technical capabilities from the existing equipment set.

NextGen

NextGen™ light engine technology increases throughput and imaging resolution, but the biggest feature is the ability to control feature size with DART™

MivaTek Global, LLC, 6 Dickinson Drive, Suite 218, Chadds Ford, PA 19317 • Website: www.MivaTek.Global
Contact: Brendan Hogan • M (610) 620-3795 • b.hogan@MivaTek.Global

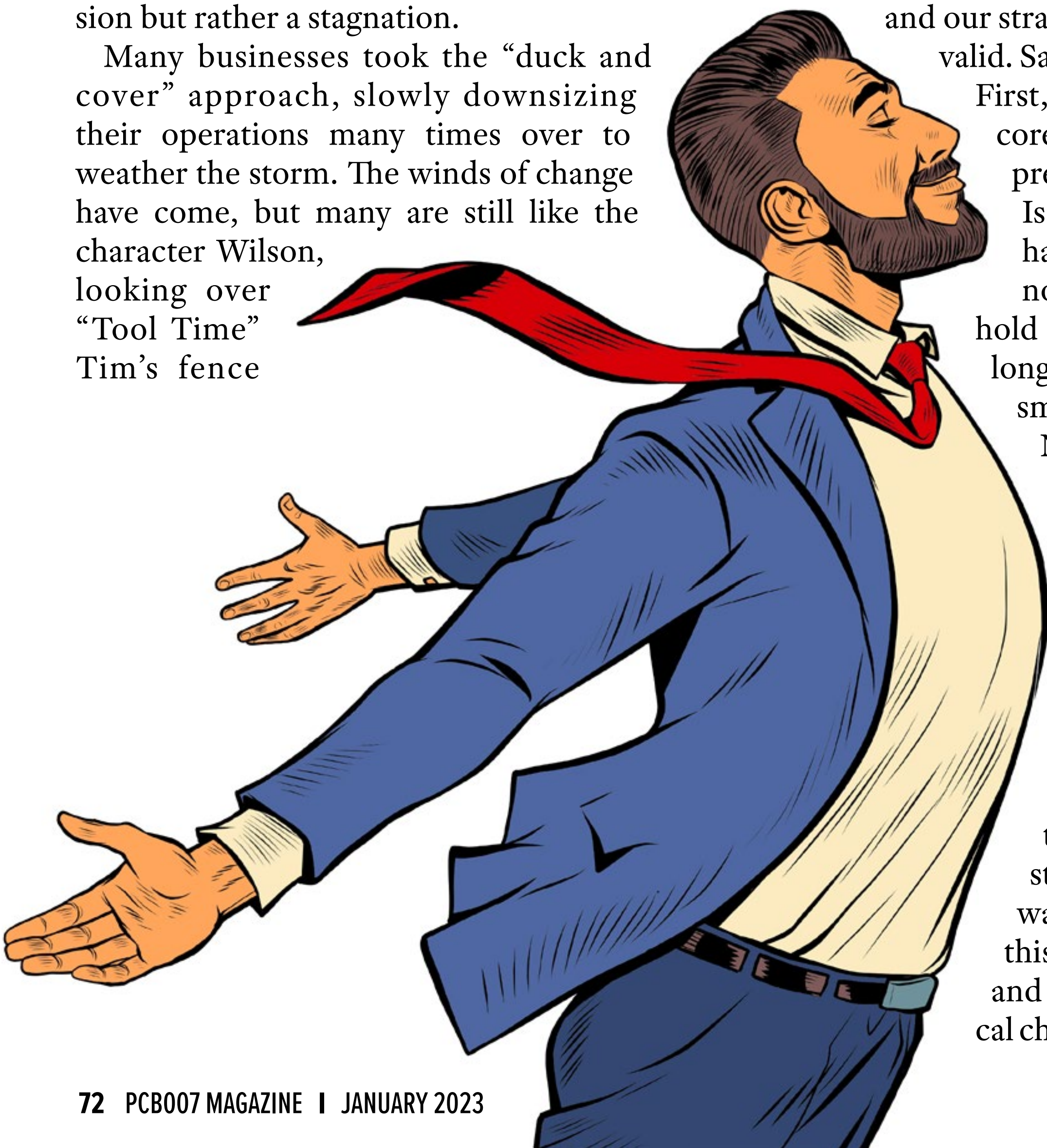
Turning Into the Wind

Testing Todd

by Todd Kolmodin, GARDIEN SERVICES USA

The last three years have been a challenge. If it wasn't the "Rona," aka COVID-19, it was the circus of shenanigans back in Washington, neither of which have been pleasant. So, it's not hard to figure out why we are all in this current situation. maybe we're not quite yet in a recession but rather a stagnation.

Many businesses took the "duck and cover" approach, slowly downsizing their operations many times over to weather the storm. The winds of change have come, but many are still like the character Wilson, looking over "Tool Time" Tim's fence to see what he will do. That is keeping us stalled out. It's time to go back to our sheds and sharpen the saw.



Now, what do I mean by this? Things may never again be the same as they were in 2019. How we did things, our market share, and our strategies are likely no longer valid. Safe to say, we must rebuild.

First, we must examine our core disciplines. Are those previous targets still valid? Is the niche we thought we had still there? Likely, but not as we remember. Don't hold on to something that no longer works. Are your teams smaller? Is that a problem? Not necessarily. These are your most important employees; they have weathered the hardship along with you. It's time to rethink the business.

Maybe it's time to redefine your niche. Strong skills come to a team that stands behind strong leadership and forward thinking. Sometimes this requires stepping back and restarting from a historical checkpoint, back when pro-

duction and output were strong. Maybe that older approach isn't the way you were doing things when the 2020 storms hit, but that was still a time of success and solid growth. Well, today's consumers, like military and aerospace, are still out there. If the market went soft for you, there is a reason. Maybe it's just too expensive for you to compete in that market and your margins can't handle it.

Here is the hard decision part: Should you stay with the losing venture, or let it go so you can redefine your core niche and go 110% at it? None of us can do all things all the time. If you're trying to do what Tim does on the table saw with a handheld skill saw, you won't succeed.

Our problem right now is still the "wait and see" attitude: "Let's watch and see what happens." Well? We've been doing that for three years now. Supply chains are recovering, gas prices are falling, and customer demand is not going to diminish.

Consumers are frustrated as products are failing to maintain inventory levels while demand remains high. However, the PCB industry has softened, with overall square footage down in many sectors, including consumer electronics. We need to get back to building. We have strong teams out there and manufacturers large and small that just need to sharpen the saw, rethink their core niche, and redeploy to do whatever they decide is best for them in this re-emerging market. Create that iron core discipline and execute it. But remember: Don't bite off more than you can provide. Create that quality product, deliver it on time, and provide your customers with the kind of service that will make them a lifetime partner.

Once your core disciplines are solid and your tools are sharp again, turn that carrier into the wind and face the battle head on. Stop waiting to see what Tim is going to do on the other side of the fence—you've got your own map to guide you to the next horizon. **PCB007**

Todd Kolmodin is VP of quality for Gardien Services USA and an expert in electrical test and reliability issues. To read past columns, click here.

MKS' Atotech: Chemically Connecting the Industry

Feature Interview by Pete Starkey
I-CONNECT007

Pete Starkey gets the rundown from Dr. Tobias Helbich, global product manager at MKS' Atotech, on how specialty chemical technologies are poised to reshape the global PCB and advanced packaging industries. Through a comprehensive product line-up and years of industry expertise in the surface-finishing solutions space, MKS' Atotech has successfully cultivated both a leading marketing position and a top-notch reputation in facilitating critical processes like electrochemical and electroless deposition that are so integral to advanced electronic devices and innovation in this field. With rapid advances in the electric vehicle sector and many opportunities on the horizon in the field of advanced packaging, surfaces—and the future—are looking bright.

Pete Starkey: I'm delighted to have the opportunity to speak with Dr. Tobias Helbich at MKS' Atotech booth here at electronica. Tobias, thank you for making us so welcome. It's great to meet you.

Tobias Helbich: Thank you very much, Pete, for coming to our booth and for giving us the chance to talk to I-Connect007. I'm also very excited to speak with you here in Munich at electronica.

Starkey: Tobias, could we begin with a summary of what technology areas you cover?

Helbich: Sure. Let me start with the bigger picture: Atotech, a brand of MKS has various products that cover a very wide field, specializing in surface metallization or, even broader, in surface treatment.

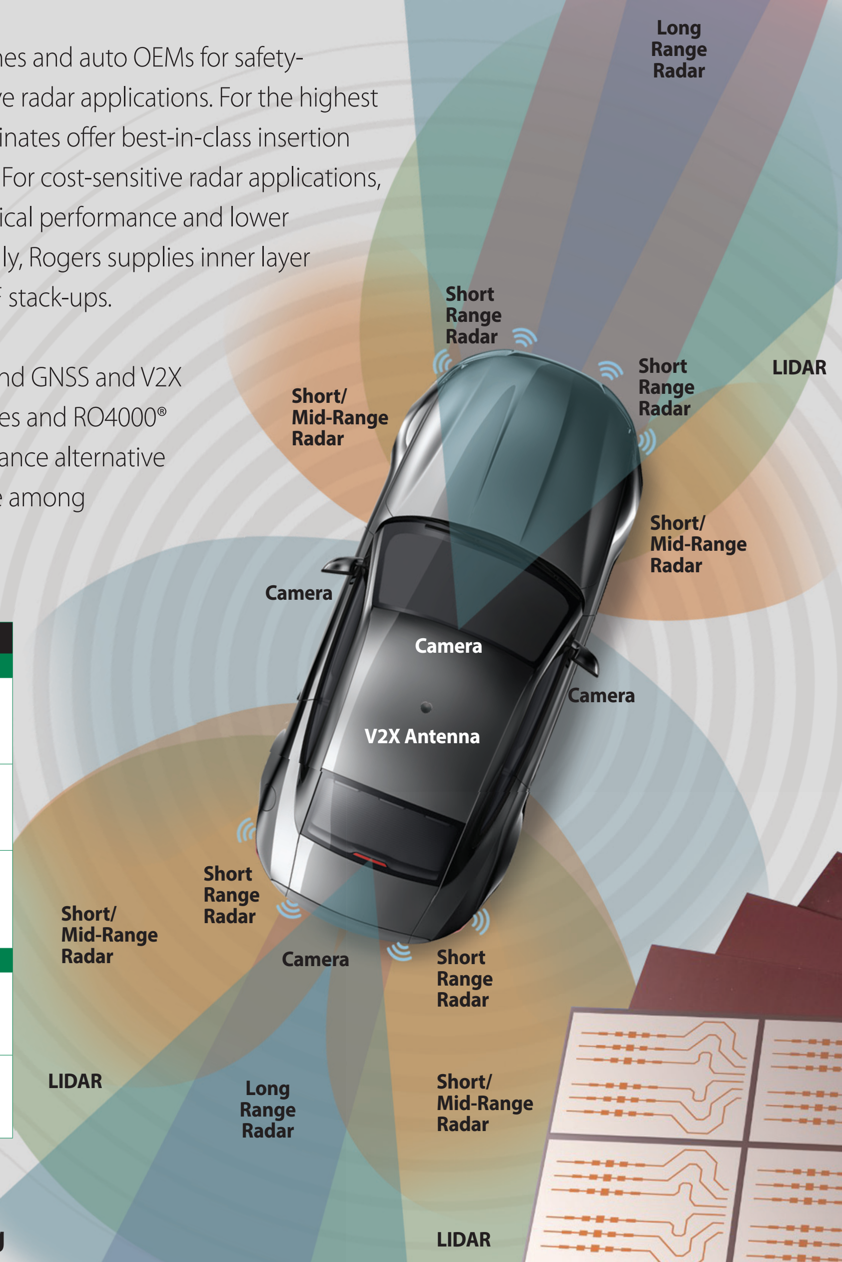
Starkey: Yes, I traditionally associate the Atotech brand with that area of expertise.

Rogers' RF solutions: Paving the way for assisted and autonomous driving

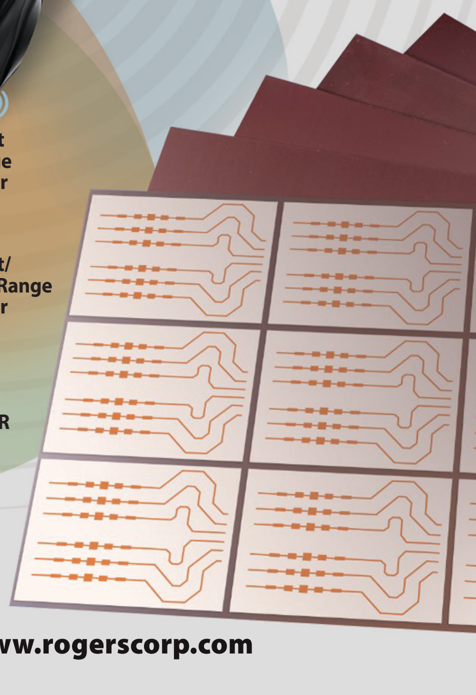
Automotive radar and vehicle-to-everything (V2X) technologies are improving the safety and enjoyment of the driver experience, as well as enabling the future of autonomous vehicles. Rogers Corporation's RF laminates and materials provide cost-effective, proven-reliable building blocks for these demanding automotive antenna applications.

Rogers' materials are trusted by global Tier Ones and auto OEMs for safety-critical 76-81 GHz front and corner automotive radar applications. For the highest performance PCB antennas, RO3003G2™ laminates offer best-in-class insertion loss and extremely stable dielectric constant. For cost-sensitive radar applications, RO4830™ laminates provide consistent electrical performance and lower material and PCB fabrication costs. Additionally, Rogers supplies inner layer and bondply material options for complex RF stack-ups.

With increasing RF requirements for multi-band GNSS and V2X antenna applications, look to Kappa® laminates and RO4000® laminates and bondplys for a higher performance alternative to FR-4 which provides the optimum balance among price, performance, and reliability.



Material	Features
76-81 GHZ AUTOMOTIVE RADAR ANTENNA MATERIALS	
RO3003G2™ Laminates	Best RF performance and board level reliability
RO4830™ Laminates	Cost-effective performance
RO4000 Laminates and Bondplys, SpeedWave® 300P Bondply	Inner layer and bondply options for multi-RF layer designs
GNSS / V2X ANTENNA MATERIALS	
Kappa® 438 Laminates	Higher performance alternative to FR-4
RO4000 Series Circuit Materials	Low loss, FR-4 processable, UL 94 V-0



To learn more visit:
www.rogerscorp.com/autonomousdriving

ROGERS CORPORATION

USA - AZ, tel. +1 480-961-1382 • EUROPE - BELGIUM, tel. +32 9 235 3611 • **www.rogerscorp.com**

Tobias Helbich

Helbich: Exactly. The PCB area is a very large field, and we offer a range of products that have earned us a market-leading position. I'm currently working for our semiconductor area. We have all kinds of technology leading in certain areas, which we can talk more about in this interview.

Starkey: What products and applications do you specialize in when it comes to the semiconductor field?

Helbich: To answer that question, I'll start with our three pillars. Our first is electrochemical deposition, which primarily comprises our products for the advanced packaging fields. Then we have electroless deposition, where we have strong products, for example, for power electronics; and we have our third pillar, which is the damascene chemistry.

Starkey: Could you explain a little about the damascene chemistry? That's a concept I'm unfamiliar with.

Helbich: Damascene chemistry is mostly copper- and cobalt-based; it's the first plating step adjacent to the front-end part of the chip. The role of the damascene layers is to connect the different transistor segments with each other and translate the small structures on the silicon wafers with the larger structures you need to contact the advanced packaging layer.

The damascene process uses a copper or cobalt chemistry to form the electrical connections on a chip between the transistors, and between transistors and the external world. We call these electrical connections interconnects. The interconnects closest to the transistor device level, which we call the "front end of the line," are the smallest and most challenging to form. As you build up the additional layers, the interconnects become larger and will finally connect the chip to the outside world via advanced packaging metallization.

Starkey: I think I can visualize it now. My background is in electrochemistry and some of the electroless chemistry, but I've always seen MKS' Atotech as a world leader in those technologies—principally in the printed circuit board application area.

Helbich: Right. The damascene chemistry is also an electrochemical deposition process. We internally separate it into a third pillar because the processes have different requirements than processes targeted toward advanced packaging applications. The damascene field is really where we are talking about the smallest plated structures of only some nanometers, much smaller than what you would find on PCBs.

Starkey: Just looking around the booth I can see that you have a big feature on advanced packaging. Very briefly, can you give me an overview of this area?

Helbich: Of course. We have a variety of applications for advanced packaging and wet chemical processes. I think the two major ones would be redistribution layers (RDLs), and the other one is pillars, which we most often combine with solder—basically solder tops that you then use to connect chips during packaging. To give you some more details on the redistribution layers, we offer, for example, very high purity copper chemistries like Spherolyte® UF 3, which is one of the big players in the market because it can form the smallest lines and spaces. We are talking about down to even one micrometer lines and spaces nowadays. Additionally stacking of RDL layers goes hand in hand with certain requirements like filling of features, where we offer market leading performance. The redistribution layers are responsible for connecting structures within the plane—connecting the different areas of the chip.

Historically, when we talked about pillars, we were talking about solder application. For larger structures you had the tin-silver or tin-solder bump directly on the pad. But due to miniaturization, it's more favorable if you have smaller pillars with a little solder bump on top. You have to consider electrochemical deposition chemistry with the pillars, which are mostly made of copper; quite often, a nickel layer is used as a diffusion barrier, but because Spherolyte® UF 5 is so pure, we don't necessarily need this nickel layer for our processes. Some customers still want it, though, because they've always had it. On top of that, you have mostly tin-silver deposits, or sometimes tin, depending on the customer's requirements.

Starkey: There used to be two distinct technology areas: PCB and semiconductor/packaging. Nowadays, the two are getting closer together, and I think advanced packaging will be a big area of future development for the PCB side. Do you have any comments on the merging of these two technologies?

Helbich: I totally agree; I also see that happening. I think this is one of the advantages that we as a company now have, of course; having a long successful history in PCB and being successful in semiconductor packaging gives us the opportunity to follow this trend from both sides and opens the field for in depth study.

Starkey: You've been able to offer expertise in both areas. In this case, it's just a question of how to reapply existing knowledge, rather than trying to build knowledge in areas you're unfamiliar with.

Helbich: Exactly. You see this in technologies like our electroless deposition processes. In the semiconductor area, you often have metal pads—under-bump metallization—which are basically contacts for wire bonds, similar to bonding processes like soldering. On the PCB side, for example, you also have these classic ENEPIG stacks, such as nickel, palladium, gold stacks. This is one of the technology areas where you see similar processes coming together. Of course, the requirements differ in some aspect.

This is one of the technology areas where you see similar processes coming together.

This also brings me to our second pillar: electroless deposition. In this area, we offer a variety of nickel processes. We needed a range of options in this area because requirements vary across applications; for example, phosphorus content might be a consideration, or the requirements for high temperature applications, and so on. Then we have a palladium process; here, purity is key for reliability, and we are one of the leading companies when it comes to pure palladium deposits. We're working together on this with the big players in the power semiconductor field. Then there's the gold layer, which requires different processes depending on how thick you need the layers. There are other varieties too, of course, like cyanide-based or cyanide-free processes and so on. We're well positioned in that we offer a full range of application processes to meet any need.

Starkey: These sound like exciting developments for MKS' Atotech.

Helbich: Absolutely, especially when we think about the bigger picture. Our electroless applications are often used, as I already mentioned, in the power semiconductor area, and we are also offering advanced solutions for electrical vehicles, which is another interesting area for which our customers demand solutions.

Starkey: I'm sure you are well prepared for a substantial and exciting future.

Helbich: The entire team is excited and will continue to give their best day in and out. So yes, thank you.

Starkey: It's been a great pleasure to meet you and to talk with you about these technologies.

Helbich: Thank you very much for your time, and I hope to see you next year again here in Munich.

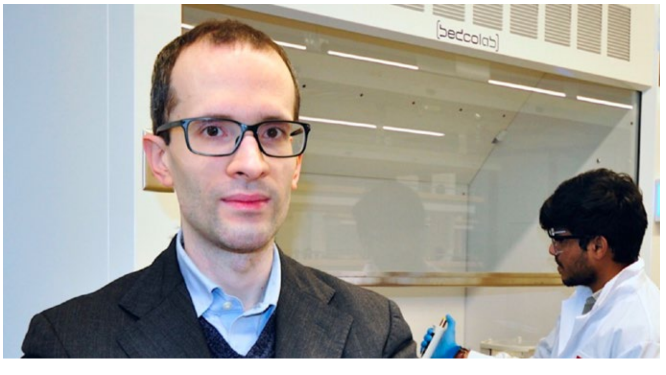
Starkey: I look forward to it. Thank you again. **PCB007**

Self-powered, Printable Smart Sensors Created from Emerging Semiconductors Could Mean Cheaper, Greener Internet of Things

Simon Fraser University

Creating smart sensors to embed in our everyday objects and environments for the Internet of Things (IoT) would vastly improve daily life—but requires trillions of such small devices. Simon Fraser University professor Vincenzo Pecunia believes alternative semiconductors that are printable, low-cost and eco-friendly could lead the way to a cheaper and more sustainable IoT.

Pecunia has identified key priorities and promising avenues for printable electronics to enable self-powered, eco-friendly smart sensors. His forward-looking insights are outlined in his paper published on Dec. 28 in Nature Electronics.



"Equipping everyday objects and environments with intelligence via smart sensors would allow us to make more informed decisions as we go about in our daily lives," says Pecunia. "printable semiconductors can deliver electronics with a much lower carbon footprint and cost."

Pecunia says making printable electronics that can work using energy harvested from the environment—from ambient light or ubiquitous radiofrequency signals, for example—could be the answer.

"Our analysis reveals that a key priority is to realize printable electronics with as small a material set as possible to streamline their fabrication process, thus ensuring the straightforward scale-up and low cost of the technology," says Pecunia. The article outlines a vision of printed electronics that could also be powered by ubiquitous mobile signals through innovative low-power approaches—essentially allowing smart sensors to charge out of thin air.

"Based on recent breakthroughs, we anticipate that printable semiconductors could play a key role in realizing the full sustainability potential of the Internet of Things by delivering self-powered sensors for smart homes, smart buildings and smart cities, as well as for manufacturing and industry."


APEX EXPO IPC 2023
MEETINGS & COURSES Jan. 21-26
CONFERENCE & EXHIBITION Jan. 24-26
SAN DIEGO CONVENTION CENTER | CA
ADVANCE IN A NEW ERA
technology
cyber security
automation
data analytics
packaging
Factory of the Future
networking
substrates
innovation
transformation
Advance your career in a new era of electronics manufacturing with networking at IPC APEX EXPO 2023. Meet leading innovators and designers, connect with peers, and create new business opportunities at North America's largest gathering of electronics manufacturing professionals on our world class show floor.
IPCAPEXEXPO.ORG

The Subtractive Vision

The Chemical Connection

by Christopher Bonsell, CHEMCUT

The November 2022 issue of *PCB007 Magazine* included a fair amount of discussion on the growing need for ultra-high-density interconnects (UHDI), an area replete with manufacturing challenges due not only to the feature sizes this technology requires (<50 micron or <2 mils), but also the lack of familiarity U.S. manufacturers have with this technology.

In an interview titled "Understanding the UHDI Market," Calumet's Todd Brassard and Meredith LaBeau stated that the U.S. is roughly 30 years behind the curve in manufacturing UHDI, which is likely the result of companies offshoring UHDI manufacturing for many years. With this gap in manufacturing expertise, we are left asking: How can we catch up? The CHIPS Act may help us shine some light on semiconductor technologies, but if we truly want to see the rapid change necessary to successfully compete against overseas companies that have been in this business for over 20 years, we will need an edge in the market. To get ahead of the competition, we need to push for improvements in subtractive processes and move toward a subtractive-driven PCB fabrication process.

From Semi-additive to Subtractive Manufacturing

By subtractive-driven process, I am referring to a PCB manufacturing process that does not require the use of a semi-additive process (SAP) to meet specifications. Moving to a subtractive-driven process for manufacturing PCBs would significantly impact the industry. Currently, SAP is necessary to obtain ultra-high-definition features; but because SAP requires additional plating steps, PCB fabrication becomes much more expensive. This is because plating is a technically challenging process, requiring lots of expertise and time on the part of highly skilled workers. Plating is also a lengthy process that adds to manufacturing time. With so many factors at play in producing UHDI resolution, there's always a significant chance that some panels will not

meet specifications—especially considering the current state of expertise and technology in the United States. For U.S. manufacturers, UHDI is very much a high-cost low-yield process. The industry has been exploring different ways to make fine features more obtainable, but so far, if you want to have a high-volume production facility, there is no way around SAP.

Although the situation puts the U.S. at a disadvantage, what if it we could skip the middle plating processes entirely while still achieving UHDI level resolution? This may be the PCB fabricator's dream, but a subtractive-driven process might make this dream a reality. Here is how a subtractive-driven process could theoretically benefit manufacturers:

- More floor space
- Reduced fabrication time
- Less need for specialized workers
- Reduction of plating chemicals in storage
- Reduction of waste from plating processes
- Less process maintenance

If you can eliminate the need for the middle plating processes, your PCB fabrication process will become more efficient. To realize this goal, the industry would need to overcome several barriers.

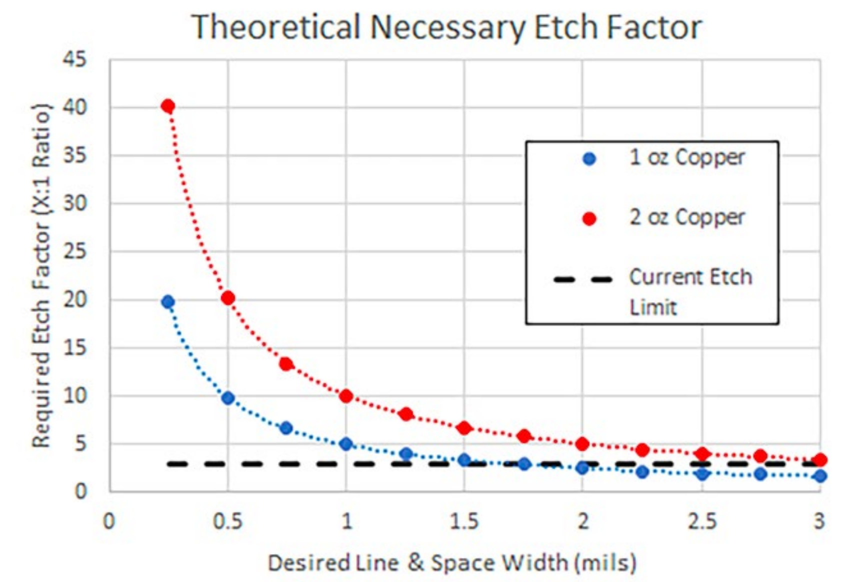


Figure 1: Estimated required etch factor to obtain various feature dimensions on 1-ounce and 2-ounce copper.

Revitalizing Copper Etch Chemistry

To become independent from SAP, we need to obtain better etch factors. Recall that etch factor is the ratio of downward etching to sideways etching. In the field of copper etching, the current standard etch factor is 3:1, but can go as high as 4:1 depending on the etchant being used. If we want to side-step SAP and have a subtractive approach to UHDI resolution, we need to obtain a bare minimum etch factor. Feature size requirements will depend on the final copper thickness needed (see Figure 1).

As shown from the diagram, the finer the features, the bigger the jump in etch factor requirements. For example, if we want to etch finer features on panels with thicker copper layers, our etch factors must compensate for that extra etch depth. Unfortunately, regarding copper, there is currently no sufficient way to dramatically improve etch factor. While there is some room for improvement on the fluid dynamics end, to reach etch factors of 20:1 or 40:1, we will need to see an improvement in the base chemistry.

An improvement could look like an entirely new etchant, or an additive to the etchants that are currently used through the industry. As I mentioned in my August 2022 column "The Etch Factor," we did get fairly close to having straight sidewalls with a PCB etchant via an additive to ferric chloride etchant that helped restrict the sideways etch. This etching process—called PERI etch—never took off in PCB manufacturing because it requires an etchant that can't be regenerated, thus significantly increasing the cost of etching. However, since we have had modest success in approaching

the high etch factors necessary to break from SAP, focusing our research efforts into copper etch chemistry might result in revolutionary developments for the industry.

To achieve this, we will need to grab the attention of the younger generation (those with a chemistry background, in particular) and bring their attention to this issue. If we can manage to get the next generation and academia invested in copper etch chemistry, we may see a rapid shift in the industry. Even if we discover that etch factors on a scale of 20:1 is impossible, PCB manufacturers still stand to benefit from general improvements in etch factor. Although it would be ideal to achieve fine features without SAP, we can still use SAP to further improve the features we have. Improving etch factors will open doors to obtaining the fine features necessary for UHDI resolution.

Conclusion

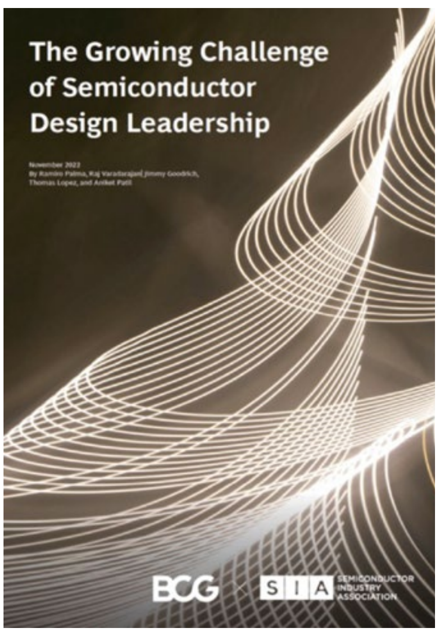
Improvements in etch factor will drive PCB manufacturing into the future and potentially allow U.S. manufacturers to get ahead of the market. Improvements in etch factor may result in a rapid shift towards subtractive-driven manufacturing processes. To achieve such progress, significant investment needs to be made in research on copper etching chemistry, which will allow us to determine how far etch factor limitations can be pushed. **PCB007**

Christopher Bonsell is a chemical process engineer at Chemcut. To read past columns or contact Bonsell, click here.

New Report Identifies Challenges to Continued U.S. Leadership in Semiconductor Design, Innovation

by Semiconductor Industry Association

Following the historic enactment of the CHIPS and Science Act to reinvigorate domestic semiconductor manufacturing and research, the Semiconductor Industry Association (SIA) and the Boston Consulting Group (BCG) today released a report finding continued U.S. leadership in semiconductor design—the critical and high-value-add mapping of a chip's intricate circuitry—is essential to America's sustained leadership in semiconductors and the many technologies they enable. The report, titled "The Growing Challenge of Semiconductor Design Leadership," identifies three key challenges facing the U.S. chip design sector and highlights opportunities to strengthen America's position as a global semiconductor innovation and workforce leader.



The report finds that a federal investment in semiconductor design and R&D of approximately $20 billion to $30 billion through 2030—including $15 billion to $20 billion for an investment tax credit for semiconductor design—will help maintain long-term U.S. chip design leadership. Such an investment would fortify the U.S. design ecosystem, support training and employment for more than 150,000 jobs across the economy, and help the U.S. win the global competition for key semiconductor-dependent innovations of the future, according to the report. The CHIPS and Science Act—now codified in 15 U.S.C. Ch. 72A § 4651-4659—includes a critical investment tax credit for semiconductor manufacturing, but not for design. The SIA-BCG report also highlights the importance of promoting STEM workforce development and ensuring open access to global markets, among other priorities.

I-Connect007 GOOD FOR THE INDUSTRY

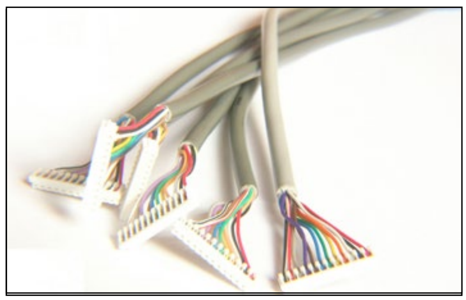
REALTIME with... PREMIUM SPONSOR

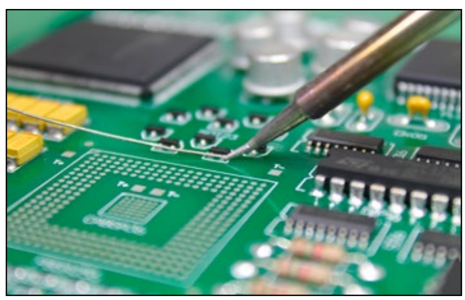
The Top Five Things You Need to Know About MANUFACTURING TRAINING

by Blackfox Training

Electronics manufacturing companies need skilled and certified workers to perform the intricate and important tasks required to build modern electronic equipment. Here, we explain five ways to gain these workers:

1. **Train and Certify Manufacturing Employees and Support Staff to the IPC Standards**
2. **Fill Training Gaps with Customized Courses that Focus on Basic Knowledge and Skills**
3. **Access Tools and Resources to Assess Your Workforce and Maintain Skill Levels**
4. **Stay Up to Date with Constant Changes in the Electronics Manufacturing Industry**
5. **Hire U.S. Military Veterans Who Have Already Completed Immense Training**





1 Train and Certify Manufacturing Employees and Support Staff to the IPC Standards

IPC certification is an internationally recognized credential that proves an employee's knowledge and skill level. IPC training and certification is industry developed and covers electronic manufacturing quality concerns, including PCB assembly and soldering, rework and repair, wire and cable harness production, and bare PCB fabrication. Having an IPC-certified workforce demonstrates an attention to detail and commitment to quality.

2 Fill Training Gaps with Customized Courses that Focus on Basic Knowledge and Skills

IPC training and other standardized courses don't cover every aspect of electronics manufacturing. Therefore, it is important to have customized courses that fill those missed gaps. Basic soldering, ESD, and electronic component identification are just a few examples of the many courses that complement IPC certification and ensure that your workforce is prepared for any challenges that may come their way.

3 Access Tools and Resources to Assess Your Workforce and Maintain Skill Levels

Assessing your workforce before and after training is an essential part of a proper manufacturing training program. The effectiveness of training and the retention of knowledge gained can be gauged through assessments that are computer-based, interview-based, or audit-based. In addition to assessments, both students and trainers need to have complete access to resource documents and training materials after training has been completed.

4 Stay Up to Date with Constant Changes in the Electronics Manufacturing Industry

Technological advances and new discoveries are occurring constantly that greatly impact how we manufacture electronic products and evaluate them for quality. This makes maintaining your IPC Certifications through renewal and recertification critically important. In addition, attending industry meetings and participating in IPC committees will ensure access to the latest information.

5 Hire U.S. Military Veterans Who Have Already Completed Immense Training

Now more than ever, highly skilled and efficient employees are needed in manufacturing. The U.S. military invests an enormous amount of training in our soldiers. They are equipped with a framework of skills and attributes such as loyalty, integrity, leadership, and excellent work ethic. They know how to learn new skills quickly and adapt to changing environments, which are highly desirable qualities for manufacturing.

BLACKFOX®
Premier Training & Certification

Blackfox is the worldwide leader in providing IPC certification and custom training systems to the manufacturing industry's top companies. Blackfox provides solutions for the manufacturing industry and for veterans seeking employment. Visit us online at Blackfox.com.

I-Connect007 GOOD FOR THE INDUSTRY REALTIME with... PREMIUM SPONSOR

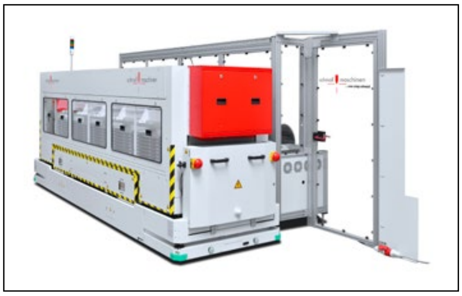
The Top Five Things You Need to Know About

DRILLING AUTOMATION SOLUTIONS

by Burkle North America

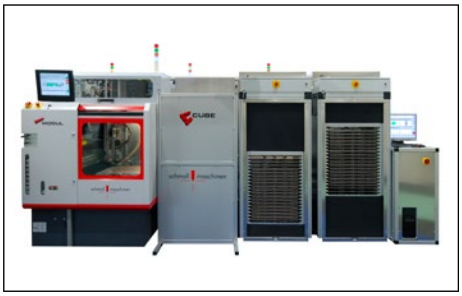
Living in this era of rapid technological progress, PCB production is making a noticeable shift toward automation. What was once manufactured manually with human hands and low production numbers has transitioned to high volume production using precise and efficient machines. Today, Industry 4.0 and artificial intelligence are further expanding the boundaries of automated production.

1 Automation in PCB Production



2 Registration, Alignment, Accuracy

3 Maximum Productivity with the Right Application



4 Automation Possibilities

5 Features for Automation to Increase Utilization

1 Automation in PCB Production

PCB manufacturers worldwide are investing in new equipment to improve technology and production, especially in the field of automation. In Europe, the automation of drilling machines is already standard to increase producivity and achieve a higher degree of utilization. The current talent shortage in the U.S. and Canada is accelerating the demand for automation as well. Drill and rout machines with shuttle system and loaders; direct imaging machines with robot arms; and X-ray capabilities with drill and inline automation already allow the automatic loading and unloading of PCBs and ensure contact-free panel handling in the factory, which results in both labor cost savings and quality assurance in the PCB.

2 Registration, Alignment, Accuracy

Highly technologized devices such as spindles, lighting-heads, laser sources, cameras, code readers, and sensors are built-up on solid granite and then connected to the machine controller to deliver perfect results and ensure highly accurate PCB processing. For high-end panels, machines with CCD are an option, as any inaccuracies of the panel will be corrected. A two-pin system on panels is mandatory for automated drilling and a well-proven process to support the needed accuracy.

3 Maximum Productivity with the Right Application

Track and trace technology is also being adopted in the handling of PCBs. With a barcode or 2D code, panels can be uniquely identified and processed according to the specific CAD/CAM program. Integrated CCDs and scanner systems in the machines handle the reading of specific part programs.

Automated calibration procedures ensure machine accuracies at the highest level to ensure quality of drilled, routed, and imaged products. Automated spindle maintenance reduces machine down-time and increases productivity.

4 Automation Possibilities

The engineering industry has recently advanced with Industry 4.0 and the building up of several new standards. Drill, rout, and laser machines can be equipped with a loader to feed the panels automatically—one of the new simplified solutions. X-ray and direct imaging machines can now be put into a production line with belt conveyors and run at a constant speed, resulting in increased output. Panels are then handled with robot arms. More robotics have also been introduced to the market, including automated guided vehicles, automated line systems, and shuttle systems.

5 Features for Automation to Increase Utilization

Standard SW interfaces to the MES allow bi-directional communication between machines and high-level production controls, which allows for real-time status information. An operator can have remote access to all machines from the control room, allowing them to monitor automated PCB production, run statistics, and react quickly to any error message or breakdowns.

Bürkle North America distributes and services Bürkle GmbH and Schmoll Maschinen equipment which includes IMPEX and LHMT. BNA distributes equipment lines for multilayer lamination, drilling, cutting, routing, imaging, registration, automation and measuring. Visit Burkle North America online.

schmoll maschinen
BÜRKLE
NORTH AMERICA, INC.

I-Connect007 GOOD FOR THE INDUSTRY

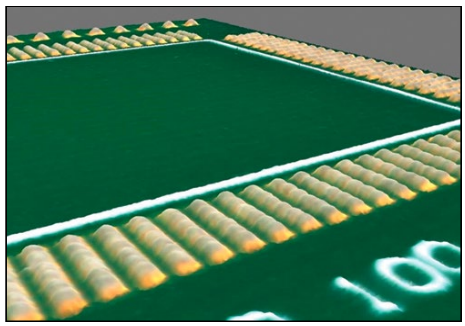
REALTIME with... PREMIUM SPONSOR

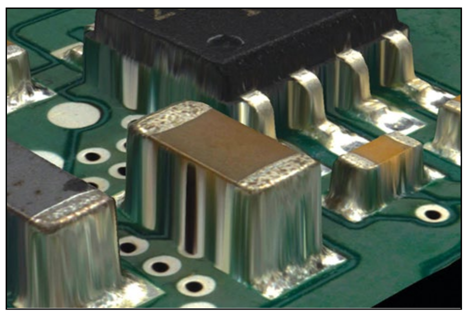
The Top Five Things You Need to Know About INSPECTION

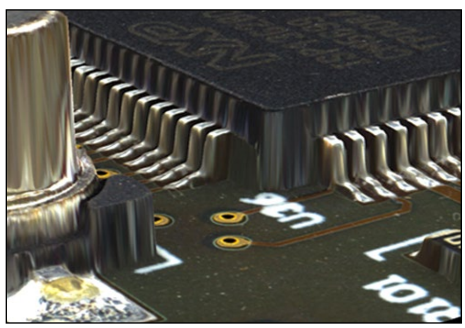
by Mycronic

Inline 3D SPI and 3D AOI are the most cost-effective ways to control and optimize process efficiency. To get the most from your investment, here are five things to consider:

1. AI-assisted Software for Easier and Faster Programming
2. Reliable and Approximation-free Volume Measurement of Paste Deposits for Highest SPI Efficiency
3. Real-time Auto-control of 3D AOI Program Efficiency to Prevent False Calls and Escapes
4. Flexible and Agile 3D AOI Technology to Ensure Consistent Performance
5. Process Control Based on Inspection Data Analysis to Maintain Highest First-pass Yield







1 AI-assisted Software for Easier and Faster Programming

Today, AI technologies make it possible to program 3D SPI and 3D AOI in record time, regardless of the operator's experience level. With MYPro Create, SPI and AOI programming is not only easier, faster, and more cost effective, but also less operator dependent. This brings inspection within the reach of low-volume/high-mix electronics manufacturers for whom speed and flexibility are prerequisites.

2 Reliable and Approximation-free Volume Measurement for Highest SPI Efficiency

Accurate Z-referencing is key to reliable inspection for increasingly miniaturized solder paste deposits. The PI series 3D SPI processes hundreds of references across its ultra-large field of view, positioning the Z-reference at the surface of each pad without applying thresholds or approximations. Regardless of board warpage, you always know the exact volume of paste deposited on even the smallest pads.

3 Real-time Auto-control of 3D AOI Program Efficiency to Prevent False Calls and Escapes

When programming your 3D AOI, how can you ensure that your last library modifications will not generate excess false defects, or worse, miss real defects? With Escape Tracker, the MYPro I series 3D AOI alerts to potential escapes and false calls generated during both programming and fine-tuning and points out the corrections necessary to avoid them.

4 Flexible and Agile 3D AOI Technology to Ensure Consistent Performance

An all-in-one 3D AOI technology needs to be extremely reliable and as flexible as possible to address changing customer requests. Mycronic's MYPro I series includes the industry's most comprehensive standard toolbox to help users manage the broadest range of applications, enabling: state-of-the-art test coverage; top and bottom THT and odd-shaped component inspection; and metrological testing, all with the same standard equipment.

5 Process Control Based on Inspection Data Analysis To Maintain Highest First-Pass Yield

Inspection equipment is the sensor of an SMT assembly line. MYPro Link, a real-time web-based interface, correlates and analyzes SPI and AOI data to transform this information into useful KPIs for monitoring production performance. Add detailed root-cause analysis from MYPro Analyze, and you can anticipate process variation and correct process drift in real-time.

I-Connect007
GOOD FOR THE INDUSTRY

REALTIME with... PREMIUM SPONSOR

The Top Five Things You Need to Know About

SOLDER MASKS

by Taiyo America

The main function of solder mask is to insulate and prevent the copper surface from oxidizing/corroding and prevent solder bridging. While these are the main objectives for solder mask, in the electronics industry there is a misconception that all solder masks are alike.

1 Selecting the Right Solder Mask

2 Solder Mask Applications Evolve

3 Advances in Solder Mask Imaging

4 To Flex or Not to Flex

5 Solder Masks Are Not Only Green

1 Selecting the Right Solder Mask

In the world of electronics there are multiple industries each with their own requirements when it comes to solder mask. For the automotive sector, solder masks are required to withstand harsh environments. In the aerospace industry, solder masks must meet out-gassing requirements. Over the years, white solder masks have been developed that provide a high degree of reflectivity for the LED market.

2 Solder Mask Applications Evolve

Solder mask and the methods by which they were applied have evolved over the years. When non-photoimageable solder resists were introduced to the printed circuit board (PCB) industry, silk screen printing was the common method of application. As the demand for real estate on PCB designs increased, photoimageable solder masks were developed. The popularity of photoimageable solder masks introduced new application systems such as double-sided screen printing, curtain coating and spray systems. These methods of application have been around for many years and are still being used today. In the past five years, several other application processes have been reintroduced to the market including ink jet and photoimageable dry film.

3 Advances in Solder Mask Imaging

As technologies advance and offer more functions, PCBs have become more populated with the miniaturization of key components. The advancements have pushed the boundaries on image registration using conventional exposing units. Over the years, direct imaging (DI) systems were introduced to the PCB industry to help alleviate the challenge. The DI systems provide different wavelengths in comparison to conventional exposing units. Solder mask manufacturers, working side-by-side with equipment manufacturers, developed DI solder masks that are better suited for these types of imaging systems.

4 To Flex or Not to Flex

Solder masks have some degree of pliability. Thinner PCBs that are not categorized as a flex build can sometimes encounter a degree of bending due to handling or manufacturing processes. Depending on the amount the substrates are bent, they can exhibit a degree of fracturing. Fracturing of the solder mask is not the same as corner cracking caused by exposure to harsh environments. In cases such as this, PCB manufacturers and contract electronics manufacturers (CEM) should consider the use of a flexible solder mask.

5 Solder Masks Are Not Only Green

Solder masks have evolved from green to several other colors over the years. The most common colors besides green are black, blue, red, white, and yellow—all of which fall in the family of primary colors. Colors were developed and brought to market at the request of original equipment manufacturers (OEMs). Colored solder mask can be used for identifying prototypes, revision changes, manufacturing facilities, or for cosmetic reasons. Colored solder masks can also be combined in measured amounts to create a vast number of other colors such as orange, purple and brown. Solder masks can also have various surface finishes such as matte, glossy, or somewhere in between, depending on customers' requirements.

I-Connect007 GOOD FOR THE INDUSTRY

REALTIME with... PREMIUM SPONSOR

The Top Five Things You Need to Know About

LONG-LASTING PARTNERSHIPS

by Technica, U.S.A.

A good supply partner becomes an extension of your business. Having the right one gives you an advantage and peace of mind. Choose wisely.

1. **Create Long and Strong Partnerships**

2. **Low Risk of Interruption of Support**

3. **Visibility Into Local and OEM Parts Inventory**

4. **Constantly Advancing Quality and Technology**

5. **Service Staff With Product, Process and Application Experience**

1 Create Long and Strong Partnerships

Partnership is a word often used in business relationships but a true partnership is built on trust and visibility. The investment of our people's time and effort has provided us with the privilege to share in true partnerships with our suppliers and customers. True partnerships withstand tough times from either side of the partnership and when the challenges arise, a True partnership comes alive.

2 Low Risk of Interruption of Support

Downtime in this environment is extremely costly and finding technical support when you need it is critical to any manufacturing business. Working with supply partners to help develop innovative programs and methods for responding to issues is important. Making sound decisions on where our supply partners are located allows us to minimize the risk of interruption caused by geopolitical concerns.

3 Visibility Into Local and OEM Parts Inventory

There is nothing more important than having 24/7 visibility to spare parts inventory. Working with a supplier that carries a large inventory of spare parts is essential in eliminating down time. Having ongoing dialogue between all parties to match inventories of critical spare parts is important part of a partnership.

4 Constantly Advancing Quality and Technology

R&D is key to maintaining your competitive advantage. It improves your quality, capability, and market growth opportunities. Suppliers that are committed to working with us and our customers towards advancement and improvement is essential to the future of our businesses.

5 Service Staff with Product, Process and Application Experience

There is no substitute for experience when it comes to a service team. Make sure your suppliers are providing you with expert knowledge that you can trust and rely on.

About Technica

Since 1985, Technica, U.S.A. has been providing the electronics marketplace with innovative products manufactured by the world's leading suppliers that provide our customers with technological advantages for producing complex electronic products.

TOP TEN

EDITOR'S PICKS

EIPC Technical Snapshot: 'There Is No Green Without Digital'


Emma Hudson

Introduced and moderated by EIPC's Emma Hudson, the 20th EIPC Technical Snapshot focused on sustainability, specifically on environmental issues impacting the electronics industry. The first speaker was Pia Tanskanen, head of environment at Nokia in Finland. A pioneer in mobile telecom, Nokia is primarily a network hardware and software provider, committed to reducing the environmental impact of its products, operations, manufacturing, and supply chains, with sustainability a key component of the company's strategy.

Industry Innovation Starts Here

If it isn't clear already, your money, time, and effort will be well spent attending IPC APEX EXPO in January. Here, we've outlined the top six reasons that this event will be the highlight of your year.

Let's Get Technical

IPC members are constantly working to move the electronics industry forward by developing new technologies, innovative processes, and testing methods—and working to find solutions to known technical challenges. The IPC APEX EXPO Technical Conference is the premier forum in North America where these challenges, solutions, and innovations are shared among colleagues and competitors alike.

Happy's Tech Talk #14: Palladium as a Final Finish

Karl Dietz never wrote on the topic of palladium as a final finish, but he did write about gold plating as a final finish and had an excellent discussion on copper plating. But palladium now has a renaissance as a final finish. Palladium was very popular with the automotive industry in the 1970s.

The Chemical Connection: Cupric Chloride Regeneration Options

Cupric chloride ($CuCl_2$), if you recall my column “Etchants of the Industry: Cupric vs. Alkaline,” is the second most used etchant in PCB etching next to alkaline etchant. It holds many benefits such as simple maintenance, easy wastewater treatment, reduced cost of etching, and efficient regeneration.

Dan’s Biz Bookshelf: End the Time Sink With ‘Make Meetings Matter’

Like everyone else, I have been subjected to a lot of pointless meetings in my day. You know what I’m talking about: meetings where some blowhard pontificates for an hour, reveling in the sound of his own voice while the rest of us are stuck there, silently praying for release.

Testing Todd: Decision Time—Invest or Delegate?

As they struggle to keep delivery times competitive, manufacturers are faced with a decision: Do I invest, or should I delegate? To stay competitive, a large percentage of capital must be slated for PCB manufacturing equipment. This is understandable as that is where the revenue is generated. Newer equipment begets higher technology builds and thus, more revenue.

Rogers: Bringing New Materials to Light


Dr. Vitali Judin

Pete Starkey talks with Dr. Vitali Judin, the new business development manager at Rogers, on how the company is making a splash with new high frequency materials meant to address the rapidly evolving needs of the additive manufacturing sector. Rogers determined that digital light processing (DLP) 3D printing technique brought the combination of speed and resolution necessary to make additive manufacturing reasonably scalable, then partnered with Fortify to bring the processing consistency needed for the RF industry.

Kirk Lockett Sr. of IEC USA Remembered


Kirk Lockett Sr.

Kirk T. Lockett Sr., former president, owner, and operator of Intermountain Circuit Supply, passed away on Dec. 7, 2022.

Punching Out: When Less Might Actually Be More

According to GP Ventures’ database, the number of PCB companies in North America is now down to 170. Just 22 months ago, the number was 199. Frankly, the actual number of active PCB manufacturers in the United States and Canada is probably closer to 150, but it is hard to keep track of the smaller shops.

For the latest news and information, visit **PCB007.com**

Career Opportunities

Find industry-experienced candidates at jobConnect007.

For just $750, your 200-word, full-column ad will appear in the Career Opportunities section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs, suppliers and the academic community.

In addition, your ad will:

- be featured in at least one of our newsletters
- appear on our jobConnect007.com board, which is promoted in every newsletter
- appear in our monthly Careers Guide, emailed to 26,000 potential candidates

Potential candidates can click on your ad and submit a resume directly to the email address you provide, or be directed to the URL of your choice.

No contract required. Just send over your copy and company logo and we'll do the rest!

Contact barb@iconnect007.com to get your ad posted today!

+1 916.365.1727

I-Connect007
GOOD FOR THE INDUSTRY

smt007 pcb007 pcb design007

Career Opportunities

TAIYO AMERICA

Europe Technical Sales Engineer

Taiyo is the world leader in solder mask products and inkjet technology, offering specialty dielectric inks and via filling inks for use with microvia and build-up technologies, as well as thermal-cure and UV-cure solder masks and inkjet and packaging inks.

PRIMARY FUNCTION:

1. To promote, demonstrate, sell, and service Taiyo's products
2. Assist colleagues with quotes for new customers from a technical perspective
3. Serve as primary technical point of contact to customers providing both pre- and post-sales advice
4. Interact regularly with other Taiyo team members, such as: Product design, development, production, purchasing, quality, and senior company managers from Taiyo group of companies

ESSENTIAL DUTIES:

1. Maintain existing business and pursue new business to meet the sales goals
2. Build strong relationships with existing and new customers
3. Troubleshoot customer problems
4. Provide consultative sales solutions to customer's technical issues
5. Write monthly reports
6. Conduct technical audits
7. Conduct product evaluations

QUALIFICATIONS / SKILLS:

1. College degree preferred, with solid knowledge of chemistry
2. Five years' technical sales experience, preferably in the PCB industry
3. Computer knowledge
4. Sales skills
5. Good interpersonal relationship skills
6. Bilingual (German/English) preferred

To apply, email: BobW@Taiyo-america.com with a subject line of "Application for Technical Sales Engineer".

apply now

BLACKFOX
Premier Training & Certification

IPC Instructor
Longmont, CO

This position is responsible for delivering effective electronics manufacturing training, including IPC certification, to adult students from the electronics manufacturing industry. IPC Instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC certification programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will primarily conduct training at our public training center in Longmont, Colo., or will travel directly to the customer's facility. It is highly preferred that the candidate be willing to travel 25–50% of the time. Several IPC certification courses can be taught remotely and require no travel or in-person training.

Required: A minimum of 5 years' experience in electronics manufacturing and familiarity with IPC standards. Candidate with current IPC CIS or CIT Trainer Specialist certifications are highly preferred.

Salary: Starting at $30 per hour depending on experience

Benefits:

- 401k and 401k matching
- Dental and Vision Insurance
- Employee Assistance Program
- Flexible Spending Account
- Health Insurance
- Health Savings Account
- Life Insurance
- Paid Time Off

Schedule: Monday thru Friday, 8–5

Experience: Electronics Manufacturing: 5+ years (Required)

License/Certification: IPC Certification–Preferred, Not Required

Willingness to travel: 25% (Required)

apply now

Career Opportunities

CHEMCUT

Technical Sales Manager

Objectives

Provide sales leadership and management for a regional sales territory. Responsible for retaining current customers as well as developing and attracting new customers and markets. Responsible for selling current and new products, keeping abreast of new technologies, market trends, and customer product needs.

Essential Functions and Responsibilities

- Develop and service assigned geographic region
- Actively and consistently seek new customers
- Visit customers and potential customers to develop relationships, deliver sales presentations, follow up on leads, and close sales
- Provide technical support and product recommendations in person, by email, and phone
- Manage major accounts; establish long-term, ongoing relationships with key individuals
- Provide feedback to Chemcut as well as sales peers regarding competition, pricing, and marketing opportunities

Qualifications

- Bachelor's degree in mechanical, electrical, chemical engineering or related fields
- 3-5 years of field sales experience with technology driven industrial products
- Well-developed sales and customer relations skills
- Ability to make decisions and evaluations to determine customer needs
- Ability to travel up to 50% of the time
- Excellent oral and written communication skills
- Knowledge of target market industries

To apply, please submit a cover letter and resume to hr@chemcut.net.

apply now

Prototron Circuits

Sales Representatives

Prototron Circuits, a market-leading, quick-turn PCB manufacturer located in Tucson, AZ, is looking for sales representatives for the Utah/Colorado, and Northern California territories. With 35+ years of experience, our PCB manufacturing capabilities reach far beyond that of your typical fabricator.

Reasons you should work with Prototron:

- Solid reputation for on-time delivery (98+% on-time)
- Capacity for growth
- Excellent quality
- Production quality quick-turn services in as little as 24 hours
- 5-day standard lead time
- RF/microwave and special materials
- AS9100D
- MIL-PRF- 31032
- ITAR
- Global sourcing option (Taiwan)
- Engineering consultation, impedance modeling
- Completely customer focused team

Interested? Please contact Russ Adams at (206) 351-0281 or russa@prototron.com.

apply now

Career Opportunities

Test Engineer, Electronics Engineer

Keytronic is a dynamic, team-based contract manufacturer with facilities worldwide. Innovation defines us. Come join us in Spokane, Washington! We invite you to bring your engineering expertise and passion for excellence. In turn, we provide meaningful opportunities for you to implement these attributes to their fullest while working together to bring our customer's high-tech automotive, aerospace, medical and commercial products to full production.

We encourage you to apply to one of our open positions below if you enjoy being challenged, working in a dynamic work setting and being a part of a team creating products to improve our world.

- **Test Engineer**—You will assist in conducting electrical test engineering support involving automation, assembly, maintenance, and data collection.

- **Electronics Engineer**—You will work on a team creating electronic circuitry, writing firmware for microprocessors and interfacing with customer development teams producing a wide array of products.

apply now

Where Science and Care Converge.

Regional Manager

Midwest Region

General Summary: Manages sales of the company's products and services, Electronics and Industrial, within the Carolinas and Mid-Atlantic Region. Reports directly to Americas Manager. Collaborates with the Americas Manager to ensure consistent, profitable growth in sales revenues through positive planning, deployment and management of sales reps. Identifies objectives, strategies and action plans to improve short- and long-term sales and earnings for all product lines.

DETAILS OF FUNCTION:

- Develops and maintains strategic partner relationships
- Manages and develops sales reps:
  - Reviews progress of sales performance
  - Provides quarterly results assessments of sales reps' performance
  - Works with sales reps to identify and contact decision-makers
  - Setting growth targets for sales reps
  - Educates sales reps by conducting programs/ seminars in the needed areas of knowledge
- Collects customer feedback and market research (products and competitors)
- Coordinates with other company departments to provide superior customer service

QUALIFICATIONS:

- 5-7+ years of related experience in the manufacturing sector or equivalent combination of formal education and experience
- Excellent oral and written communication skills
- Business-to-business sales experience a plus
- Good working knowledge of Microsoft Office Suite and common smart phone apps
- Valid driver's license
- 75-80% regional travel required

To apply, please submit a COVER LETTER and RESUME to: Fernando Rueda, Americas Manager

fernando_rueda@kyzen.com

apply now

Career Opportunities

Application Engineer

Flexible Circuit Technologies (FCT) is a global supplier providing design, prototyping and production of flexible circuits, rigid flex circuits, flexible heaters and full assembly services.

Responsibilities

- Gain understanding for customer/specific project requirements
- Review customer files, analyze - application, design, stack up, materials, mechanical requirements; develop cost-effective design to meet requirements
- Quote and follow-up to secure business
- Work with CAD: finalize files, attain customer approval prior to build
- Track timeline/provide customers with updates
- Follow up on prototype, assist with design changes (if needed), and push forward to production
- Work as the lead technician/program manager or as part of FCT team working with an assigned application engineer
- Help customer understand FCT's assembly, testing, and box build services
- Understand manufacturing and build process for flexible and rigid-flex circuits

Qualifications

- Demonstrated experience: flex circuit/rigid-flex design including design rules, IPC; flex heater design +
- Ability to work in fast-paced environment, broad range of projects, maintain sense of urgency
- Ability to work as a team player
- Excellent written and verbal communication skills
- Willing to travel for sales support and customer support activities if needed

Competitive salary, bonus program, and benefits package. Preferred location Minneapolis, MN area.

apply now

Technical Marketing Engineer

EMA Design Automation, a leader in product development solutions, is in search of a detail-oriented individual who can apply their knowledge of electrical design and CAD software to assist marketing in the creation of videos, training materials, blog posts, and more. This Technical Marketing Engineer role is ideal for analytical problem-solvers who enjoy educating and teaching others.

Requirements:

- Bachelor's degree in electrical engineering or related field with a basic understanding of engineering theories and terminology required
- Basic knowledge of schematic design, PCB design, and simulation with experience in OrCAD or Allegro preferred
- Candidates must possess excellent writing skills with an understanding of sentence structure and grammar
- Basic knowledge of video editing and experience using Camtasia or Adobe Premiere Pro is preferred but not required
- Must be able to collaborate well with others and have excellent written and verbal communication skills for this remote position

EMA Design Automation is a small, family-owned company that fosters a flexible, collaborative environment and promotes professional growth.

Send Resumes to: resumes@ema-eda.com

apply now

Career Opportunities

pluritec®
MACHINES FOR PRINTED CIRCUIT BOARDS

Field Service Engineer

Location: West Coast, Midwest

Pluritec North America, ltd., an innovative leader in drilling, routing, and automated inspection in the printed circuit board industry, is seeking a full-time field service engineer.

This individual will support service for North America in printed circuit board drill/routing and X-ray inspection equipment.

Duties included: Installation, training, maintenance, and repair. Must be able to troubleshoot electrical and mechanical issues in the field as well as calibrate products, perform modifications and retrofits. Diagnose effectively with customer via telephone support. Assist in optimization of machine operations.

A technical degree is preferred, along with strong verbal and written communication skills. Read and interpret schematics, collect data, write technical reports.

Valid driver's license is required, as well as a passport, and major credit card for travel.

Must be able to travel extensively.

apply now

ventec
INTERNATIONAL GROUP
騰輝電子

European Product Manager

Taiyo Inks, Germany

We are looking for a European product manager to serve as the primary point of contact for product technical sales activities specifically for Taiyo Inks in Europe.

Duties include:

- Business development & sales growth in Europe
- Subject matter expert for Taiyo ink solutions
- Frequent travel to targeted strategic customers/ OEMs in Europe
- Technical support to customers to solve application issues
- Liaising with operational and supply chain teams to support customer service

Skills and abilities required:

- Extensive sales, product management, product application experience
- European citizenship (or authorization to work in Europe/Germany)
- Fluency in English language (spoken & written)
- Good written & verbal communications skills
- Printed circuit board industry experience an advantage
- Ability to work well both independently and as part of a team
- Good user knowledge of common Microsoft Office programs
- Full driving license essential

What's on offer:

- Salary & sales commission--competitive and commensurate with experience
- Pension and health insurance following satisfactory probation
- Company car or car allowance

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits. Please forward your resume to **jobs@ventec-europe.com.**

apply now

Career Opportunities

Koh Young America

Technical Service & Applications Engineer

Full-Time — Midwest (WI, IL, MI)

Koh Young Technology, founded in 2002 in Seoul, South Korea, is the world leader in 3D measurement-based inspection technology for electronics manufacturing. Located in Duluth, GA, Koh Young America has been serving its partners since 2010 and is expanding the team with an Applications Engineer to provide helpdesk support by delivering guidance on operation, maintenance, and programming remotely or on-site.

Responsibilities

- Provide support, preventive and corrective maintenance, process audits, and related services
- Train users on proper operation, maintenance, programming, and best practices
- Recommend and oversee operational, process, or other performance improvements
- Effectively troubleshoot and resolve machine, system, and process issues

Skills and Qualifications

- Bachelor's in a technical discipline, relevant Associate's, or equivalent vocational or military training
- Knowledge of electronics manufacturing, robotics, PCB assembly, and/or AI; 2-4 years of experience
- SPI/AOI programming, operation, and maintenance experience preferred
- 75% domestic and international travel (valid U.S. or Canadian passport, required)
- Able to work effectively and independently with minimal supervision
- Able to readily understand and interpret detailed documents, drawings, and specifications

Benefits

- Health/Dental/Vision/Life Insurance with no employee premium (including dependent coverage)
- 401K retirement plan
- Generous PTO and paid holidays

apply now

ARLON ELECTRONIC MATERIALS

Arlon EMD, located in Rancho Cucamonga, California, is currently interviewing candidates for open positions in:

- Engineering
- Quality
- Various Manufacturing

All interested candidates should contact Arlon's HR department at 909-987-9533 or email resumes to careers.ranch@arlonemd.com.

Arlon is a major manufacturer of specialty high-performance laminate and prepreg materials for use in a wide variety of printed circuit board applications. Arlon specializes in thermoset resin technology, including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, High Density Interconnect (HDI) and microvia PCBs (i.e. in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2015 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customers' requirements.

For additional information please visit our website at www.arlonemd.com

apply now

Career Opportunities

Career Opportunities

Career Opportunities

eptac
TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

apply now

American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

The CAD/CAM Engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creation of manufacturing data, programs and tools required for the manufacture of PCB.

ESSENTIAL DUTIES AND RESPONSIBILITIES

- Import Customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, penalization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design Issues with customers.
- Other duties as assigned

ORGANIZATIONAL RELATIONSHIP

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

QUALIFICATIONS

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge
- Experience using Orbotech/Genflex CAM tooling software

PHYSICAL DEMANDS

Ability to communicate orally with management and other co-workers is crucial. Regular use of the phone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

apply now

Career Opportunities


THE SOLUTIONS GUIDE TO...
Thermal Management
THERMAL MANAGEMENT – IMS MATERIALS
SIGNAL INTEGRITY
CLEAN HIGH-TECH
MECHANICAL FLEXIBILITY
IC-PACKAGING MATERIAL
ventec
INTERNATIONAL GROUP
I-Connect007
THE PRINTED CIRCUIT DESIGNER'S GUIDE TO...™
Thermal Management with Insulated Metal Substrates
THE PRINTED CIRCUIT DESIGNER'S GUIDE TO...™
Thermal Management with Insulated Metal Substrates
Volume 2
Didier Mauve and Robert Art
Ventec International Group

I-007eBooks The Printed Circuit Designer's Guide to...

Designing for Reality by Matt Stevenson, Sunstone Circuits

Based on the wisdom of 50 years of PCB manufacturing at Sunstone Circuits, this book is a must-have reference for designers seeking to understand the PCB manufacturing process as it relates to their design. Designing for manufacturability requires understanding the production process fundamentals and factors within the process that often lead to variations in manufacturability, reliability, and cost of the board. Speaking of making better decisions, read it now!

Thermal Management with Insulated Metal Substrates, Vol. 2

by Didier Mauve and Robert Art, Ventec International Group

This book covers the latest developments in the field of thermal management, particularly in insulated metal substrates, using state-of-the-art products as examples and focusing on specific solutions and enhanced properties of IMS. Add this essential book to your library.

High Performance Materials

by Michael Gay, Isola

This book provides the reader with a clearer picture of what to know when selecting which material is most desirable for their upcoming products and a solid base for making material selection decisions. Get your copy now!

Stackups: The Design within the Design

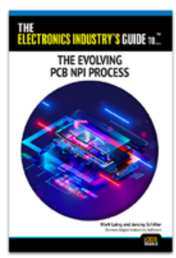
by Bill Hargin, Z-zero

Finally, a book about stackups! From material selection and understanding laminate datasheets, to impedance planning, glass weave skew and rigid-flex materials, topic expert Bill Hargin has written a unique book on PCB stackups. Get yours now!

THE ELECTRONICS INDUSTRY'S GUIDE TO... The Evolving PCB NPI Process

by Mark Laing and Jeremy Schitter, Siemens Digital Industries Software

The authors of this book take a look at how market changes in the past 15 years, coupled with the current slowdown of production and delivery of materials and components, has affected the process for new product introduction (NPI) in the global marketplace. As a result, companies may need to adapt and take a new direction to navigate and thrive in an uncertain and rapidly evolving future. Learn how to streamline the NPI process and better manage the supply chain. *Get it Now!*



Our library is open 24/7/365. Visit us at: I-007eBooks.com

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

MANAGING EDITOR: **NOLAN JOHNSON**
(503) 597-8037; nolan@iconnect007.com

EDITOR | COLUMNIST COORDINATOR: **MICHELLE TE**
michelle@iconnect007.com

CONTRIBUTING EDITOR: **PATRICIA GOLDMAN**
(724) 299-8633; patty@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

CONTRIBUTING TECHNICAL EDITOR: **DAN FEINBERG**
baer@iconnect007.com

CONTRIBUTING TECHNICAL EDITOR: **HAPPY HOLDEN**
(616) 741-9213; happy@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 365-1727; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

PRODUCTION MANAGER: **SHELLY STEIN**
shelly@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA, TOBEY MARSICOVETERE**

CREATIVE TECHNOLOGIST: **BRYSON MATTIES**

COVER: **SHELLY STEIN**

COVER IMAGE: **ADOBE STOCK © GECKO STUDIO**

PCB007 MAGAZINE

PCB007 MAGAZINE®
is published by IPC Publishing Group, Inc.
3000 Lakeside Dr., Suite 105N, Bannockburn, IL 60015

January 2023, Volume 13, Number 1
PCB007 MAGAZINE is published monthly
by IPC Publishing Group., Inc., dba I-Connect007

ADVERTISER INDEX


Problems solved!
PCB007 MAGAZINE
NOVEMBER 2022
DESIGN007 MAGAZINE
DECEMBER 2022
IPC APEX EXPO 2023 DESIGN CLASSES
Menu
DESIGN FOR
SMT007 MAGAZINE
JANUARY 2023
SUBSCRIBE NOW