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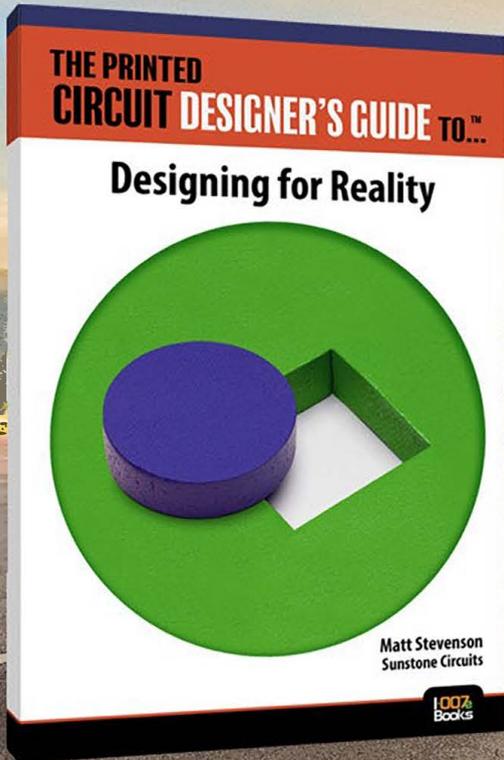
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The Impact of Advanced Packaging



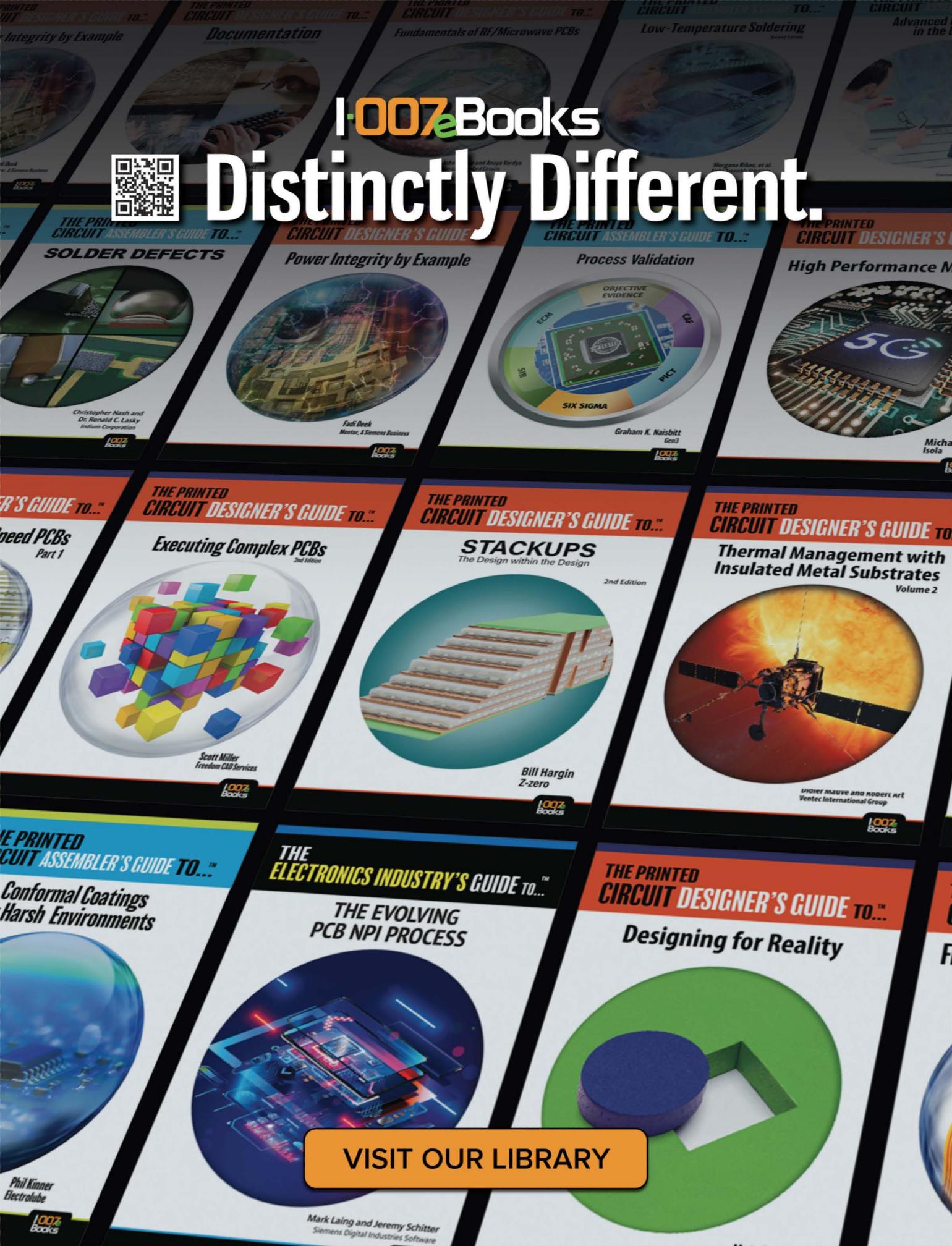
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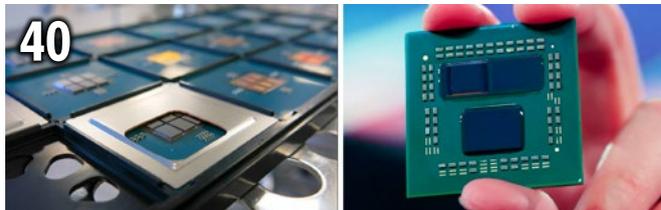
As semiconductor companies seek ways to prolong Moore’s Law, new advanced component packaging techniques are moving the boundaries between printed circuit fabrication and semiconductor fabrication. What will be the impact on the EMS industry? In this issue, we discuss how advanced packaging will change the structure of our industry.



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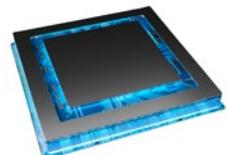
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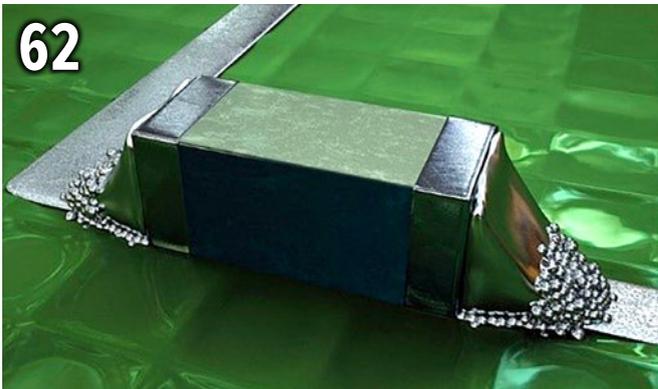
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Advanced Packaging

Nolan's Notes

by Nolan Johnson, I-CONNECT007

“Is multifurcated even a word? I hope so because that’s what it looks like in advanced packaging.” —Chuck Bauer

Chuck Bauer is well known as an expert in semiconductor packaging. He’s also the organizer of the SMTA Pan-Pacific Conference, so a chat over lunch with him is time well spent. He asked me that question over lunch as we were discussing how new packaging methods were making their way into industrial usage. Well, Chuck, according to multiple online dictionaries, multifurcated means to be multi-divided or forked off from a common source. Your observation is astute.

Advanced packaging is not new to our coverage. Over the past two years, we’ve written about the heterogenous integration roadmap (*PCB007 Magazine*, October 2020), as well as reported on the October 2022 IPC Advanced Packaging Symposium in Washington, D.C. This is a topic wherein printed circuit manufacturing and semiconductor manufacturing begin to converge.

As we prepped this issue for publication, I noted Taiwan-based TSMC announced its decision to increase its semiconductor investment in its new Arizona facility from \$12 billion to \$40 billion¹. Nearly simultaneously, Apple announced its inten-

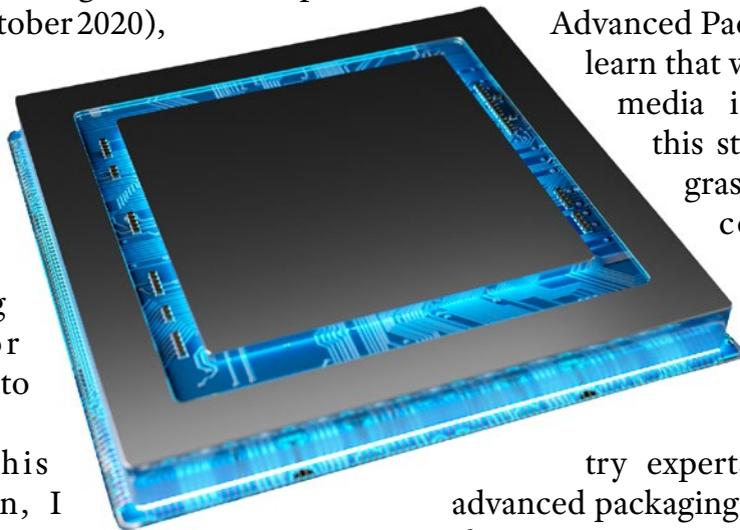
tion (along with AMD and NVIDIA) to use the U.S. manufactured chips in their products². This news makes for good public relations events, but there is still that nagging issue: a lack of packaging services in the U.S. to support those chips. As it stands, it seems that all the silicon from TSMC Arizona will still be shipped to Asia for packaging. Two trips across the Pacific, it seems to me, is a longer supply chain, not a shorter one. No wonder packaging capabilities are a common area of discussion when the topic is semiconductors.

Regular readers of the IPC Government Relations newsletter, as well as announcements from USPAE and PCBAA, are all too aware that there is plenty of news here. In fact, in a Dec. 16, 2022, article from IPC’s Chris

Mitchell titled “IPC Goes Deep on Advanced Packaging in 2022,” you

learn that while the mainstream media is actively covering this story, they don’t fully grasp the idea that semiconductors are the headwaters of the stream that leads to a working piece of technology in their home. Industry

experts will tell you that advanced packaging comprises R&D and manufacturing. So, outside of Asia, any conversation about advanced packaging necessarily includes discussion of the technology and the supply chain pretty much simultaneously. Nevertheless, all this dialogue in the news



simply shines another spotlight on advanced packaging and confirms our reasoning for a focus here.

Now, during my conversation with Chuck Bauer, he outlined all the different packaging technologies either entering the market, or currently under R&D development. It's not an either/or choice; in other words, multiple packaging choices are coming our way. This topic fits under the heterogeneous integration banner, of course—the technology for extending Moore's Law by allowing an IC system to be broken into multiple chips which are then combined to configure the final product. Hopefully we'll be able to coax Chuck into sharing more on upcoming packaging technologies in future issues.

It's one thing to design the packages; it's another thing altogether to do the packaging at production volumes. As is true for much of our leading-edge technology, the United States leads the way in development, but then outsources the humdrum manufacturing overseas. The goal of the CHIPS Act is to begin turning the tide. In February, NIST will begin accepting proposals for CHIPS Act programs. NIST has stated in presentations that it will be looking for and approving proposals that help bring additional capabilities to printed circuit boards and packaging alongside semiconductor build-out. Are you writing a proposal?

This is such a big topic that we've dedicated all three I-Connect007 January issues to advanced packaging. Just like the advent of surface mount, advanced packaging brings changes to both PCB fabrication and PCB assembly. Even still, we'll only be cracking the book open on this topic; there will be much more to cover over time.

For this issue of *SMT007 Magazine*, we contacted industry experts on packaging technologies to get their perspective on advanced packaging, and followed up with many of the participants in the IPC symposium, seeking a deeper dive into their presentations. We found enthusiastic voices willing to share their con-

cerns, solutions, and R&D work with you.

To this end, we open with an interview with IPC Chief Technologist Matt Kelly, who helps define advanced packaging. Getting a bit more specific, Intel's Tom Rucker describes how advanced packaging will allow for more configuration inside the package, Sam Sadri from QP Technologies shares how OCPP techniques allow new IC systems to be used in retrofit situations, and Tom Bergeron of Integra shares insight on how die prep will change with advances in packaging.

Equally important, MX2's Divyash Patel returns this month with more perspective on the upcoming CMMC milestone dates and why, if you haven't started certification yet, you may find yourself in a bind mid-year.

Finally, we're always grateful for our columnists including Jennie Hwang, Michael Ford, and Ron Lasky. Each provides such a unique perspective from their many years of professional experience. Jennie, for example, has been writing for I-Connect007 for more than two decades, and provides insight into how she made a pivotal switch from chemistry to engineering and the impact it has had.

As you'll see, Bauer's three-dollar word fits not only the advanced packaging subject matter, but with all our content, it's multi-directional stemming from the same initial source.

Happy New Year, and we hope to see you at IPC APEX EXPO 2023 in San Diego.

References

1. "TSMC triples Arizona chip plant investment, Biden hails project," by Steve Holland and Jane Lanhee Lee, Dec. 6, 2022, Reuters.
2. "Apple, NVIDIA to be first customers of TSMC Arizona chip plant," by Cheng Ting-Fang, Dec. 5, 2022, Nikkei Asia. **SMT007**



Nolan Johnson is managing editor of *SMT007 Magazine*. Nolan brings 30 years of career experience focused almost entirely on electronics design and manufacturing. To contact Johnson, [click here](#).

Creating a **Better World** Through Engineering

SMT Prospects and Perspectives

by Dr. Jennie S. Hwang, CEO, H-TECHNOLOGIES GROUP

What is the role of an engineer? In my definition, an engineer plays a crucial role in bridging science and society. In this spirit, The National Academies of Engineering (one of the triad Academies of The National Academy of Science, Engineering, and Medicine) recently initiated a video interview series with the theme, “Today’s Engineers—Creating a Better World.” I was invited to be one of several interviewees for the series. What follows are excerpts from that conversation.

Q *What inspired you to become an engineer?*

A I would not be where I am today without the encouragement and support of my family; at home, as the emphasis was on learn-

ing, excelling, and reaching for the stars. Education was of ultimate importance. During my formative years, I was fortunate to spend abundant time with my grandfather, who showered me with his intellect and wisdom. I am eternally grateful and cherish what I was given.

In a nutshell, I was not a kid who gravitated to one subject. During my school days, girls who pursued science and engineering were considered “smart.” I wanted to be smart, so I pursued science. At the same time, I was also intrigued by what felt like “the other side of the world,” namely fashion, dancing, and singing.

Three of my four academic degrees are in science: chemistry, liquid crystal science, and physical chemistry. The exciting part was moving into engineering. I was recruited by Case Western Reserve University as the first woman



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PhD candidate in Materials Science and Engineering. When I informed my chemistry dissertation professor at Columbia University about my plan to transition into engineering, he said, “Jennie, I have known so many female students who never finished their PhD once they left there. After you receive your PhD from there, you could do very well.” The rest is history.

The practice of the Engineering School at Case at the time was to have a master’s in engineering or physics as a prerequisite for PhD candidacy. However, my condition on coming to Case Engineering School was to go directly to the PhD without any delay. Having been a student in both chemistry and engineering, my experience was that chemistry curricula was quite different from engineering curricula; because of that, I was quite nervous. There was only one way to tackle that difficulty, and that was to study hard. Luckily, I was able to get top grades in all my graduate engineering courses.

With my background in chemistry, I found engineering to be extremely interesting, particularly in how engineering creates things. Looking back, I appreciate how tremendously beneficial my engineering training has been in every endeavor in my career of 40+ years, in everything from technology enterprise to manufacturing operations to business.

Q *How has your background strengthened your engineering experience?*

A My engineering training has facilitated my engagements in many areas, including in technology, manufacturing, and business.

To me, life is a progression of three stages. The first stage is schooling, when we prepare for the future by building a foundational education into a solid platform from which to grow.

The second stage is intellectual growth and “seasoning,” wherein we develop our

career, establish ourselves in our field, and learn how to contribute meaningfully to that field.

The third and final stage, which I consider the prime of my life, is a valuable time where we can use what we’ve learned to contribute the most to our field and the world, while continuing to learn and experience things. This is where I am now.

After completing formal education, deciding whether I wanted to go into academia or into industry was a huge and difficult decision. Once I decided to enter industry, my first job was with Lockheed Martin Corporation (then Martin Marietta Corporation), where I was swiftly put on the fast track toward an executive position. My time at Lockheed was such an intense learning journey; I was like a sponge. I started to truly appreciate the value of a solid education. I realized that the environment of one’s very first job is a pivotal component for future career development.

Working in an intellectually challenging environment is always a joyful and rewarding experience.



I often thought of my grandfather's teaching—the mindset to “reach for the stars.” That ethos guides me constantly in my search for wisdom. To that end, perhaps it's worth sharing something I learned recently. I made a point to attend the Berkshire Hathaway shareholders annual meeting in person to listen to the legend of legends, Warren Buffett, and to observe the dynamic of all the aspiring people present. During the Q&A session, attendees kept asking the same question, although they articulated that question in different ways. In essence, they wanted advice on what to invest in and, more importantly, how to succeed in life in this unprecedentedly uncertain time of high inflation and a draconian increase in the price of goods and services in our daily life, not to mention the widespread geopolitical issues. Mr. Buffett shared this wisdom:

Invest in yourself to gain rewards even when inflation bites. The abilities you have can't be taken away from you—they can't actually be inflated away from you. The best investment, by far, is anything that develops yourself, and that's not taxed at all. The best thing you can do is to be exceptionally good at something. You want to be the best at what you do—be the best engineer, the best doctor, the best dancer.

I thought this was truly powerful advice for all of us.

Some of this wisdom relates to women engineers. During the last four decades, as we know, women have made substantial strides in all professions, including engineering. Yet there is more progress to be made, especially in industry sectors such as the microelectronics/electronics industry. Women engineering professionals still need encouragement and support. For example, as of my recent professional development lectures to the industry, I've noticed that attendees are still predominately male professionals. I made the same observation in the 1990s, and today, in 2022, the same dynamic prevails.

Q *What does being an engineer mean to you?*

A I see engineering training as unique in a way that can be useful to all professions: as an engineering practitioner, a CEO leading a company, a venture capitalist investing in new business, or serving in the government.

As an engineer, the ultimate goal is to inspire by demonstrating results. In the grand scheme of things, being an engineer means creating for the betterment of society and human life; engineers need to enable, to do, and to lead. The ability to lead comes with the ability to inspire and get the best outcome in any environment or in any situation.

Leadership has great impact outcomes, from the war room to the boardroom to the engineering profession. There are different definitions and variations of leadership. I would define “leadership” as the ability to influence the outcome, not necessarily to command and control. In contrast to some opinions on this, I believe that leadership can be learned and nurtured. In any case, wanting to learn to be a better leader is always rewarding, especially for engineering professionals.

As an engineer, sharing knowledge and insights is a fulfilling experience. Outside my day job, I am invested in both writing and teaching; serving as an editorial columnist for two global industry magazines has been a meaningful endeavor to me. These publications disseminate timely information to readers who are mostly engineering-trained professionals. I have taken on this weekend employment for over 35 years. When it comes to speaking, I have delivered professional development courses, lectures, workshops, and webinars over the years to tens of thousands of engineers, researchers, and executives interested in continuing professional education in the workforce. This experience has allowed me to interface with engineering practitioners and executives, which helps me relate my engineering education to the workforce.

Teaching, like writing, has helped me develop and clarify my own thoughts; to that end, it is a self-fulfilling task as well.

I am happy to be helpful to younger women engineers; being helpful and being able to contribute is a good feeling.

In one of my speaking engagements, the president of the Society of Women Engineers (SWE) Cleveland wrote to me after the event:

Dear Dr. Hwang, on behalf of SWE, I would like you to know how much I appreciate your illuminating speech at the SWE. Because of this successful event, SWE has plans for expanding our mentor program. I was inspired by your journey to success. I plan to attend graduate school and your story of balancing professional accomplishments with a rewarding personal and family life encourages me to pursue all my dreams.

It is tremendously humbling to read letters like this from budding young women engineers.

Another experience that has been formative for me is my advisory capacity to the U.S. Defense Department's ManTech program. In the late 1980s, the Defense department's ManTech program set a goal to reduce cost and to enhance the reliability of electronics weapons on a national scale. The Army Materiel Command was searching for advice, not only academic scientific expertise but also manufacturing know-how. After my first book was published in 1989—in which I related microelectronics/electronics technology to manufacturing—I was invited to be an advisor to help advance that goal.

Looking back, it was an efficacious and satisfying task. Certainly, working in this capacity meant putting my engineering background to work. This is also another manifestation of the substantial role of engineering to national defense and security.

Distilling from my commencement speech at Ohio University, a few points on this topic are perhaps worth sharing:

- Keep a broad perspective to develop a world view—this is especially applicable to engineers.

- Always acquire new knowledge and skills, and learn fast.
- Meet a challenge head-on and go for creativity and innovation.
- Prepare to deliver more than what is expected in any task.
- Keep in mind that the best preparation for tomorrow is to do today's work well.
- When opportunity knocks on your door, you will be able to open the door. If a door does not exist, build one.
- Success is a journey—a long, steady journey, made of many, little, daily victories.
- Nothing can replace hard work. **SMT007**



Dr. Jennie S. Hwang—an international businesswoman and speaker and a business and technology advisor—is a pioneer and long-standing leader to SMT manufacturing since its inception as well as to the develop-

ment and implementation of lead-free electronics technology. Among her many awards and honors, she was inducted to the International Hall of Fame—Women in Technology, elected to the National Academy of Engineering, named an R&D Star to Watch, and received a YWCA Achievement Award. Having held senior executive positions with Lockheed Martin Corp., Sherwin Williams Co., and SCM Corp., she was the CEO of International Electronic Materials Corp. and is currently CEO of H-Technologies Group, providing business, technology, and manufacturing solutions. She has served on the board of Fortune-500 NYSE companies and civic and university boards; the Commerce Department's Export Council; the National Materials and Manufacturing Board; the NIST Assessment Board; as the chairman of the Assessment Board of DoD Army Research Laboratory and the chairman of the Assessment Board of Army Engineering Centers; and various national panels/committees and international leadership positions. She is the author of 600+ publications and several books and is a speaker and author on trade, business, education, and social issues. Her formal education includes four academic degrees, as well as the Harvard Business School Executive Program and Columbia University Corporate Governance Program. For more information, visit JennieHwang.com. To read past columns, [click here](#).

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The **Nuts** and **Bolts** of Advanced Packaging

Feature Interview by the I-Connect007 Editorial Team

The I-Connect007 Editorial Team asked IPC Chief Technologist Matt Kelly: Will you help us understand what advanced packaging means? This informative conversation touched on topics for both assembly and board fabrication. To that end, we will present this conversation in two parts. In this issue of *SMT007 Magazine*, Matt helps define not only what advanced packaging is, but the approach EMS companies must take when looking ahead. Think it's about just adding some new equipment and software? Think again. There are logistics, onboarding, and so much more.

To read an excerpt from this interview that was previously published in the November 2022 issue of *PCB007 Magazine*, [click here](#).

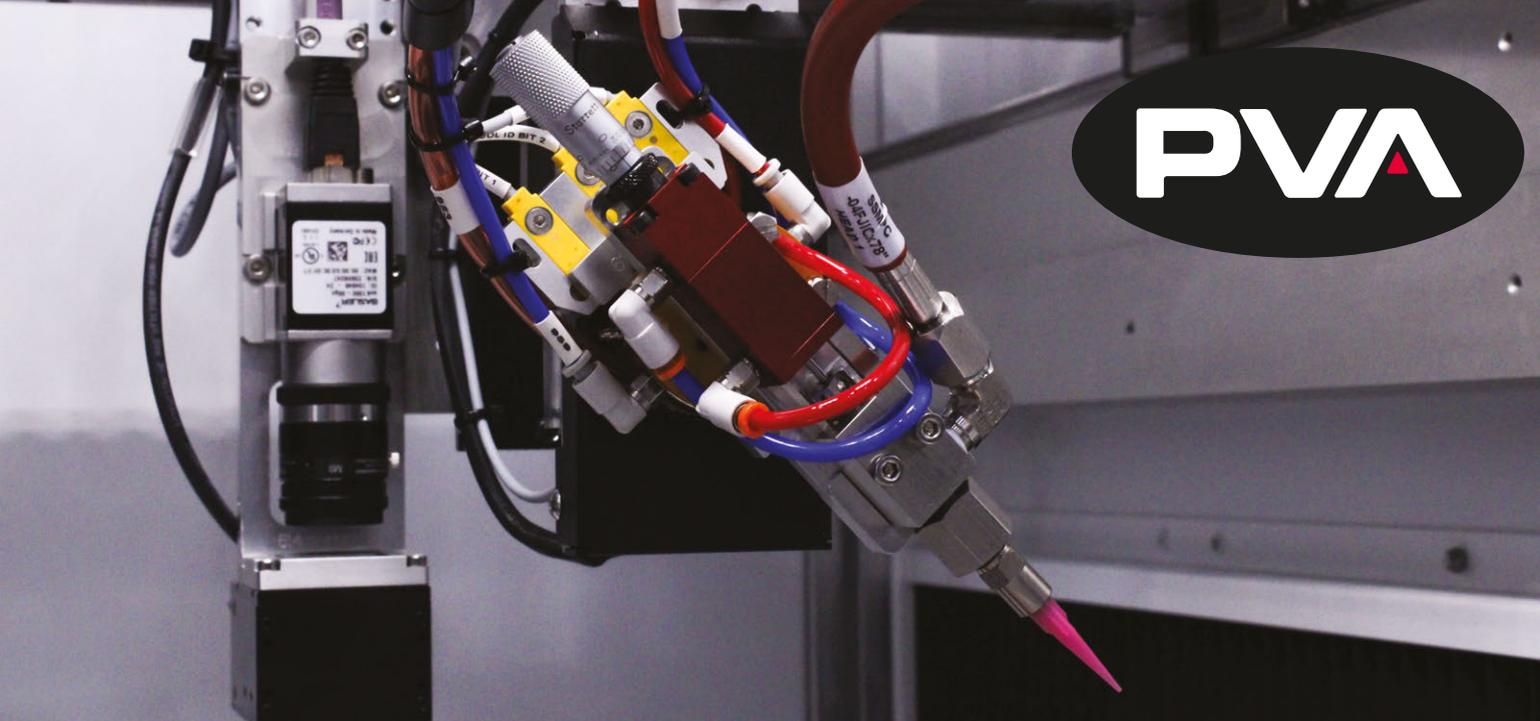
Nolan Johnson: Matt, I was on the exhibition floor at a technical conference recently and heard a lot of questions about advanced packaging: What is it, how does it apply, what does

it mean to EMS providers, etc.? Would you help to define and provide a framework about advanced packaging?

Matt Kelly: There are two terms to define. An advanced package is an electronic component; it's as simple as that. It has a few elements—it's comprised of a semiconductor chip (typically silicon) and an interposer and/or substrate—followed by interconnection and assembly of the component. Advanced packaging is the process by which these elements are integrated, assembled, and tested. Advanced packages represent a very specific class of electronic components called active devices. They are called active devices because they contain silicon that provides compute, memory, or other logical device functions. Advanced packaging is critical because the combination of performance, reliability, cost, and functionality that future consumers are demanding can only be

The PVA logo is displayed in white, bold, sans-serif capital letters within a black oval shape. The letter 'A' features a small red triangle at its top right corner.

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A close-up photograph of a PVA valve tool changer. The device is a complex assembly of metal, plastic, and electrical components. It features a red cylindrical body, a yellow top section, and various colored hoses (red, blue, white) connected to it. A pink-tipped nozzle is visible at the bottom. The background shows a blurred industrial setting.

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Matt Kelly

met by integrating silicon chips through an advanced packaging process.

Keep in mind this is just one of many different components in a system. While these components are important—they're the brain of a system—they're still just one of many different component types. Advanced packaging is a very specific component type. But what types of components are they? These advanced packages have different functions, the first of which is compute. It's the Intel chip inside your laptop (CPU), graphics accelerators (GPU), AI-based neuro-network chips (NPU). It's also the solid-state memory (DRAM, NVRAM, NAND Flash) within your phones and computers. These packages can also serve as sensors, analog, mixed signal, and system integration functions. Basically, they are actively doing something within the circuit design. Those are the main functions of an advanced package.

There's also a difference between definitions of advanced packaging in the past, what it means today, and what it will mean in the future. For example, for at least 50 years, there's been an active type of component called monolithic silicon, a single chip that is mounted to a substrate and then packaged into a component.

A class of those are called multi-chip modules (MCM) and have been in use for decades.

As we move forward with the monolithic silicon, the idea of Moore's Law becomes less economically viable and advanced packaging is morphing.

For example, when you think about a circuit card from the past, you typically had a compute chip and DRAM (memory banks), which were two different things connected on a printed circuit board. Those are now merging using chiplet-based heterogeneous integration architectures that are now integrating compute and high bandwidth memory (HBM) together within the same electronic package. The result is faster speeds and reduced latencies within a single component package. The resurgence in advanced packaging is driving increased functionality, performance, and speeds within a single device.

Johnson: Increased functionality, increased speed, and an overall smaller package means leaving more real estate available to further integrate more things.

Kelly: Absolutely. For example, if you look at images of a recent Apple Watch teardown, it's unbelievable what can be accomplished in these small spaces. There are numerous small chips performing many functions within a very small area. Next generation designs continue driving miniaturization, increased functionality, and speeds. On the downside, these configurations are power hungry, meaning there are more power and thermal needs—thus challenges—that need to be addressed with these architectures.

How Does This Affect EMS Companies?

Johnson: For an EMS company, your job is to reliably put these components onto boards. While that doesn't fundamentally change, these packages will change the skill set needed to do the work. How will this affect the EMS companies?

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Kelly: From a receiving standpoint, an EMS provider will need to increase their incoming quality inspection procedures because these are brand new parts. How are they receiving them and what is the quality? These are the primary needs—improved logistics and warehousing on the front end.

In terms of assembly, there are some things to consider. First, there is the printing of very small, uniform deposits of solder paste, so you're not having opens or other defects. The printing of these can or will change whether they're big or small parts. In terms of reflow, you need an understanding of what these parts can handle. Hopefully, MSL values and other things are not changing these parts so that we don't go back to popcorning problems and inner layer, first level delamination issues of the parts. That will likely be covered as part of the component qualification process before the part comes in; next generation incoming inspection techniques continue to evolve.

Can AOI and AXI tools inspect for defects of these parts when the IO count is high? With these packages, you'll see more silicon—more chiplets. When you look at X-ray, you're looking through the part. When you're in that center of the die, you can't really see what's underneath because the die is dominating. When your whole package is covered with die, you can't necessarily see the bottom balls. Head-in-pillow (HIP) detection comes to mind because HIP will be a bigger problem here as warpage fights us.

As more chips are placed in increasingly smaller areas, increased power densities are driving new thermal solutions to manage heat dissipation. Advanced heat sink structures, forced air, and active liquid cooling techniques will need to be developed for the most challenging advanced packages. Increased usage of thermal interface materials (TIMs) is also expected.

Test is the last area, and it's something often overlooked because it's one of the last areas in the process. We will be doing test in different

ways. The historical ICT/FCT flow may not work anymore because with miniaturization and limited real estate, you don't have much room for pin-outs for flying probe test or in-circuit test beds—bed of nails—where you want them to be. You must look at different test approaches moving forward. There will be higher demand on boundary scan, more software-based types of tests, and the like.

There's also the metrology needs for qualification or failure analysis within the lab. For example, being able to examine second-level interconnects with computed tomography (CT) X-ray in a timely manner will be quite a challenge from an I/O standpoint. You can imagine looking for subtle voiding defects in a 10,000 I/O component; it's like looking for a needle in a haystack.

You can imagine looking for subtle voiding defects in a 10,000 I/O component; it's like looking for a needle in a haystack.

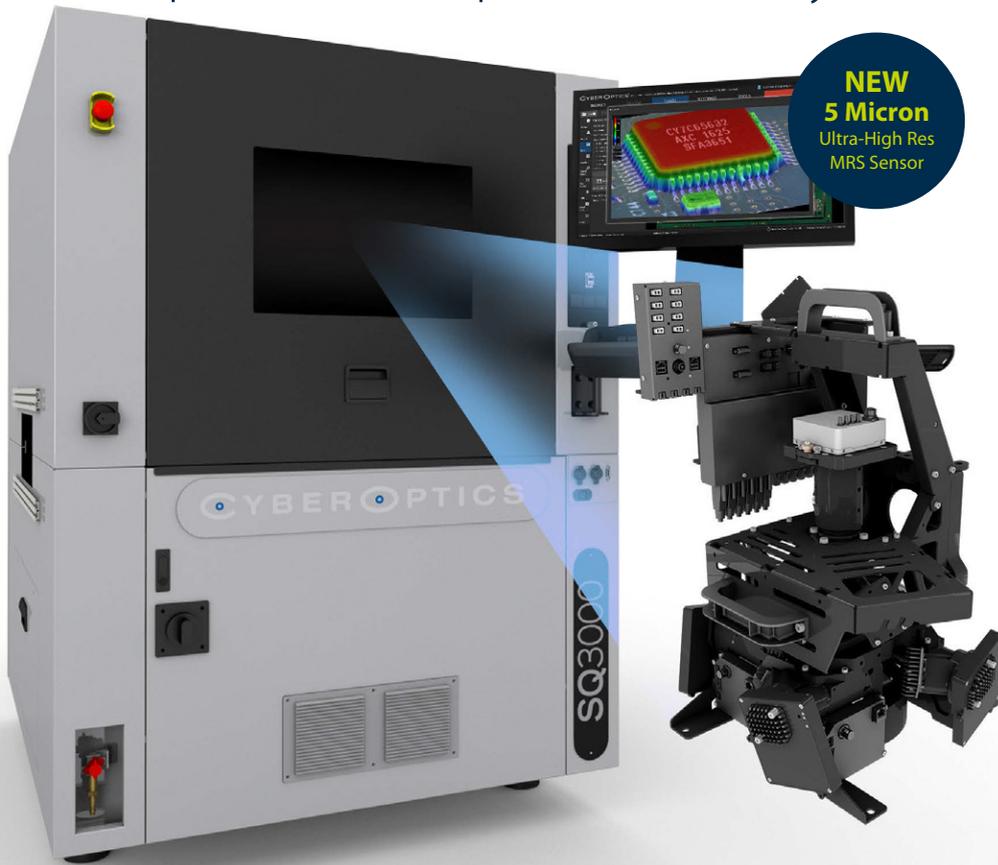
Why It's So Important

Johnson: Why is advanced packaging so important to IPC right now?

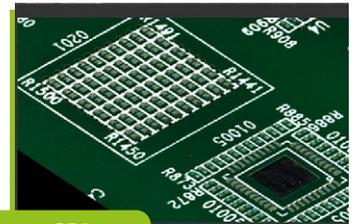
Kelly: IPC is expanding its mission. For the past 50 to 60 years, we have focused on being a printed circuit board and assembly focused organization. IC substrate and HDI PCB technology lines are blurring. With IPC's extensive background in printed circuit boards, it's a natural extension to support the changes that are underway across the industry. Likewise, while there are differences, there are also many similarities between EMS second-level assem-

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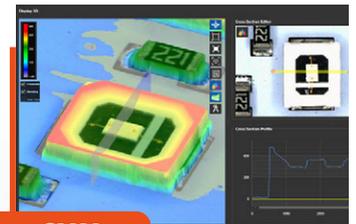
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bly and OSAT first-level component assembly. With IPC's long history in electronics assembly, it's a natural extension to support OSAT component-level assembly. Our members have been asking for increased engagement in advanced packaging and IPC is actively expanding support of advanced packaging in the areas of IC substrates and OSAT packaging assembly and test.

With IPC's extensive background in printed circuit boards, it's a natural extension to support the changes that are underway across the industry.

CHIPS Act Funding

Barry Matties: EMS providers will need to accommodate the changes and trends in the market. What should they be thinking about and what can we say that will help them learn along this journey?

Happy Holden: How do you take an advanced surface mount assembly facility and make it an OSAT facility? How do you take an advanced printed circuit fab facility and make it an advanced substrate facility?

Kelly: I believe the question is about whether an existing PCB fabricator can transform itself to produce substrates, and what an EMS provider can do to transform itself into an OSAT assembler. Is that the question?

Holden: One may evolve from the other, but they're not the same whatsoever. In North America, too many fabricators seem dominated by the perspective of, "Why should we

change?" But if you look at the fabs embracing advanced packaging, they're likely facing two problems: Where do I get financing and how do I convince young engineers to work for me? This will take a lot of engineering horsepower because the IC fabs are out recruiting the same engineers.

Kelly: One specific example for a PCB fab going to an IC substrate is environmental cleanliness. For yield, you need to be installing class 10,000 clean rooms. While there are similarities in equipment and tool sets, those quality control measures are paramount for quality and yield. Number one, then, is significantly increased process control.

Holden: Almost to a level of passion.

Kelly: Actually to levels that might make people faint. Qualification protocols will be much more stringent. Statistics will feed into both Factory of the Future and Industry 4.0 techniques. If we were to do some of this packaging in North America with qualification efficiency, you need the statistical knowhow—not just by the systems, but you need an understanding of what these numbers and dashboards mean. You need master black belts trained in design of experiments (DOX) and statistical methods. That is what fuels quality, but on the F2 side, data continues to be a theme because you need it to show whether you're in or out of spec, as well for automation for efficiency.

I learned long ago from an IBM fellow that when you're dissecting these problems, you need to think about the what and the how. Factory of the Future is the how, and advanced packaging is the what. If we can connect these two, that might be where we start to fully utilize Factory of the Future.

Matties: Matt, do you have any final thoughts?

Kelly: It's been said by many that this is a special point in time, a once-in-a-generation opportu-



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nity. Big changes are coming from semiconductor companies. First, I would say that if CHIPS funding didn't come through, everyone would probably just say, "Okay, we're done. It's a global supply chain, we're too late, so we continue and that's how it will be. We'll have to manage that." But this is an opportunity for companies to understand what's happening. If you think that everything is the same, then unfortunately, you're not paying attention because I would argue there's more happening now than I've ever seen in my entire career.

There are opportunities for companies to transform, whether that will be getting into new market segments like substrates and OSAT, doing a better job of receiving those parts, or doing a better job of producing them as an EMS provider or PCB fab. There are opportunities for implementing new ways of working, such as with Factory of the Future. There are not very many times in your career when you will see large investments as we're

seeing today, and I encourage companies to take a due diligence and exploratory perspective on this.

Don't jump in and think everything is great and easy, but if there really is a need for more regional capabilities—whether it's in Europe or North America—we shouldn't lose or miss this opportunity. As this money is deployed, there's a five-year window in which the government and others will make a cost/benefit analysis.

If we can show progress as an industry, this is not just a one and done; we could enter more discussions about moving forward. If we mess this up, then we will have lost an opportunity to make a difference.

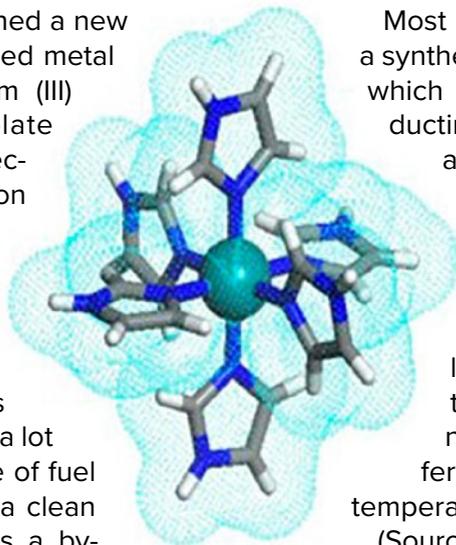
Johnson: Matt, thank you for your comments today. It has really helped to clarify what advanced packaging is about and steps that can be taken to move forward.

Kelly: You're welcome, glad to help. **SMT007**

Novel Multi-Proton Carrier Complex as Efficient Proton Conductor at High Temperatures

Fuel cells often fall short when it comes to operating at temperatures beyond 100°C owing to their dependence on water as a proton conduction medium. To overcome this issue, a team of researchers from Japan designed a new hydrogen-bonded starburst-shaped metal complex consisting of ruthenium (III) ion and six imidazole-imidazolate groups. The resulting single molecular crystal shows excellent proton conductivity even at temperatures as high as 180°C and as low as -70°C.

As the world is moving toward more environment-friendly and sustainable sources of energy, fuel cells are receiving a lot of attention. The main advantage of fuel cells is that they use hydrogen, a clean fuel, and produce only water as a by-



product while generating electricity. This new and clean source of electricity could replace conventional lithium-ion batteries, which currently power all modern electronic devices.

Most fuel cells use a Nafion membrane—a synthetic polymer-based ionic membrane—which serve as a water-based proton conducting solid electrolyte. The use of water as a proton conduction medium, however, creates a major drawback for the fuel cell, namely the inability to function properly at temperatures above 100°C, the temperature at which water starts to boil, leading to a drop in proton conductivity. Therefore, there is a need for new proton conductors that can transfer protons efficiently even at such high temperatures.

(Source: Tokyo University of Science)

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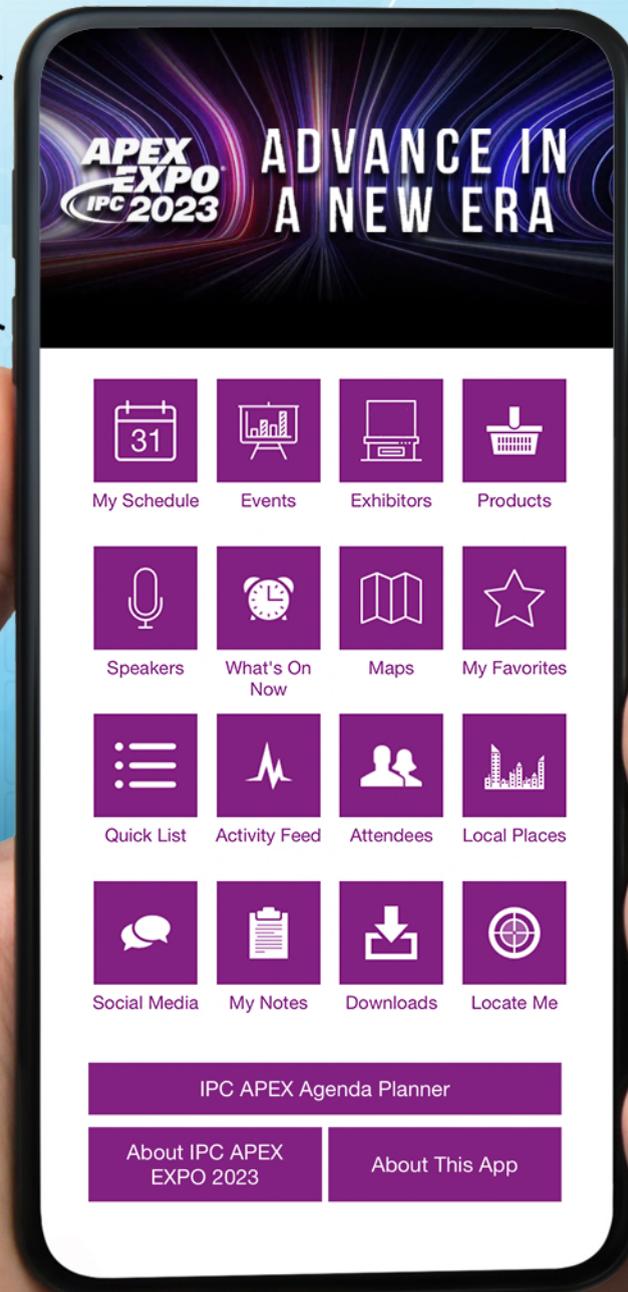
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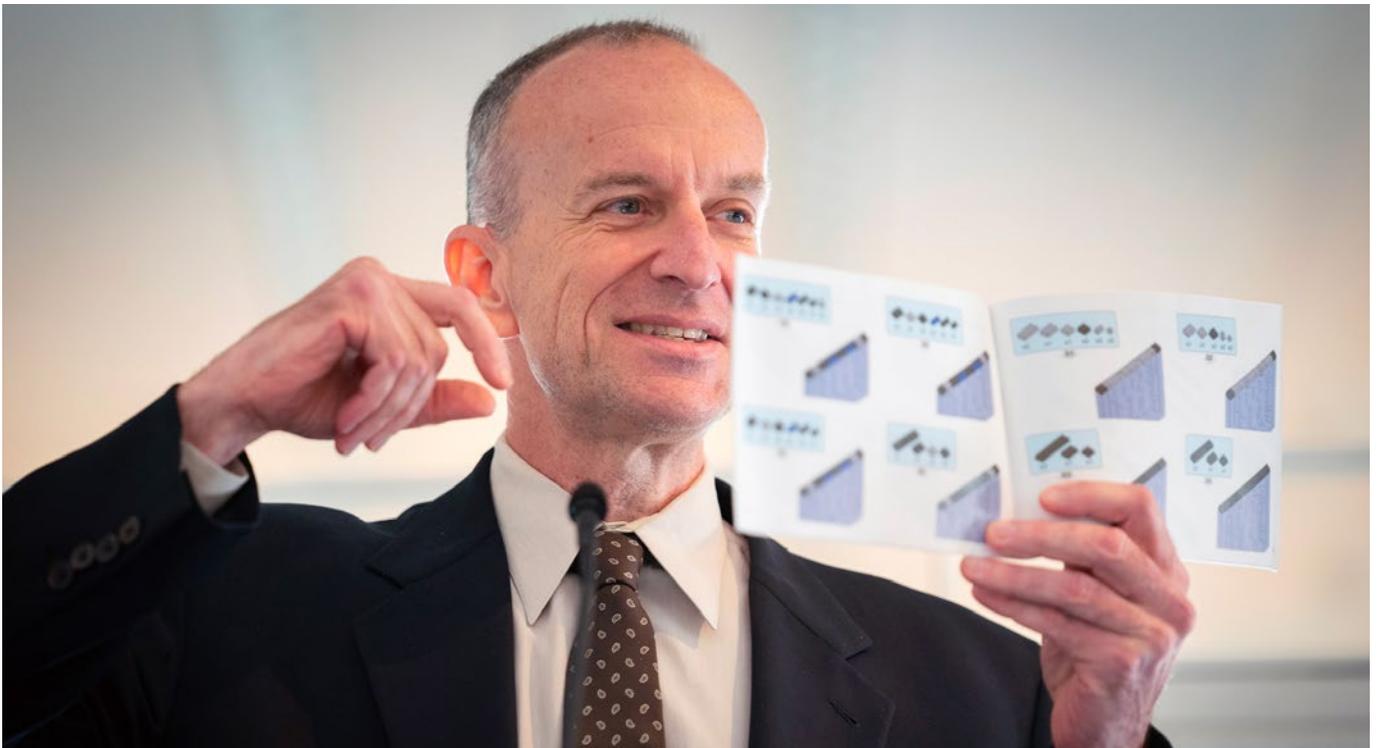


Photo credit: John Harrington

Advanced Packaging Beyond the Zetabyte Era

Feature Article by Tom Rucker

INTEL

As the industry continues to aggressively pursue Moore's Law, the technology envelope and solution space has grown to include packaging. Historically, the role of the package was to protect the die from the environment and to scale the small geometries of the die to the significantly larger pitches of the system board. Moving forward, the package is also being used to interconnect multiple die in one unit. This facilitates assembling die from different technology nodes into overall smaller form factors with higher performance. The industry refers to this approach generally as "advanced packaging," or heterogeneous 3D integration. Across market segments, from computing to communications to defense, products that use advanced packaging technologies are becoming more prevalent.

The importance of packaging technology is reflected in its prominent inclusion in the U.S. CHIPS and Science Act. The law establishes the National Advanced Packaging Manufacturing Program (NAPMP), which seeks to "strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem." These provisions demonstrate that the importance of packaging technologies has spread beyond the technology industry into the realm of policymaking. Programs funded in the CHIPS Act ensure that the U.S. will continue to drive important advances in packaging technologies, supporting efforts to rebalance global chipmaking capability and capacity. This onshoring will both strengthen the overall supply chain and ensure the fulfillment of critical domestic market require-

Free Checklist: Vulnerability Assessment

The Checklist helps CEOs understand what to expect from their Vulnerability Scan, so they can be prepared to better understand risk and make necessary changes. Topics include:

- ✓ The CEO's role before, during and after a Vulnerability Scan.
- ✓ Baseline cybersecurity tenets that CEOs need to be confident in.
- ✓ Questions CEOs should be asking to understand and justify the risk associated with each of the findings.
- ✓ How CEOs can communicate the results of a Vulnerability Scan.

THE COMPLETE SECURITY VULNERABILITY SCAN CHECKLIST

What is a Vulnerability?

- ✓ A design flaw or misconfiguration which makes a network (or a host in a network) susceptible to malicious attacks from local or remote users. (Risk varies from disclosing information to a total compromise of a network).

Where Does a Vulnerability Exist?

- ✓ Vulnerabilities exist in: Firewalls, Servers (Email, Application, File Transfer Protocol (FTP), etc.), or Operating Systems.

Vulnerability Scan Process

- 1 - **IDENTIFY** by running a scan
- 2 - **ANALYZE** by reviewing report results
- 3 - **RISK ASSESS** by reviewing severities by level
- 4 - **REMEDiate** by acting to resolve vulnerabilities

What is a Vulnerability?

- ✓ A design flaw or misconfiguration which

ments. The funding will allow the U.S. to accelerate the development of innovative packaging technologies that will support new revolutionary and evolutionary end products. The Department of Commerce is currently working on the details of the NAPMP implementation plan, with more details expected in early 2023.

Delivering on the goals set by the CHIPS Act requires development in a wide variety of technical domains and the integration of these diverse building blocks. The processing components can be separated into three general functional areas: wafer-, panel-, and unit-level processing.

Delivering on the goals set by the CHIPS Act requires development in a wide variety of technical domains and the integration of these diverse building blocks.

Wafer processing steps, which follow the manufacturing flow of building and interconnecting the transistors on a die, involves electrically connecting multiple die. These die can be side by side and connected through a polymer/metallization structure, or they can be stacked on top of each other with connections composed of solder or copper. A multitude of architectures have been developed by the industry, each optimized for the final product performance and cost targets. These wafer-based processing steps take advantage of the tools and extensive experience of the wafer fabrication industry.

Panel-based processing steps support a variety of use cases, from building substrates (packages) where one die is attached, to being an alternate approach for interconnect-

ing multiple die in the same unit through different process flows. Based on package body size, die count, and total die area, panel-based processing can offer a lower-cost alternative to wafer-based processing. Panel-based processing benefits from higher panel utilization for larger package sizes relative to wafers and a higher number of units per panel. Like the economies of scale the semiconductor industry achieved in the transition from 200 mm to 300 mm wafers, panel processing achieves equivalent benefit over wafer processing. In addition, advances in panel-based technologies and materials enable unique solutions for a variety of market segments such as communications and computation.

However, there are challenges that need to be overcome to proliferate panel-based processing. For example, the materials, process equipment, and facilities to build advanced substrates is becoming closer to wafer fab equipment, and so equipment development is needed. The smaller geometries of panel-based processing require clean environments, advanced lithography, and higher performance dielectrics, among other materials. Panel handling needs to improve to increase line yield. These capabilities can be applied to other industries such as display and board manufacturing, which further incentivizes scaling these technologies to the level required to overcome the unique defect, quality, and reliability challenges facing the panel testing industry. Packaging provisions from the CHIPS Act may accelerate these efforts.

Unit-based processing can be viewed as the continued evolution of what is commonly referred to as assembly and test. This manufacturing stage also requires technical advances to support higher thermal loads and tighter pitches.

Many products require processing using all three advanced flows—wafer, panel, and unit. For example, the Intel® Data Center GPU Max Series product has approximately 100 billion transistors in a 47 tiles/die package. These



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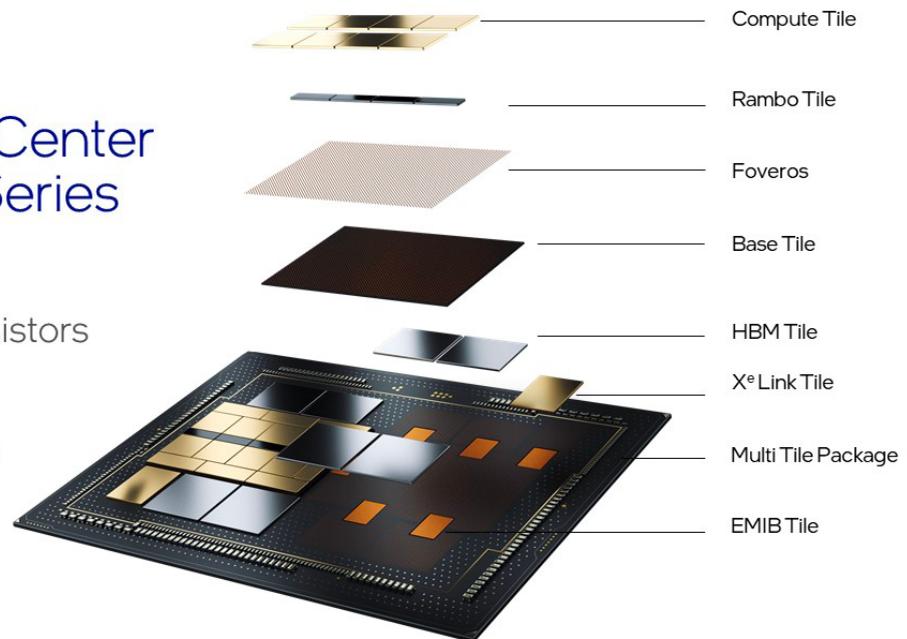


Figure 1: The Intel® Data Center GPU Max Series, an example of a complex advanced package product.

products feature multiple advanced packaging technologies, including die stacked on different die, die embedded into the package, multiple die stacks attached to the package, and an advanced thermal solution. This “mix and match” architecture gives product designers the flexibility to deliver the best products.

Across all these manufacturing stages, demonstrating economic viability for domestic manufacturing will require dramatic changes to how factories and process tools are designed. Output per tool must improve significantly, while labor content needs to decrease significantly—each by an order of magnitude. This represents both a challenge and an opportunity for the industry and should become an area of focus for programs launched under the CHIPS Act.

Ensuring the final packaged products meet the stringent quality and defect levels requires significant testing—both in-line and at end of line. With current products requiring 100 billion transistors and projections calling for 1-trillion-transistor products around 2030, the

challenge is large. These products have tight performance targets and must be able to perform under broad use conditions.

Yield management with multiple die in one unit requires performing high levels of test coverage and defect management within the process flow. The cost impact of yield loss is significant. Testing for advanced packaging has the unique characteristic of needing to test and verify the performance and reliability of all die ahead of package assembly. Rather than simply sorting wafers to look for gross fab defects, die testing needs to test for both fab defects and some performance characteristics; further, this process needs to stress not only individual die, but stacks of die as well. Post-assembly, devices must be tested for assembly defects, stressed, classified, and run at the system level for optimal performance characterization, as well as quality and reliability verification.

In addition, if the final unit is composed of mixed technology node components such as digital, analog, optical, and/or MEMs, the testing methodology is further complicated

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by different test requirements and capabilities needed for each subcomponent, in addition to verifying that the complete, integrated units perform to specifications. A further challenge with advanced packaging is determining the optimum locations in the process flow for the different testing steps, to balance costs and yield management, as well as the scalability of the test and measurement solutions themselves.

The world is moving to zeta-scale computing, driven by the exponential growth of data that needs to be collected, stored, and analyzed. As this trend continues, advanced packaging becomes a requirement to meet the performance and dimensional requirements of

these systems. Breakthrough technologies across design and manufacturing are needed to successfully deliver innovative products and capabilities. Innovation in computing products requires major advances in advanced packaging over the next few years, a development that promises to usher in a new and exciting era of opportunity for the industry. **SMT007**



Tom Rucker is vice president of technology development at Intel.

NIST Resources for CHIPS Act Participants

Article by Nolan Johnson

At the recent IPC Advanced Packaging Symposium, Dr. Frank W. Gayle, deputy director of the Advanced Manufacturing National Program Office, an interagency team with core staff hosted at the U.S. National Institute of Standards and Technology (NIST), gave a presentation on the work NIST has recently undertaken in support of both the semiconductor and R&D sectors, and the CHIPS and Science Act.

In Gayle's presentation, he said the vision for the CHIPS and Science Act (also known as the CHIPS Act) is to develop and preserve three key areas: economic security, national security, and future innovation.

He emphasized that the CHIPS Act is about more than just the semiconductor chips, reserving an entire slide for that point alone. While NIST acknowledges that the U.S. holds an impressive 85% stake in the semiconductor design market, only 3% of the global packaging industry resides within the U.S. (Figure 1).



Figure 1: The U.S. has a majority stake in semiconductor design but trails behind the rest of the world in both manufacturing and packaging¹.

In support of this mission, Gayle drew attention to a series of resources that are now available on NIST.gov:

- **Metrology and Standards**

“Strategic Opportunities for U.S. Semiconductor Manufacturing: Facilitating U.S. Leadership and Competitiveness through Advancements in Measurements and Standards,” August 2022.

- **Stakeholder Input on CHIPS Act**

“Incentives, Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry: Summary of Responses to Request for Information,” August 2022.

- **Commerce Strategy for Implementation**

“A Strategy for the CHIPS for America Fund,” September 2022.

- **Semiconductor Supply Chain RFI Findings**

“Results from Semiconductor Supply Chain Request for Information,” January 2022.

Gayle concluded that the Incentives Program application process will be announced in February 2023 with funding proposals considered on a rolling basis. Learn more about the CHIPS Act at [nist.gov](https://www.nist.gov).

References

1. Data courtesy of the U.S. Department of Defense and IPC.

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An Unblinkered View

Smart Factory Insights

by Michael Ford, AEGIS SOFTWARE

For many, blindly going where no one has gone before is just a normal day in the factory. As new products are introduced, manufacturing is expected to provide perfect products based primarily on assumptions and reverse engineering. Without accurate and complete product data, there can be no engineering automation, which results in a complete waste of energy. This should no longer be acceptable in the industry. A lack of adequate contextualizing of product information creates unnecessary cost and risk in manufacturing operations, thereby limiting competitiveness. What's behind the industry's reluctance to change on this matter?

The key reason relates to security. Releasing full design data to manufacturing exposes valuable intellectual property (IP), which could make its way to competitors. The current paradigm wherein we trade performance for security needs to be destroyed if we, as an indus-

try, will ever succeed in our business goals. Recently, performance and security considerations have become more urgent and significant, such that we will soon reach a crucial tipping point. On one side, there is a clear expectation for assembly manufacturing to be as efficient as possible. Operational exceptions, compromises, and defect rates that were once acceptable are no longer viable in a successful assembly operation; these include general wastes of time, resources, and investment, including delayed deliveries and poor quality. Any activity that invokes waste of any kind is unacceptable. Perfection is paramount.

Digital manufacturing technology has now come of age, making automated processing an integral component of manufacturing engineering software. These new processes are meant to eliminate the needless, repetitive, and error-prone conventional methods that have long guided the industry's decision-mak-



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ing. Product design data has been fully digitized, comprising 3D-CAD data, bills of materials (BOMs), and PCB layouts and specifications for electronics assembly. From a layperson's perspective, product data simply needs to be converted into instructions needed for the entire assembly operation to take place. Instructions are needed for automated processes, such as those assigned to machines and robots, as well as for human assembly operators; all this is derived from product data. With product design tools and ERP systems already computerized, why is so much work still done manually?

Today, there are many more product variants, even customized product variants that require tailoring assembly at key operations.

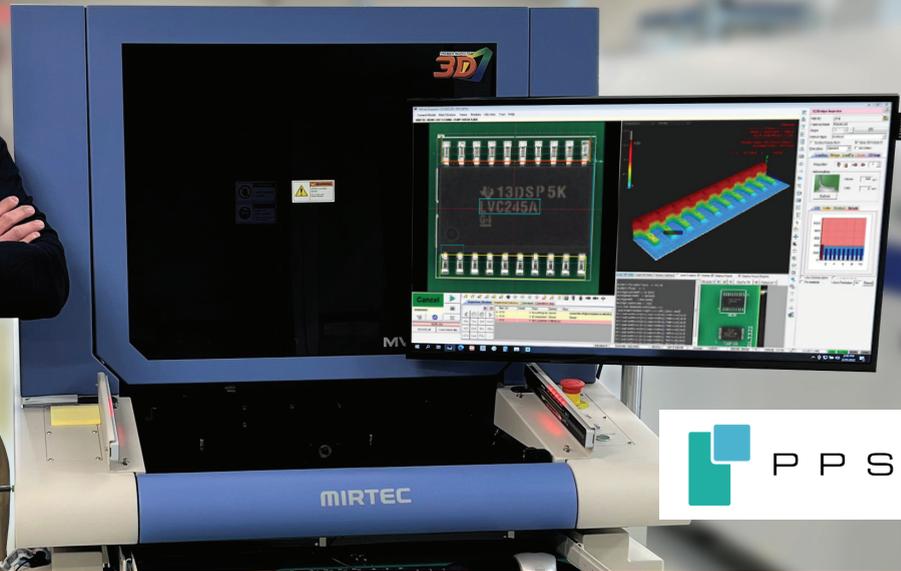
Back in the days of high volumes and limited product mix, manually compiling data worked fine. Today, there are many more product variants, even customized product variants that require tailoring assembly at key operations. For example, each core chassis in a mobile phone has many thousands of active variants. At the other extreme, variability is opened, such as the height of a bespoke piece of furniture, or the dimensions of a window blind. Humans can handle all this variation, but it takes time; a lack of automation coupled with an exponential increase in degree of variation makes mistakes inevitable. In addition, people with essential skills are now leaving the manufacturing industry, and there's little motivation for new people to take on these stressful and repetitive roles for so little reward.

Removing low-level and repetitive critical

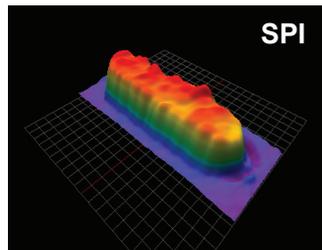
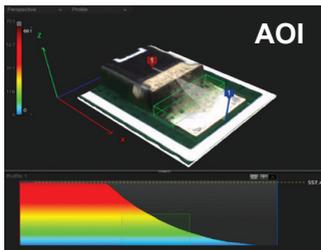
actions from manufacturing engineering is essential. With digital product data, manufacturing engineering tools now have the opportunity to elevate engineering's contributions. Although digital product design information has been available for some time, few operations have set up the data flows necessary to handle it. Very few tools on the market have the built-in capability to use such data as their core driver, yet digital manufacturing engineering tools offer innumerable benefits, including the ability to quickly expose any exceptions or specialist requirements inherent in a design via the enhanced visibility provided by digital design data. New digital best practices make it possible to automate processes associated with an individual product, including assigning product configurations, selecting materials, and creating work instructions. Automating these processes helps limit operational mistakes, defects, and delays.

This effect of automation on the operation is not restricted to new products. Digital manufacturing engineering allows risk-free, on-the-fly production allocation; these processes now take seconds as opposed to days. Engineering is now in the driver's seat, replacing the individual who, until now, has blindly pushed the car along the road. Contextualizing designs with data collected from the shop floor enables immediate decision-making, which improves operational effectiveness overall; low-level decisions are now made automatically. And because every data point is precisely considered in the context of the design, variant, material, process, timing, etc., overall value increases. This all sounds great, doesn't it?

However, most companies are not using digital design data to automate their manufacturing engineering processes. Company profitability and survivability are being compromised in lieu of IP security. Protecting IP is not new. The latest products from competitors are being physically torn down and their features, functions, and technologies analyzed in labs run by all the major product design teams.



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A competitor's design data can now be reverse engineered in minutes. The risk of cloned, compromised, and even counterfeit products has become a major concern for the industry.

While these concerns are legitimate, everything comes down to trust between the company owning the product IP and the companies involved in the manufacturing. Such companies are generally diligent about providing contracts and agreements that protect the IP of their customers. It is extremely difficult, however, to ensure that every person with access to that data will refrain from leaking it to the many individuals and companies offering significant incentives to do so. Dealing with sensitive data requires mechanisms that ensure minimum risk and access to a minimum number of people. Engineering automation eliminates the need for a person to have access to the design data itself; instead, they need only have access to the various abstracts created from it. Technologies available today can ensure that holistic design data never leaves the security of its owner's servers. Authenticated engineering solutions allow secure, selective access on demand, with no need to store core design data locally. Trust is earned through long-term relationships, but as trusted people are always leaving companies, trust can't always be a part of the equation.

Most companies are now digitally transforming their operations in ways that they consider "safe" for their business. But these changes need to be made as part of an overarching strat-

egy, not as a piecemeal, step-by-step process meant to preserve the balance between performance and security. Sharing design data that is then processed manually offers few benefits, especially because the increased risk of IP leakage is high. In contrast, modern digital manu-

facturing engineering tools prevent people from manipulating raw design data. Automating low-level jobs means that engineers can work at an abstracted layer from the data. Any design data needed by machines or in work instructions is thereby isolated from the main design IP, which has very little value when it can't be painstakingly reverse engineered.

With appropriate IT security practices in place, automating manufacturing engineering creates an environment in which products can be reliably made with reduced exceptions and defects. These systems are also very safe from threats to IP leakage, since they can designate or prevent access to core design data as necessary. Trustworthy companies who want their digital transformation projects to remain competitive need to consider updating the entirety of their data flow and automation practices so as not to get caught in this "blind leading the blind" trap of modern information technology. **SMT007**



Michael Ford is the senior director of emerging industry strategy for Aegis Software. To read past columns, [click here](#).



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Key Findings From Semiconductor Fabrication Research

In November 2021, IPC published an industry report titled, “North American Advanced Packaging Ecosystem Gap Assessment: Critical Systems, Capability, Capacity Analysis and Recommendations.” This report, issued by Matt Kelly, IPC chief technologist, and Jan Vardaman, president of TechSearch International, takes a detailed look at the technologies and the infrastructure required for advanced packaging in both the current state as well as potential future states.

This excerpt from the report describes some of the semiconductor fabrication issues, both economic and technical, that go into creating that finished package used to assemble the printed circuit subassembly. The entire report can be [downloaded here](#).

Semiconductor Fab and Foundry Global Mapping

Chip plants run 24 hours a day, seven days a week. They do that for one reason: cost. Building an entry-level factory that produces

50,000 wafers per month costs about \$15 billion. Most of this is spent on specialized equipment—a market that exceeded \$60 billion in sales for the first time in 2020. Three companies—Intel, Samsung and TSMC—account for most of this investment. Their factories are more advanced and cost over \$20 billion each. In 2021, TSMC will spend as much as \$28 billion on new plants and equipment. Compare that to the U.S. government’s attempt to pass a bill supporting domestic chip production. This legislation would offer just \$50 billion over five years—only two-thirds of which is targeted at boosting near-term chip production.

Once you spend all that money building giant facilities, they become obsolete in five years or less. To avoid losing money, chipmakers must generate \$3 billion in profit from each plant. But now only the biggest companies, in particular the top three that combined generated \$188 billion in revenue last year, can afford to build multiple plants.



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The ability to build multiple plants engaged in high-volume manufacturing is important; the more a company manufactures, the better they get at it. Yield—the percentage of chips that aren’t discarded—is the key measure. Anything less than 90% is a problem. But chipmakers only exceed that level by learning expensive lessons repeatedly and building on that knowledge.

The brutal economics of the industry mean fewer companies can afford to keep up. Most of the roughly 14 billion smartphone processors shipped each year are made by TSMC. Intel has 80% of the market for computer processors. Samsung dominates in memory chips. For everyone else, including many new and aspiring companies in China, it’s not easy to break in. (Source: Bloomberg)

- Many NA fabs already, expanding foundry capability in 2024 (TSMC, Intl, Samsung)—fabless model

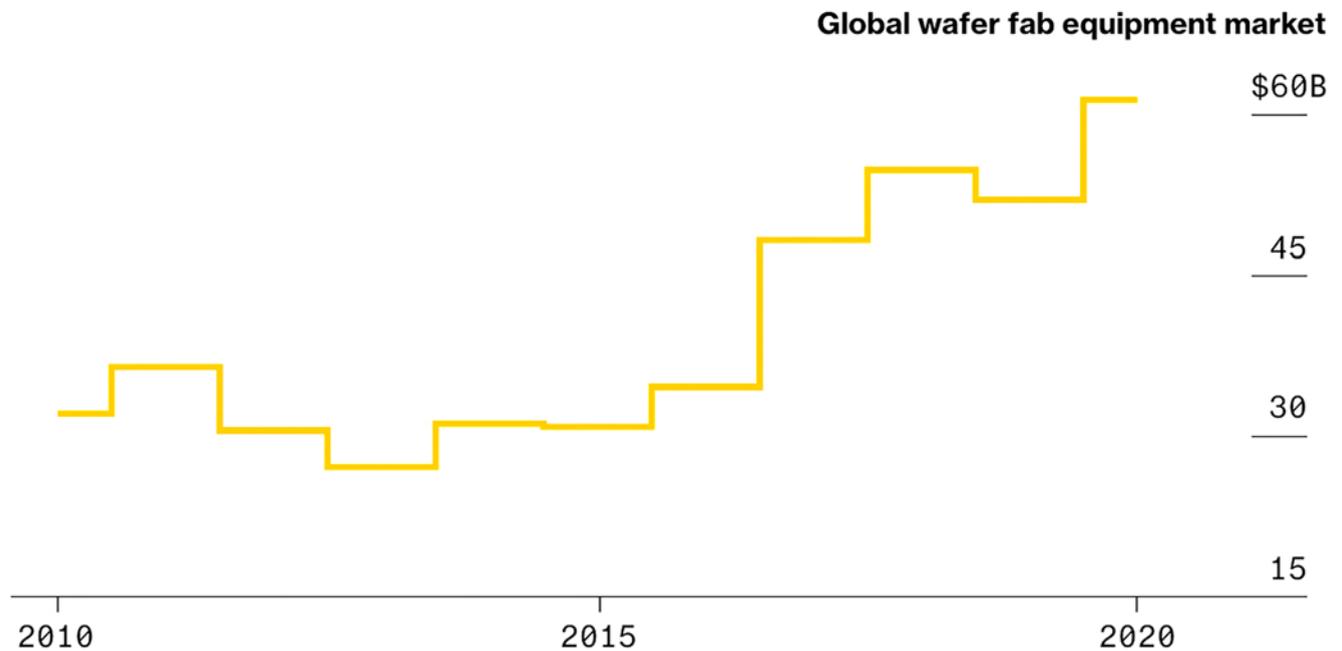
- It should be noted that there is significant advanced packaging development at the foundries
- Fabless model growth and success (Qualcomm, Broadcom, NVIDIA, MediaTek, AMD, Apple)

Migration to Chiplets

Chiplets will be a key enabler for next 10-20 years. With the high cost of monolithic integration, it is no longer possible to achieve the same economic advantages as was once observed. Rising manufacturing costs include up front expenses such as mask sets and cost per chip, increased complexity of design rules in leading-edge nodes, and the architectural challenges of meeting the relentless demand for more and more computation power. In response, there is a trend toward disintegration of system on chips (SoCs) into multiple smaller chiplets (Figures 3–5).

Heavy Duty

Sales of equipment used in chip manufacturing have doubled since 2015

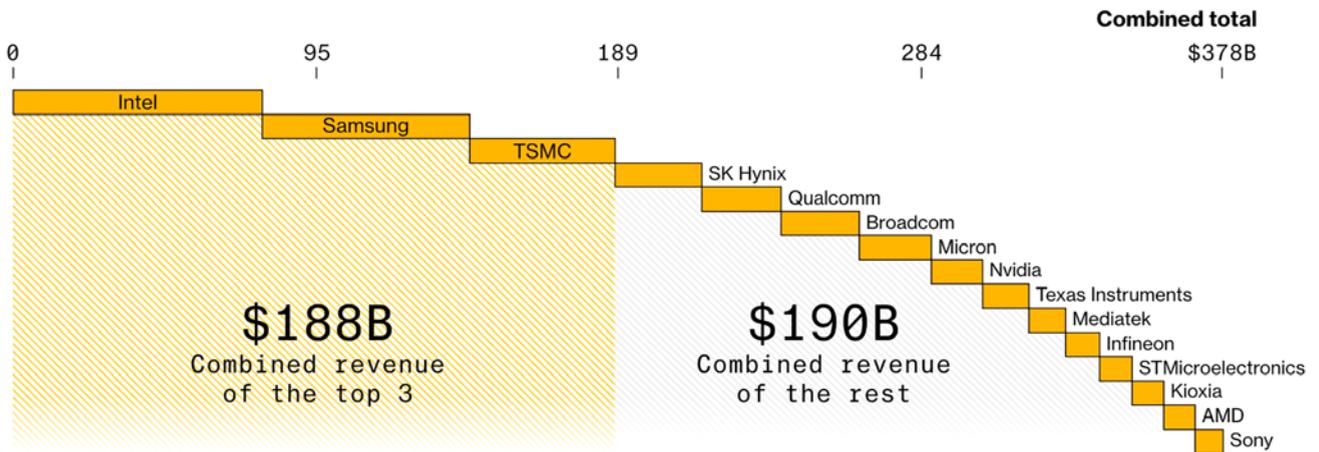


Source: SEMI

Figure 1.

Big-Fish Industry

Intel, Samsung and TSMC generated almost as much revenue in 2020 as the next 12 largest chipmakers combined



Note: Figures for Samsung and Sony include their chipmaking businesses only.
Sources: Company data compiled by Bloomberg; IDC

Figure 2.

Semiconductor Nodes

The 7 nm node is in mass production and 5 nm nodes have been introduced for some of the latest processors. The industry is on the way to introducing 3nm nodes. Samsung has provided some details of its 3 nm development plans. TSMC is in production with 5 nm

semiconductor technology, shipping application processors for Apple’s iPhones. TSMC is working on 3 nm and 2 nm nodes. IBM has announced the development of a 2 nm chip, based on gate-all-around FET. Intel indicates it is working on advanced processes and has announced plans for Intel 7 in 2021, Intel 4 for

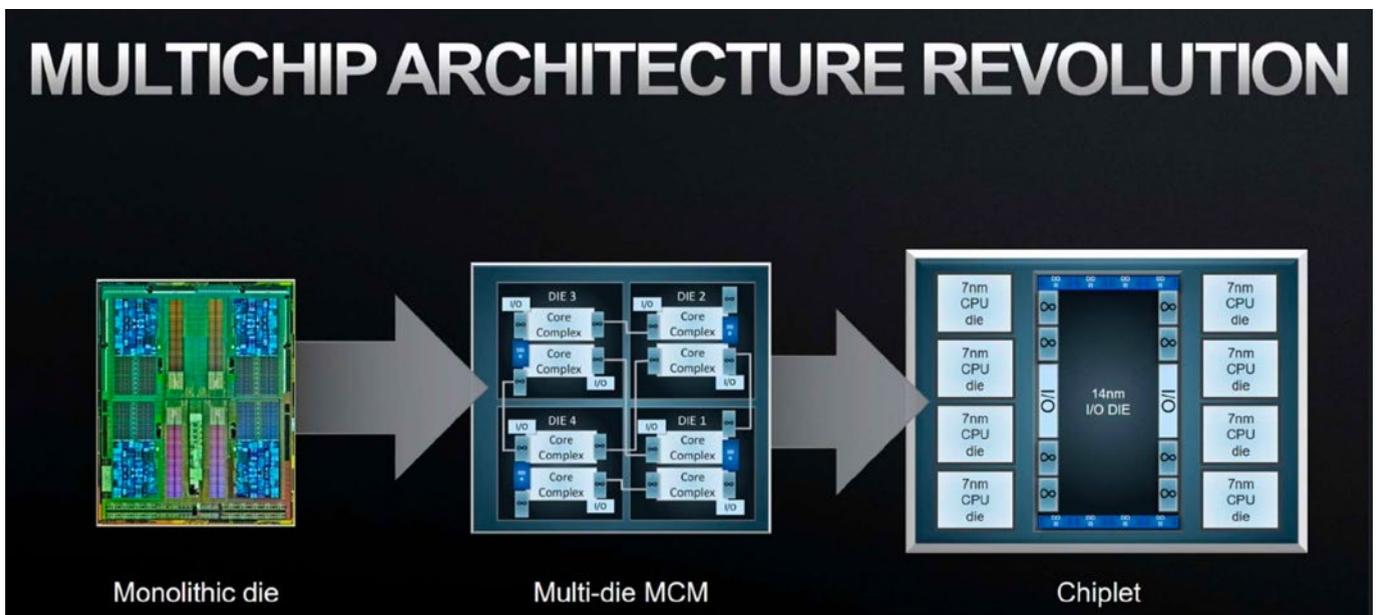


Figure 3: Migration towards chiplet architecture.

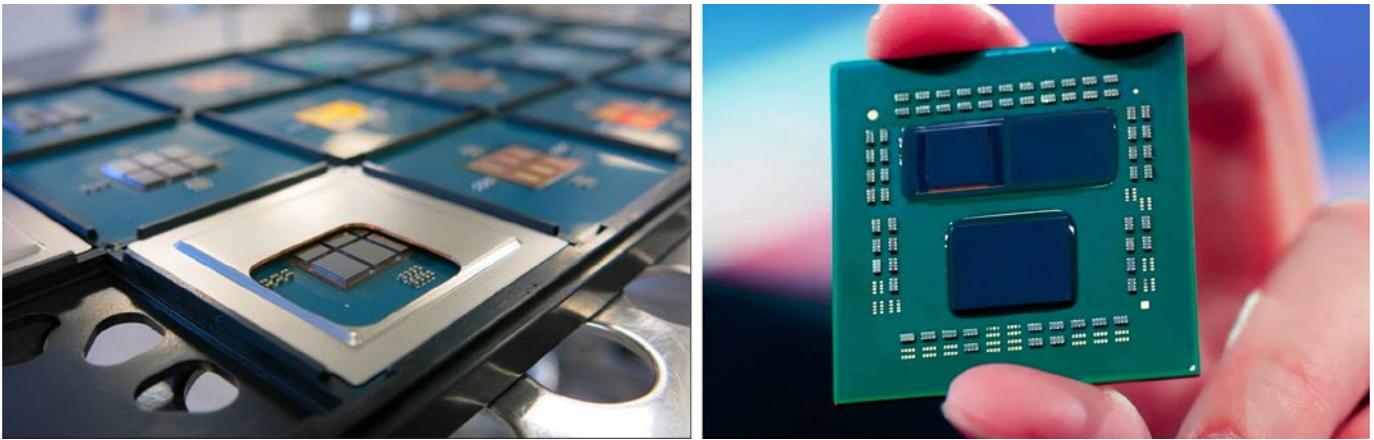


Figure 4: Chiplet layout under heatsink metal lid. (Source: Sources: IEEE, left, and AMD, right)

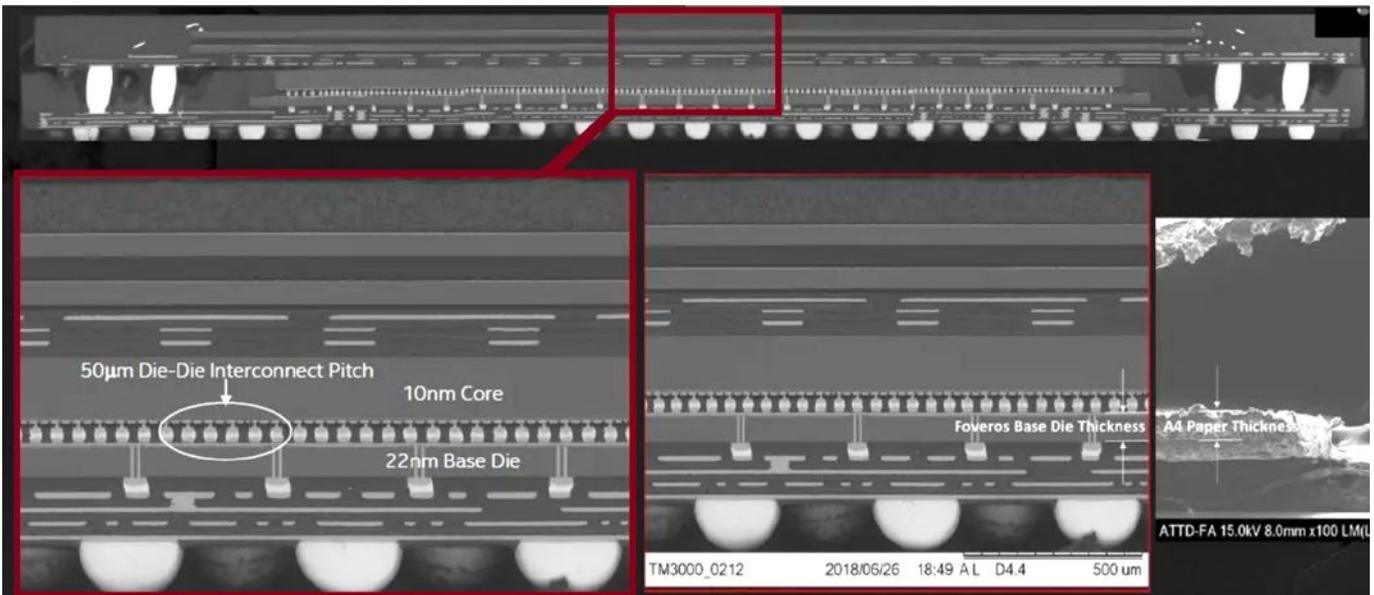


Figure 5: Intel Foveros 3D stacked die cross-section: complexity, features, structures, materials. (Source: Intel)

the second half of 2022, and Intel 3 for the second half of 2023. Intel is developing Intel 20A using a gate-all-around transistor in 2024, followed by Intel 18A. The 3 nm semiconductor node production is expected to begin in mid-2022 and 2 nm is anticipated in 2023–24. Only a few companies will be able to afford these advanced nodes and even fewer companies will be able to make them. Tables 1 and 2 show major fabs and foundries and the technology nodes offered.

Semiconductor Shortages

Semiconductor shortages are impacting shipments of automobiles, appliances, per-

sonal computers, smartphones, and servers. COVID-19 restrictions caused supply chain disruptions that led to chip manufacturing plant closures or production slowdowns yet demand for electronics products continues to rise. IDC reports that traditional PC shipments, including desktops, notebooks, and workstations reached 83.6 million units in Q2, an increase of 13.2% from the second quarter a year ago. Laptop demand for gaming remains strong.

IDC reports that worldwide server shipments increased 8.3% year-over-year to almost 2.8 million units in Q1 2021. Servers remain in high demand, but component and CPU short-

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ages could hamper shipments. TrendForce expects global server shipments to increase in the second half of the year.

Analysts expect the most problematic semiconductor shortages will end in 2022, although UMC and Intel do not see an end until 2023. Semiconductors used for the automotive industry are competing with analog ICs, power management ICs, microcontrollers, and sensors used by consumer and industrial products¹. Many of these devices are fabricated on 200 mm wafers where a shortage of capacity remains. SEMI reports that 200 mm fabs will increase from 197 in 2019 to 215 in 2022.

Analysts expect the most problematic semiconductor shortages will end in 2022, although UMC and Intel do not see an end until 2023.

The number of 300 mm fabs will increase from 121 to 151 over the same period². Ten of the new 300 mm fabs will begin operating in 2021, with 14 more in 2022. Industry experts generally agree that while double booking is causing some of the shortage, trade friction is also a stronger contributor. Over the last two quarters, major fabless companies have moved their traditional designs out of fabs located in China.

- Companies continue to order in excess, for example, Apple, Tesla—next gen 4/5 nm nodes
- The ongoing semiconductor shortage, driven by a confluence of factors, including inadequate capacity and stronger-than-expected demand, has highlighted supply chain vulnerability
- Some chip customers are making upfront payments to secure supply
- The electrification of automobiles (EV) has contributed to the chip shortage³

Silicon Wafer Shortages

Wafer supply constraints are an increasing concern. TECHCET reports that 300 mm prime wafer demand will be at >99% utilization through 2022. Epitaxial capacity is also in the 99% range. Global 300 mm wafer production capacity will need to be expanded by 6% or more over the next two years to avoid a shortage in meeting the current 300 mm wafer shipment forecast. Several companies have announced investment plans. MEMC Electronic Materials, a subsidiary of Taiwanese company GlobalWafers, will invest \$210 million for 300 mm wafer production in its Missouri facility. SK Siltron is expected to expand wafer production as early as this year. The expansion will be the first in four years since SK Group acquired LG Siltron and expanded its Gumi plant in 2017. Shinetsu and Sumco, the world's number one and number two players have announced plans to expand their facilities.

Continued Taiwan Semiconductor Technology Dominance

- TSMC fabs are the most advanced on the planet. Intel uses TSMC for advanced nodes
- TSMC continues to invest heavily (\$100 billion) over the next few years to grow capacity
- Taiwan maintains edge as largest base for IC wafer capacity
- TSMC supplies 50 to 55% of global semiconductor output offering leading edge nodes which enable everything from the latest smartphone models to graphics processing units used in data centers and AI applications

Advanced Nodes Coming from Asia; NA Suppliers Playing Catch-up

- NA nodes lagging 28 nm, 10 nm, and 7 nm
- NA headquartered fabs are lagging in state-of-the-art nodes

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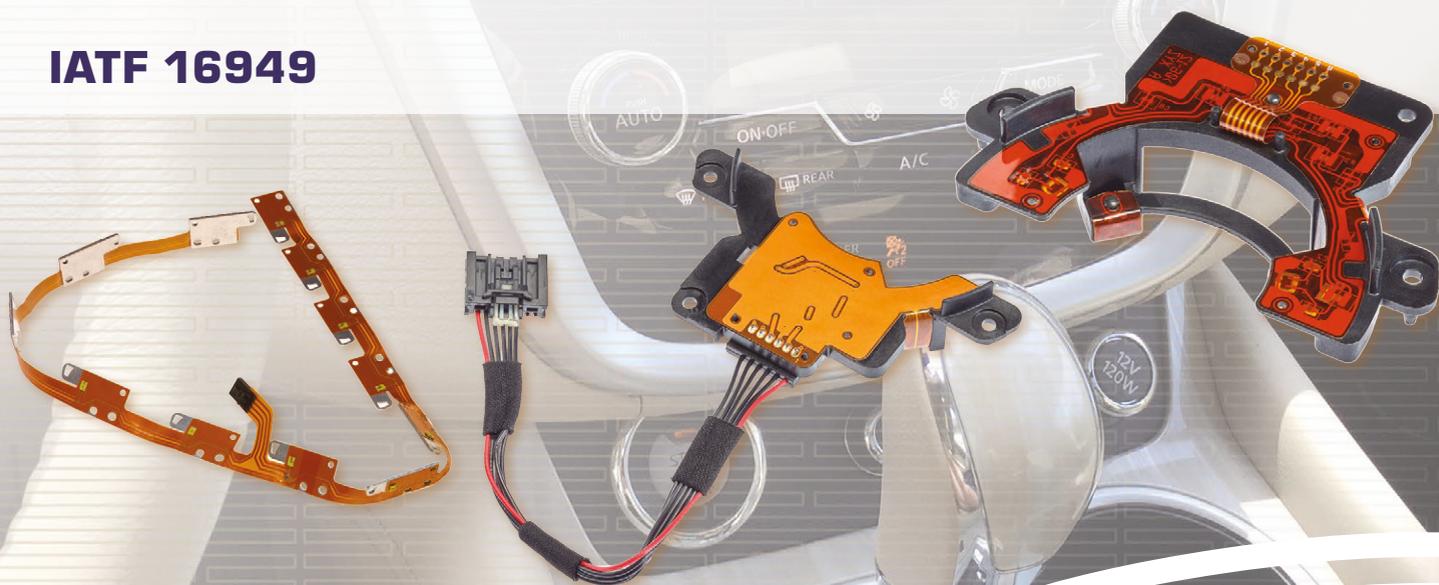
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- NA range: 10–28 nm, leading 5–7 nm, state of art 2–3 nm
- Most advanced nodes in production are used by TSMC and Samsung ranging from 7 nm, down to 5 nm and 3 nm planned for 2022. Global foundries using 28 nm, and Intel at 10 nm, 7 nm planned. Smallest 2 nm node by IBM now in development/ scale-up⁴

- Highest growth rates were from fabless suppliers (AMD, MediaTek, Qualcomm, NVIDIA)

North American Strength is in Silicon and Systems Design

Many of the top semiconductor revenue generators in the semiconductor industry are fabless. These companies have expertise in design and use a foundry to fabricate their chips. With this model they are able to maintain high gross margins

North American Semiconductor Fabs/ Foundries Current Situation

- U.S. policymakers view the semiconductor industry as strategically important because it supplies the fundamental enabling technologies for advanced defense, communications, big data and artificial intelligence among other industries
- Already have strong semiconductor capability/capacity in NA
- Fabless Model: 6/16 (40%) fabless using foundries latest investments being made in Arizona by Intel, TSMC, and Samsung are all foundries, enabling fabless support in NA
- Intel has existing fabs, but also expanding to foundry in 2024
- Global Foundries (GF) already has plant, but not leading-edge node (28 nm)
- TSMC and Samsung planning 5 nm and 3 nm foundries in 2024 in United States
- Over 50% of top-15 semiconductor revenues already coming from NA HQ companies \$5181 Q21

U.S. West Coast Fabless Model Ecosystem

New foundries planned for 2024 by TSMC, Samsung, and Intel service top performing fabless companies: Apple, NVIDIA, and Broadcom in Silicon Valley, and Qualcomm in San Diego. Location selection for these foundries

Top-15 Semiconductor Global Company Highlights

- Significant plays continue within silicon fabs and company landscape
- Example: “In his March 23 message, Intel CEO Pat Gelsinger stated that Intel would dedicate \$20 billion to two new chip foundries in Arizona, the first components of an independent division called Intel Foundry Services. The IFS foundries can now fabricate chips for any architecture and company”⁵⁻⁶.
- It took almost \$2.6 billion in quarterly sales to make it into the 1Q21 top-15 semiconductor supplier list
- Of top 15, eight headquartered in the U.S.; two each in Taiwan, S.Korea and Europe; one in Japan
- Intel and Samsung have many more fabs used for internal designs and systems, beyond the foundries listed in this report
- Top-15 revenue surged by 21% in 1Q21
- 14 of 15 of companies had revenues > \$3B in single quarter
- Two new entrants in top-15 list: MediaTek (replacing HiSilicon) and AMD (replacing Sony)
- HiSilicon is the semiconductor design division of Huawei (impacted by tariffs, sanctions)
- AMD revenue surged 93%, highest growth rate of any top-15. Expecting 2021 revenue +50% overall
- MediaTek posted 90% increase 1Q21-1Q20

Table 1: Logistics Transit Times to Support Demand and Production

Fabless Company Location	2024 Foundry Location	Travel Times
San Francisco	Phoenix	1hr 50min flight / 12hrs truck delivery
San Diego	Phoenix	1hr 5min flight / 6hrs truck delivery

can service Silicon Valley and Southern California fabless chip makers.

Significant investment already being made by US Government to increase domestic capability:

- Intel, TSMC, and Samsung (top three) all working on 2024 foundries to service fabless demand
- TSMC: 5 nm node, Arizona plus potential 5 more in US. Announced \$12B investment
- Intel: \$20B in 2 new plants, Arizona
- Samsung: \$17B 5 nm node, Austin, Texas
- Note: There are concerns by TSMC with domestic NA capability/capacity, as this is likely to slow progress and increase prices⁷ **SMT007**

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Shrinking Qubits for Quantum Computing With Atom-thin Materials

For quantum computers to surpass their classical counterparts in speed and capacity, their qubits—superconducting circuits that can exist in an infinite combination of binary states—need to be on the same wavelength. Combine qubits together into larger circuit chips, and you end up with a big physical footprint, which means quantum computers take up a lot of physical space.

In collaboration with Raytheon BBN Technologies, Wang Fong-Jen Professor James Hone’s lab at Columbia Engineering recently demonstrated a superconducting qubit capacitor built with 2D materials, rendering it a fraction of the size of previous capacitors.

In the current work, published on November 18 in NanoLetters, Hone’s

PhD students Abhinandan Antony and Anjaly Rajendra sandwiched an insulating layer of boron nitride between two charged plates of superconducting niobium diselenide. The team then combined their capacitors with aluminum circuits to create a chip containing two qubits with an area of 109 square micrometers and just 35 nanometers thick—that’s 1,000 times smaller than chips produced under conventional approaches.



New device designs should be able to shrink things down even further, said Hone, by combining the elements into a single van der Waals stack or by deploying 2D materials for other parts of the circuit.

(Source: Columbia University)



MilAero007 Highlights



One World, One Industry: Rallying Around a Robust Ecosystem ▶

The U.S. CHIPS and Science Act has been enacted and funding is now in place for its implementation. Governments globally are marshaling resources and policy mechanisms to make their own semiconductor industries more competitive in the global marketplace.

Digital Transformation: Leveraging Digital Automation to Accelerate PCB Design ▶

I see digital automation as the simplification of manual tasks that have been optimized in the digital world to a point where they require the least amount of effort to successfully do what they are required to do in the real world.

The Pulse: Fitting Physics to Fact ▶

The realities of engineering mean that compromise is always needed—and so the desire of the purist for “absolute perfection” has to be balanced with the skill of the engineer in designing product to be “good enough” for the specific application.

Pulsar Circuits Technology to Expand Operations in 2023 ▶

Pulsar Circuits Technology, a leading provider of printed circuit boards for the electronics and semiconductor industries, has just announced its expansion in the fall of 2023.

Defense Speak Interpreted: SWaPing Nanosatellites for Defense Systems ▶

When I say “SWaP,” you might be thinking: A swap for what? SWaP is a common term in the

defense community; it stands for size, weight, and power—the holy grail of technical performance for defense systems.

Northrop Grumman to Enhance UH-60V Aircraft Capabilities ▶

Northrop Grumman Corporation has been selected to provide engineering services for the KBR-led \$156.7 million, five-year Department of Defense Information Analysis Center’s multiple-award contract vehicle.

Report: Rising Use of PCBs in Aerospace, Aviation Sector Boosts Growth ▶

According to a global report by Research and Markets, a surge is expected in the coming years due to the rising use of flexible PCBs in satellites. Increasing aircraft traffic is expected to play a significant role in the rise in the demand for aircraft, worldwide.

Raytheon Missiles & Defense, TTM Technologies Reach Agreement ▶

TTM Technologies, Inc. and Raytheon Missiles & Defense, a Raytheon Technologies business, have reached a multi-year agreement to provide radio frequency assemblies, electronic hardware, and printed circuit boards for the SPY-6 family of radars. The agreement has the potential to reach \$500 million over five years.

Collins Selected to Participate in Multiple EU Clean Aviation Projects ▶

Collins Aerospace has been selected to participate in seven projects under the European Union’s Clean Aviation Joint Undertaking.

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A CMMC ‘Plan B’

Article by Divyash Patel

MX2 TECHNOLOGY

As I attend industry events and connect with the leaders of manufacturing companies in the Defense Industrial Base (DIB)—everyone seems aware that CMMC 2.0 rules are coming soon. I see a bit more activity and I’m fielding more questions. Some DIB contractors are getting it, and that’s good news. But there’s also bad news: Too many still bet they can win a high-stakes game of “chicken” with the DoD.

Running a business means balancing risk tolerance and aversion. Many of us will take risks to grow revenues or achieve strategic goals; just as many of us want to avoid risk (especially in terms of expense) if the status quo is running well. That’s a fancy way to say, “If it ain’t broke, why fix it?” Normally, that’s a legitimate question, but asking it requires you to know what “broke” looks like. When a piece of production equipment breaks, it’s obvious. When it comes to your IT network, “broke” is anything

but obvious. Your operations could be running along fine yet you have cybersecurity holes big enough to drive a truck through. That’s just what the DoD wants to avoid.

Will the Government Blink?

When business leaders act as if they don’t feel any particular urgency to hit the compliance deadline, I often hear, “If enough of us don’t comply, the government will blink. It will have no choice but to either kick the compliance deadline back again (it worked once, after all) or maybe even exempt us small operators. The DoD is going to swerve first.” That sounds like wishful thinking to me, and in the words of Vince Lombardi, “Hope is not a strategy.”

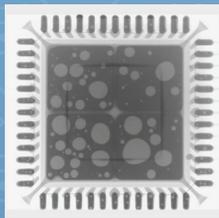
The DoD will not budge this time. Not for Levels One and Two—and those will cover the vast majority of small- and mid-sized contractors. If for no other reason than credibility, the

Pyramax Technology to Eliminate Solder Voids

Pyramax Vacuum

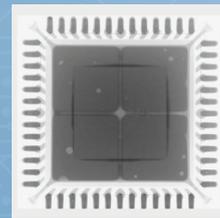


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Traditional Reflow

Voiding occurs when flux or solder paste oxidation is entrapped in the solder joint. Shown here is an MFL processed with and without vacuum reflow. BTU's vacuum reflow solution is designed to reduce voiding to <5% (process dependent).



Vacuum Reflow

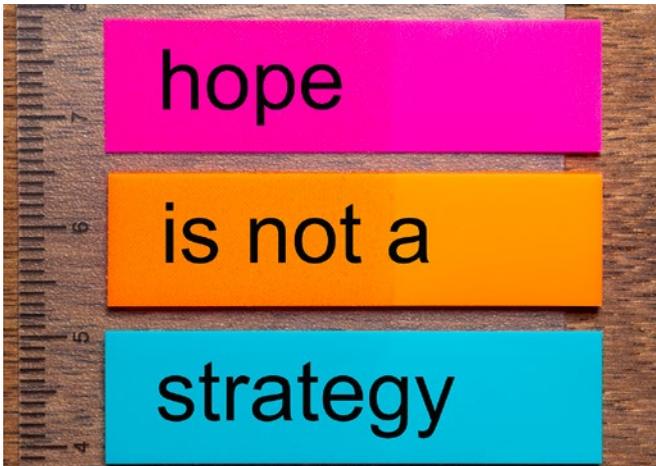
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government has to put a stake in the ground. To be honest, that stake isn't an unreasonable one. The first level of CMMC compliance amounts to little more than straightforward cyber-hygiene and a system security plan—the things that any manufacturer should be doing to protect itself, its employees, and customers from cyber-threats, be they phishing scams, ransomware, or targeted hacking.

CMMC 2.0's interim rule is scheduled to be released in March 2023, and let's say it's the very last day—Friday, March 31, 2023. What happens next? Sixty days later—call it May 31—to bid or to be included in a bid package, contractors must be able to demonstrate their compliance if asked.

Remember that Level One compliance only requires self-attestation—and while that's an improvement in terms of cost and complexity from requiring third-party assessment, it creates another potential can of worms. Come the spring of 2023, I can imagine the temptation to self-attest and then get compliant as fast as possible will be great but talk about a gamble. It's one thing to miss out on an opportunity while you become compliant. It's another thing entirely to commit fraud. But I can almost guarantee that it will happen. I certainly hope it won't happen in your case.

You Need an Individualized Plan

Maybe the contractors that are waiting think that compliance will be quick—just a nip here

and a tuck there. Or maybe there's an off-the-shelf, cookie-cutter solution they can buy online and give to their IT guy to apply. I can see why they might think that. Blog after blog, website after website, and article after article mention checklists to ensure you meet all 17 of the Level One controls. My own company publishes one. The thing is, while the 17 controls apply to everyone, each company will have to take its own path to meet them. Take, for example, access control (and I'm not even getting into physical access—meaning if your servers are kept under lock and key in a properly protected area). Some companies (many I've worked with personally) have an open-access policy. Just about anyone can access just about anything on the network. While this has advantages from a convenience standpoint, it's a nightmare from a compliance standpoint. I've had to help several clients map their business processes to actually understand who needs access to what. If these processes haven't been mapped before, this alone can be a very time-consuming activity.

Speaking of time, let's look at how long it might take to get compliant. I'm assuming there will be contractors who start in the new year, and those who will wait until March 31 (or whatever the actual date proves to be).

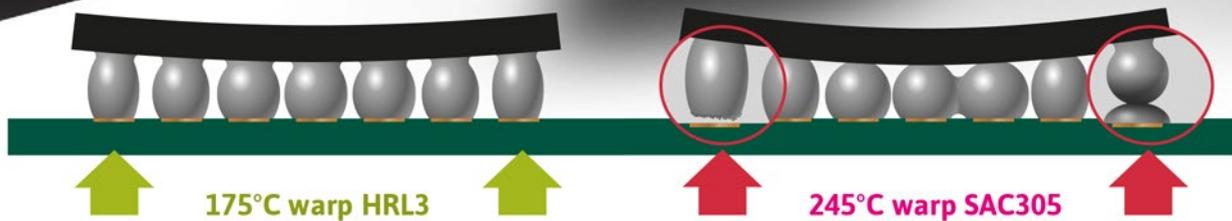
Act Now and Fast

If you've read this far, I assume you haven't started yet, so I'll make it personal. If you hit the ground running on Jan. 3, you might very well get to a level of confident self-attestation by the end of May—and maybe sooner—depending on the size, complexity, and degree of readiness of your technology environment. It will help if you are already compliant with other standards, say ISO 9001. Because you've already gone through a compliance process, you know how to meet a standard. You likely have document controls in place, you understand the versioning process and the training process. You might even have solid IT policies in place, so there would likely be some overlap between what you are already doing and where

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you need to go, but the first step is a gap analysis. To do this, you will need help, and there are a growing number of folks specializing in CMMC compliance consulting. They aren't cheap in isolation but compared to losing out on serving the DoD they are very cheap. You want to do this fast.

Whatever you do, do not rely on your in-house IT folks' assessment of your state of compliance. You will be the one signing the self-attestation, not them. This is not a knock on your IT folks. Even the best of us miss things—especially in networks we think we know like the back of our hand. That degree of familiarity creates blind spots. I have been overconfident in my knowledge of a network at times, only to find a fresh set of eyes found things I'd missed. At the least, have a competent consultant do a review after your IT folks tell you you're good.

I have been overconfident in my knowledge of a network at times, only to find a fresh set of eyes found things I'd missed.

Now, for the other group—the ones who wait until March to get started. I'm frankly worried about them. If they rely on DoD contracts for any significant part of their revenue, they might be in big trouble. If they start compliance from a greenfield state, it's a six-to-eight-month process at best, and likely longer. That is with a significant bit of outside help—which brings up another problem. As more companies demand their services, it will be harder and pricier to find competent consultants. These contractors will be guaranteed to miss out on opportunities that in prior years would have been a lock. Then, after their long-term partner organizations have been forced to

find new suppliers to fill the gap they left, those prime contractors might end up with the new supplier long term.

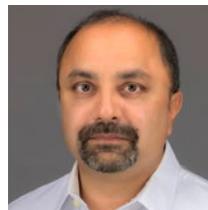
I know a few business owners who are working on satisfying Level One requirements just to get by. This is even though their standard projects would require Level Two compliance. They are taking smaller opportunities to maintain relationships. Because here is what's going to happen: Some DIB businesses will clearly not make the deadline. I don't care how long they have worked together or how good the relationship is, the major contractors will not include them on CMMC regulated projects.

Conclusion

The big contractors are obviously going to face higher degrees of scrutiny faster than small businesses will. The primes are the ones assuring the DoD that their entire supply and value chain is compliant. The stakes are just too high. What rational company would risk hundreds of millions or even billions in future earnings on \$500,000 worth of widgets? Not one. They would likely pay twice as much for the security of knowing their business is protected.

My guess is that CMMC will result in a shake-out in the small contractor community—maybe a big one. Some will stop supporting the DoD by choice. Some will find that by the time they get compliant, they will have to fight to get their market share back. Some will run out of cash and close up shop for good. While that will be terrible for the employees and their families, it will also be an opportunity for contractors that are CMMC ready. **SMT007**

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Divyash Patel is president of MX2 Technology.

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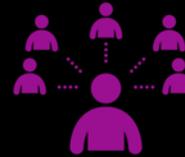
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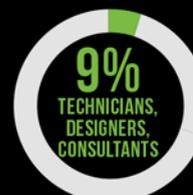
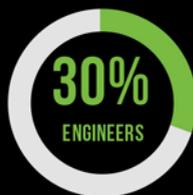




Photo credit: John Harrington

Integra: Redefining Die Prep in the U.S.

Feature Article by Matt Bergeron

INTEGRA TECHNOLOGIES, LLC

Integra is one of the largest and most experienced semiconductor die prep, assembly, test, and qualification facilities in the United States, with locations in both Wichita, Kansas, and Silicon Valley, California. At the recent IPC Advanced Packaging Symposium, Integra was invited to present information about how we meet our customers' specific needs.

For over 40 years, Integra has held its position as the largest outsourced semiconductor assembly and test (OSAT) operation in the U.S.—an accomplishment considering that most of our competition (and a few of our former owners) have given up on manufacturing in the U.S. altogether. Five years ago, customers and suppliers were saying things like, “When are you opening a facility in Asia?” and “What volume facility are you tied to?” Having a factory in the U.S. was considered laughable.

But with the arrival of COVID-19 and all its supply chain disruptions—not to mention the

current precarity of global politics—there came a realization that we are increasingly dependent on Asia for manufacturing. The CHIPS Act has generated new discussions; now we hear comments like, “We’ve said all along that we need to bring manufacturing back to the U.S.,” and “We’re building a factory here too.” People who laughed when we had a U.S. presence are now asking if we can help them get substrates sooner.

While most folks were moving out of the United States, we were looking for ways that we could make U.S. manufacturing work. We focused on two core ideas: products that are differentiated, and customers that can't or won't go to Asia.

With respect to differentiated products, we specifically targeted unique processes, such as SiPho, III-V materials, etc.; unique and unruly requirements in low-volume quantities (qualification runs, DPA, test, etc.); and volumes that Asia typically will not accept.



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Today's complex electronics include more functionality and better performance in a smaller footprint, which increases board density, reduces component size, and introduces new manufacturing techniques. These aspects challenge typical inspection techniques, especially for ultra-thin solder or mirror-finish die.

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With the Meister series, users can master critical manufacturing challenges of advanced packages.



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This last criterion also happened to fit with the space technology sector quite well.

Customers who cannot or will not use Asia for manufacturing include (but are not limited to):

- Trusted
- Military
- Medical
- R&D projects
- ITAR
- Aerospace
- Quick turn

While we continuously ran into issues with the above core ideas (like military builds in Asia), we eventually settled in with customers that wanted to make things work. Our commitment to remain flexible in how we approached pricing and customer service gave customers numerous compelling reasons to stay with Integra.

Substrates and Working With an OSAT

We currently service many customers with substrates. When building a presentation for IPC, we took a random sampling of the substrates and came up with a few key points that are distinct from the main discussion points offered by most future-looking pundits:

1. Current demand = 99% organic.
2. Lower layer counts tend to be smaller in square mm.
3. Higher layer counts tend to be SiP and larger in square mm.

Layers vs size in sq.mm

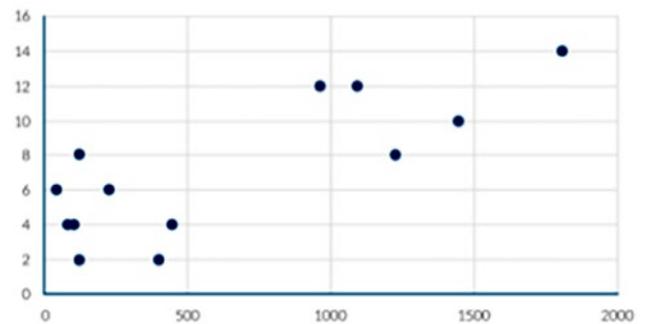


Figure 1: Substrate layer counts compared to size. (Source: Integra)

Today, our vendors tend to be mid- to low-volume; large volume vendors do not work with us.

We also looked at what we need from substrate vendors today and in the future (Figure 2). We have found that there is a distinct possibility of working with more U.S. vendors as they bring up their capabilities.

We are optimistic that as Integra evolves to become a volume player in the U.S. market, we will see U.S. substrate vendors also increase capabilities to meet the above roadmap. **SMT007**



Matt Bergeron is vice president of business development at Integra Technologies, LLC.

WHAT WE NEED FROM SUBSTRATE VENDORS

Today

- Technology**
 - 7-2-7 build-up
 - GL102 and other highspeed materials
 - 10um lines
 - 60um holes & 95um pads
 - SOP at 85um pitch for copper pillar
- Volume**
 - MOQ of a few panels (100 – 1500)
 - Volume of up to 50,000/mo
- Quality Standards**
 - AS 9100
 - ISO 13485 & other applicable
- Pricing**
 - Competitive with low volume US



In 2025

- Technology**
 - Variety of High density
 - Vast array of BU materials
 - Sum lines
 - 50um holes & 80um pads
 - Pitches <50um
- Volume**
 - MOQ of a few panels (100 – 1500)
 - Volume of up to 1 million per week
- Quality Standards**
 - AS 9100
 - ISO 13485 & other applicable
 - Automotive Standards such as IATF 16949
- Pricing**
 - Competitive with Asia



Figure 2: A visual summary of Integra’s current and prospective needs regarding substrate vendors. (Source: Integra)



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Fair and Square

Maggie Benson's Journey

by Dr. Ronald C. Lasky, INDIUM CORPORATION

Editor's note: Indium Corporation's Ron Lasky continues this series of columns about Maggie Benson, a fictional character, to demonstrate continuous improvement and education in SMT assembly.

Let's look in on Andy Connors, Sue March, and Chuck Tower at Castellanos Electronics after Maggie and John's decision to buy the company.

Maggie and John have asked Andy, Sue, and Chuck to join them in a Zoom meeting to discuss the details of their recent purchase of Castellanos Electronics. The meeting appeared to be winding down when Maggie asked Andy and Sue about their summer plans.

"It's only early June and your part-time classes at Ivy U don't start until early September, right?" Maggie asked. "Can you two stay onsite and help us with the transition?"

Andy gave Sue a questioning look. He was about to say that he and Sue needed to talk it over when Sue suddenly grabbed his hand. "We would love to," she said excitedly.

Andy and Chuck looked at each other and burst out laughing.

"What?" Sue asked, unsure why agreeing to help was so funny.

"Ah, you might have asked Andy's opinion," Chuck teased.

"Oops, sorry honey," Sue replied sheepishly.

Even though they were engaged, Andy melted every time Sue referred to him with an endearment. "It's okay," he said, "I'm just as excited as you are about staying here."

After hopping off the call, Andy, Sue, and Chuck began developing a plan. Chuck would stay a few days to perform a thorough audit of the entire operation and develop a suggested continuous improvement plan. Andy would





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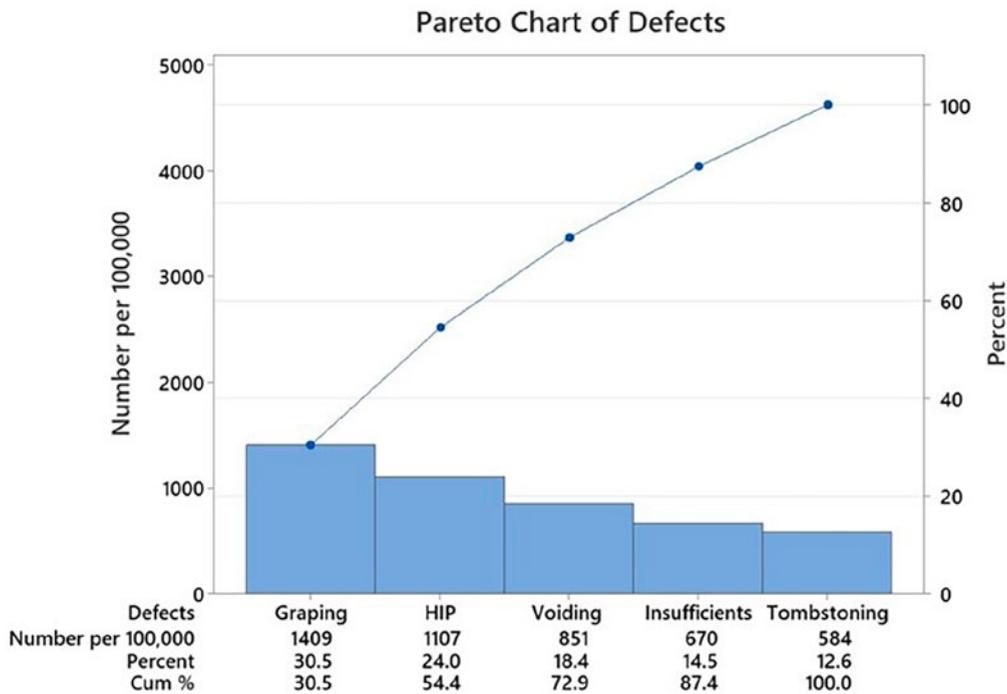


Figure 1: A Pareto Chart of the defects at Castellanos Electronics.

work with José to identify four people who, with the proper training, had the potential to become fully-fledged process engineers. Andy would oversee developing and executing that training. Eventually, these engineers would have the capability to set up lines for new jobs and, essentially, run the factory if José was not there. Sue decided that she would help Carlos develop a plan to address the defects identified in the Pareto chart the two of them had made together (Figure 1).

Once everyone was clear on their tasks, Sue met with Carlos.

“Carlos, we’ve identified graping as the most common defect,” Sue said. “Who would be the best person to discuss this with?” Carlos answered that she should meet with Miguel Santos, so together they found Miguel at his desk.

“How can I help?” Miguel asked, once everyone had introduced themselves.

Sue explained that she and Carlos had identified graping as the company’s biggest quality issue, and she wanted to discuss how to minimize it (Figure 2).

“Sue, can you explain how graping happens?” Miguel asked.

“Sure,” she said. “Graping occurs when the oxygen barrier in the solder paste is exhausted. This situation can occur for a few different reasons. The major reason for graping is that the printed solder paste deposit is too small. Because the deposit is so small, it has too much surface area-to-volume ratio, which exhausts the oxygen barrier materials in the flux—meaning they can no longer protect the solder particles from oxidation. Once solder particles oxidize, graping can occur. Graping usually occurs on solder joints that were printed

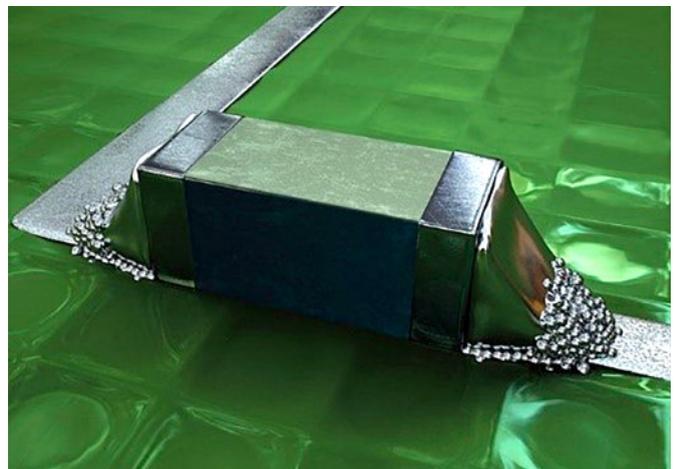
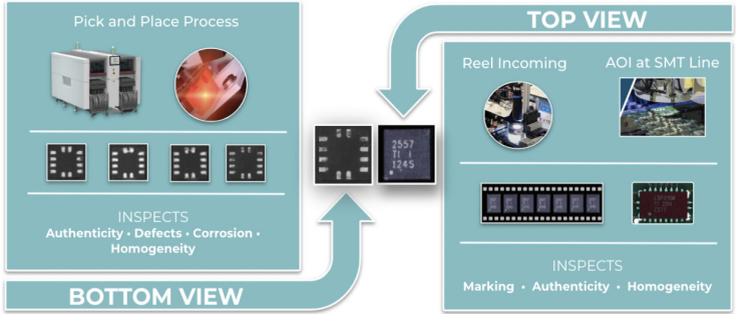
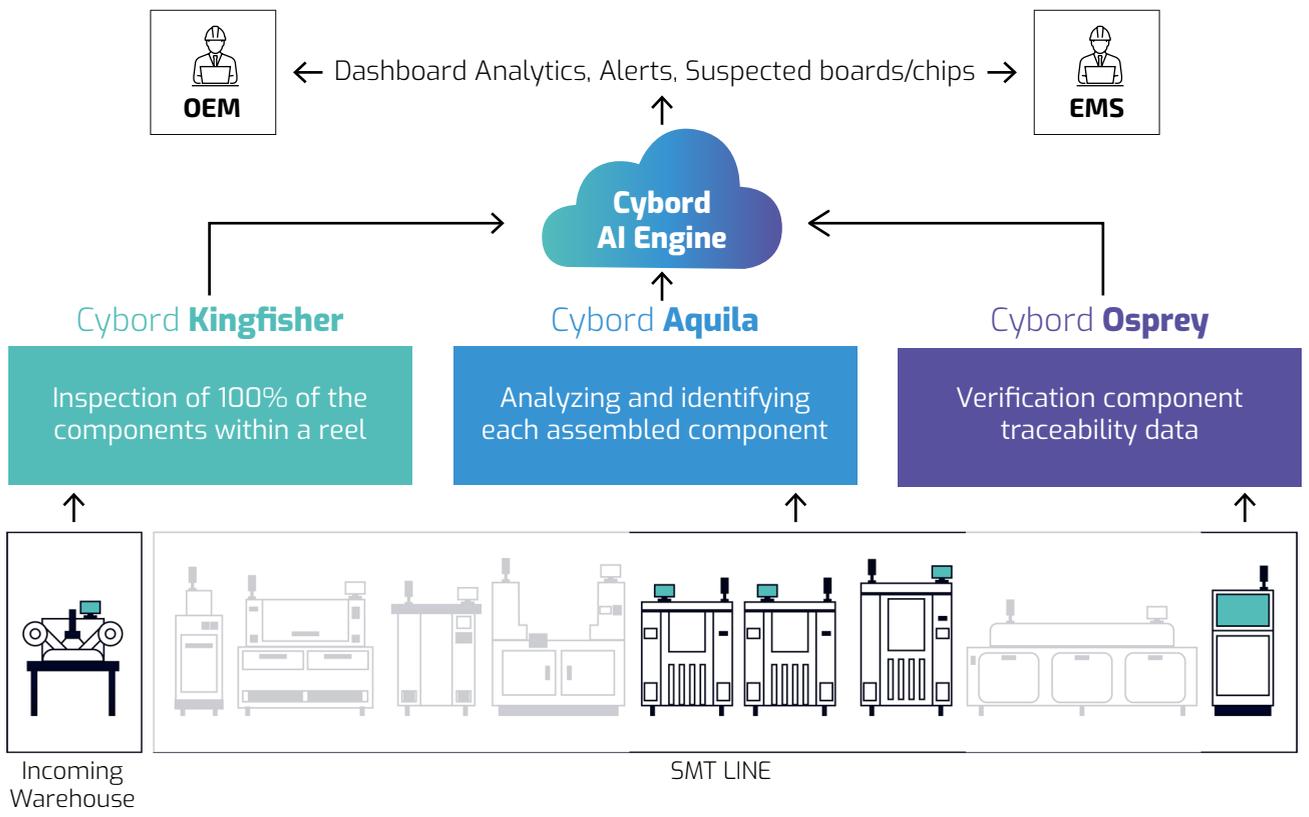


Figure 2: An artist’s conception of graping.



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with circular apertures for BGA components—is that correct, Carlos?”

“Si, señorita,” Carlos responded.

Sue continued, “Printing square apertures provides about 25% more surface area, hence 25% more paste volume. However, experiments¹ have shown that square apertures also enable improved transfer efficiency over circular apertures. It is believed that this is due to the curvature of the circular aperture, which makes the solder paste adhere more to the stencil than the pad. If we change the stencil apertures to square, the problem might go away.”

To illustrate her point, Sue pulled out a couple photos showing the differences between reflowed solder deposits from both circular and square apertures (Figure 3).

Miguel seemed impressed. “Wow, that is a dramatic difference,” he said.

“I see your PWB pads are solder mask defined, and that helps keep the solder paste flux from flowing away, which is a good thing,” Sue said. “In addition, the reflow profile is a ramp-to-peak, which also minimizes graping. So, my hope would be that changing from circular to square apertures might solve the problem¹.”

Meanwhile, Andy was meeting with José and the four process engineer candidates: Juan, Santiago, Jesús, and María. José explained to the group that Andy wanted to train the candidates to become process engineers. The training would be voluntary and would be performed on overtime, so the candidates would be adequately compensated for their time. All four looked nervous. José had selected them because they had worked at the company for more than five years, were all good employees, had good attitudes, and most importantly, were eager to learn.

“What if we’re not smart enough?” Santiago asked anxiously.

“Andy and I discussed what you would need to learn and I’m confident all of you can do it. You are all high school graduates, know how to run almost all the equipment, are good at math, and most importantly, you’re all curious

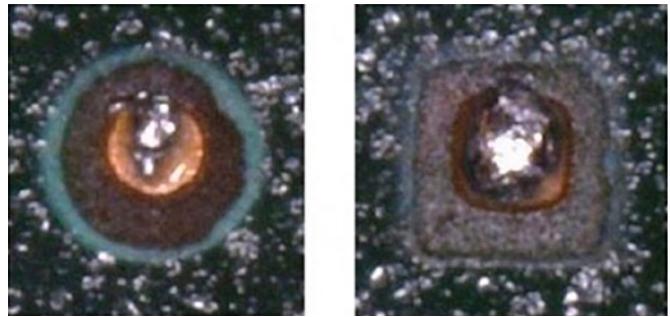


Figure 3: Solder paste reflowed after being printed from a circular aperture (left) and a square aperture (right).

and interested in learning new things,” José answered.

“How do you know we are good at math?” María asked.

“Because, at one time or another, each of you has asked me either how line balancing or reflow throughput is calculated. After showing you how to do those calculations, I’ve asked you to perform them on numerous occasions, and you’ve always gotten them right,” José responded.

Will square apertures fix the graping problem? How will Andy prepare these new process engineers for success? Stay tuned to find out. **SMT007**

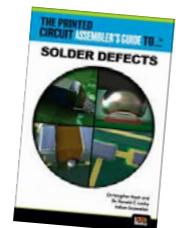
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1. “Square vs. Circular Apertures and the Five Ball Rule Revisited,” by Ron Lasky, hotwires.net.
2. For more details on minimizing graping, see *The Printed Circuits Assemblers Guide to Solder Defects*, by Christopher Nash and Dr. Ronald C. Lasky, 2021.



Ronald C. Lasky is an instructional professor of engineering for the Thayer School of Engineering at Dartmouth College, and senior technologist at Indium Corporation. To read past columns, [click here](#).

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Durability and Cost Benefits Drive Mil-Aero Demand for **OCPP**

Feature Article by Sam Sadri

QP TECHNOLOGIES

Chip packaging for military and aerospace applications must meet stringent requirements for robustness, longevity, and cost savings. Open-cavity plastic packaging has a proven history and a bright future for this market.

Ceramic packages were, for many years, the option of choice for semiconductor prototype assembly, particularly in military-aerospace applications. They can withstand high temperatures and can be hermetically sealed. However, they can be costly and, while they allow for rapid assembly of first samples, the final product is typically a plastic package, so the ceramic prototype doesn't offer an accurate representation. This need for a better, more viable alternative to ceramic was one of the catalysts that gave rise to open-cavity plastic packaging (OCPP).

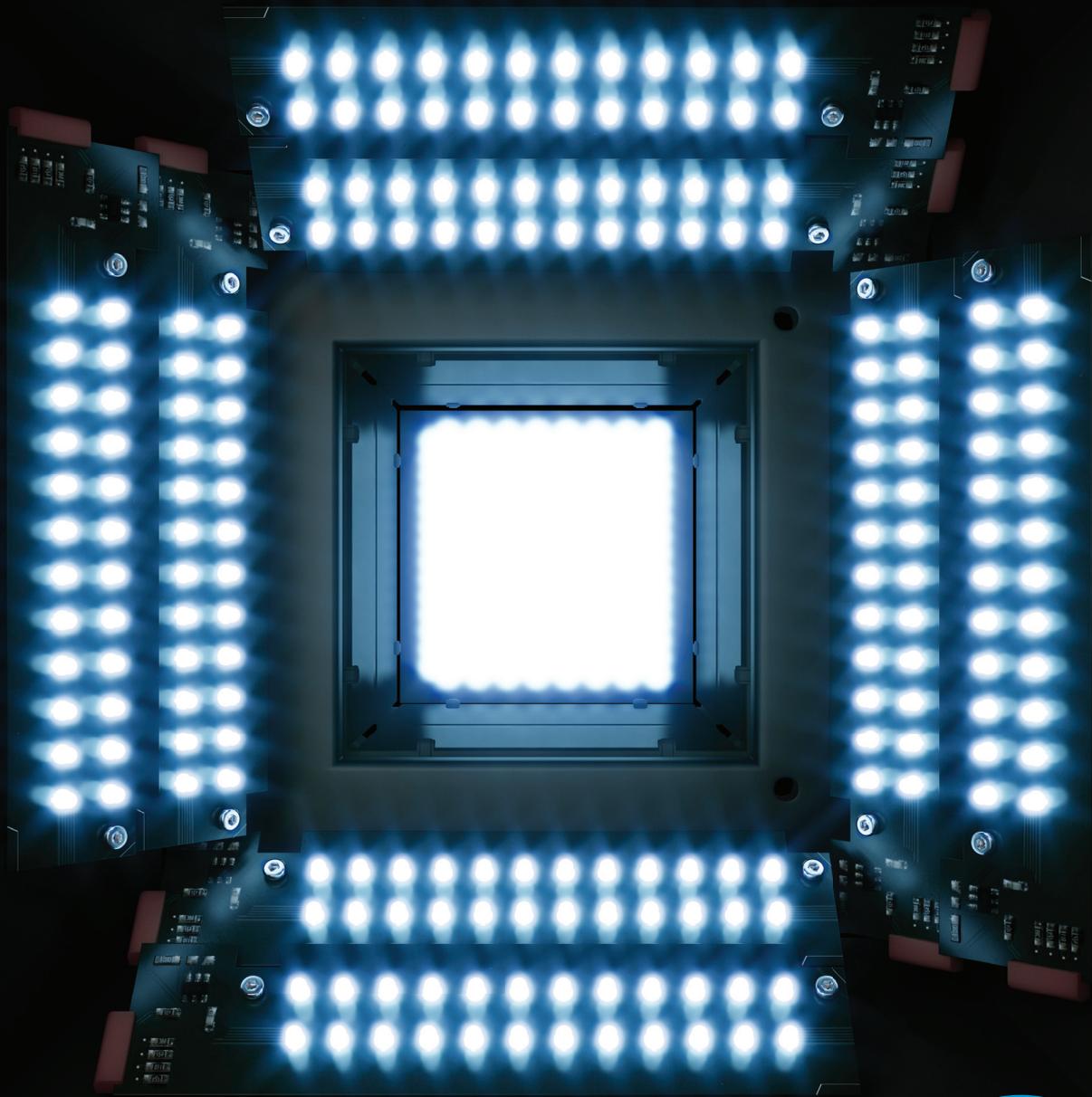
OCPP is the ideal platform for new IC prototypes because the packages are mechanically and electrically identical to a chipmak-

er's future transfer-molded production parts. They can be prepared in advance and stored for assembly as soon as the wafers and/or die are ready.

OCPP is made to withstand the test of time. This article looks at the benefits and advantages of OCPP and describes a real-world project that illustrates why utilizing OCPP for device designs offers a cost-effective solution for low- to mid-volume packaging destined for mil-aero end applications.

The Need for a Secure Supply

Semiconductor manufacturers have always striven to optimize utilization of their fab, packaging and assembly resources. The global pandemic and subsequent supply-chain issues that began in 2020 created shortages that have elevated the need to maximize these resources—and to revisit or take a new look at existing solutions with attractive time and cost benefits.



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When a project or customer deadline looms, outsourced semiconductor assembly and test (OSAT) providers may not have the resources to provide the parts needed in a timely manner. OSATs aren't structured to support product development and device verification processes. Smaller, more nimble companies can have open-cavity plastic packages readily available for quick-turn assembly of prototypes and small quantities of packaged devices.

This challenge becomes even more pronounced when the devices in question are developed for military or aerospace end products, which have stringent requirements with respect to long-term robustness and functionality. In the U.S., security restrictions also require that assembly be provided by a stateside supplier, but most OSATs are located offshore.

What Is OCPP?

Reliability data show that OCPPs have long-term value in both their ability to withstand challenging natural environments and to guard against obsolescence. When a military, avionics, or aerospace end product needs devices for which packages may no longer be available from a previous provider, redesigning is rarely an option. The manufacturer needs packages that can be quickly developed to accommodate existing functionality and fit existing package footprints.

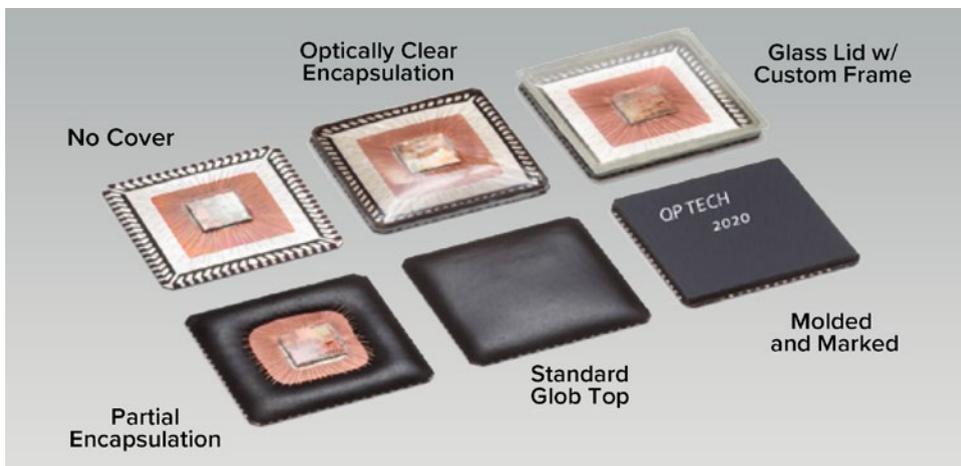


Figure 1: Encapsulation options for OCPP.

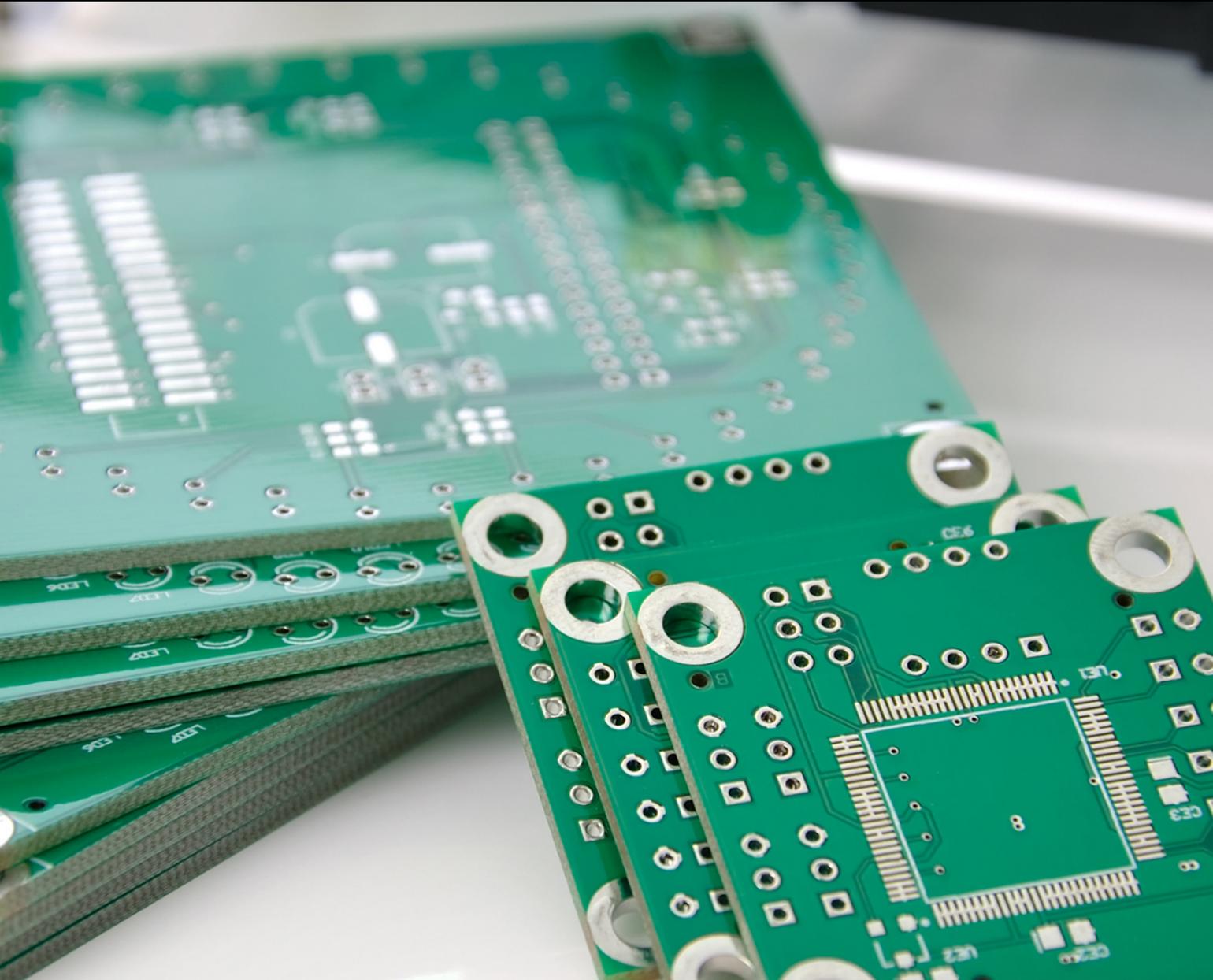
OCPPs are a type of quad flat pack (QFP) leaded package that can withstand hundreds to thousands of thermal cycles, at temperatures between -40°C and 125°C. The OCPP concept is time-tested and proven as a means of combating package obsolescence. Military vessels such as long-serving battleships, for one example, have benefited from the use of OCPP packages to preserve existing device designs and footprints, keeping the ship from having to be dry-docked.

This long-life implementation of electronic components is a well-established pattern for military and aerospace applications. In service for decades, they require devices with the quality and robustness to remain operational over the end product's lifetime. OCPP-type packages have proven their resilience for this market.

A wide variety of options can be implemented using open-cavity plastic packages. Once the molding compound is removed and the precious metal surfaces cleaned, exposing the die attach page and bond fingers, a variety of encapsulation approaches can be utilized. Figure 1 illustrates some of these options.

OCPP is analogous to a high-quality pre-owned car. Using OCPP allows reclaiming of existing "dummy" packages, e.g., electrical rejects, test packages, or excess inventory. After removing plastic and existing die down to the copper, a new package is then built within the OCPP shell. OCPP is well suited for cost-sensitive projects or those that only require small batches.

Another key application for OCPP is to employ it as an interim solution, optimizing the package and working out any kinks, before transitioning to open-molded plastic packages, which enable rapid turnarounds



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for prototype packaged devices. Die designers are often pushed to validate the performance of their new designs as quickly as possible. The time-to-market is often paramount. OSATs' infrastructure and geographical location make it challenging for them to support quick-turn prototyping for U.S.-based semiconductor design firms. With the availability of open molded plastic packages, companies with flexible assembly operations can provide the support needed.

Meeting MSL Requirements

The JEDEC moisture sensitivity level (MSL) rating is a key characteristic of plastic encapsulated micro-circuits (PEMs) that defines the storage and handling constraints during the manufacturing process for a particular PEM product. The MSL rating also determines the preconditioning stress level for the package reliability tests that are performed to qualify a PEM product for release to production.

The joint IPC/JEDEC J-STD-020E Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid-State Surface-Mount Devices standard is used to determine what classification level should be used for initial reliability qualification. Once identified, the PEMs can be properly packed, stored and handled to avoid subsequent thermal and mechanical damage during the assembly solder reflow attachment and/or repair operation.

The standard establishes the period in which a moisture-sensitive device can be exposed to ambient room temperature. MSL floor life ratings are shown in Table 1. The definition of "floor life" is the allowable time storage at $\leq 30^{\circ}\text{C}$, 60% RH before degradation occurs.

A Real-World Example

As noted earlier, OCPP is an attractive option for production when no onshore sources are available for a particular plastic package assembly, and lead time and International Traffic in Arms Regulations (ITAR) constraints prohibit offshore assembly. When avi-

Table 1: MSL definition

MSL Rating	Floor Life
1	Unlimited (30°C less than 85% RH)
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use

onics ASIC provider Device Engineering Inc. (DEI) ran into this problem, QP Technologies' OCPP approach was an effective solution for DEI's crucial production schedule, reliability requirements, and ITAR supply constraints.

DEI sought out OCPP technology as a solution for production assembly of its 64-lead thin QFP (TQFP) 10 mm x 10 mm ePad product when its prior onshore assembly provider ceased doing business, in turn, creating a challenge for DEI's customer. Once DEI was able to source a quantity of suitable dummy IC packages (containing no die) from an offshore supplier, QP Technologies converted them to OCPP, developing the assembly process and materials that achieve DEI's required package performance.

The IC was characterized for MSL, as determined by J-STD-020, and qualified via environmental stress-based accelerated reliability tests. The IC was qualified in the end product and has entered production.

To find the right process for DEI's specifications, QP Technologies experimented to evaluate various OCPP types and configurations. First, 64-lead TQFP packages were opened



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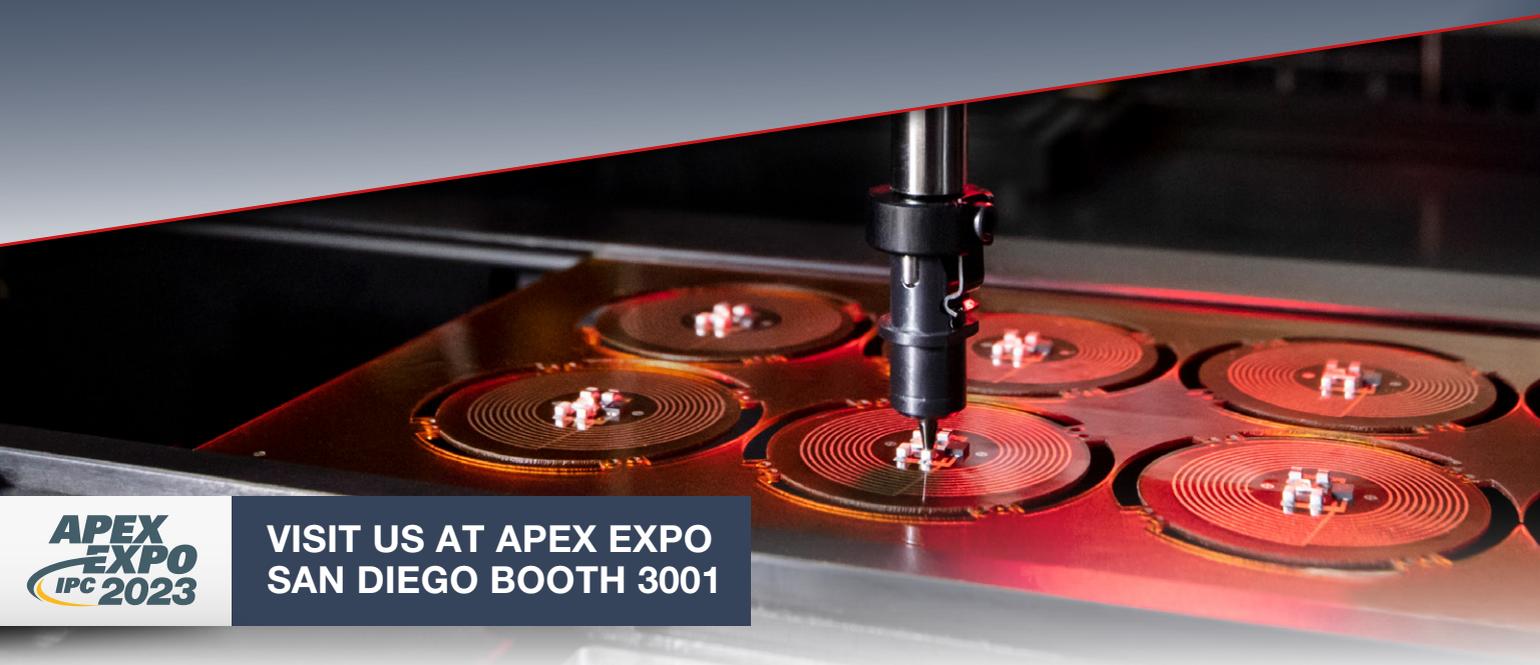
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and sent out to plating to protect the copper with a nickel-gold (Ni+Au) alloy. Nickel acts as a diffusion barrier, with gold protecting the circuit from elements.

Various die-attach epoxies were then evaluated. These included Ablebond 84-11mi and H70E, both electrically conductive epoxies with silver particles. In both cases, epoxy bleed-out later created delamination between encapsulation and surface of the package, with parts failing solder stress tests as detected by confocal scanning acoustic microscopy (CSAM) imaging.

As the design comprised multiple downbonds, it was essential that the die attach pad be free of delamination from solder stress. Experiments were performed that demonstrated that the die attach pad with its native copper and silver spot plating yielded better solder stress performance compared to those with nickel-gold plating. Thus, the extra plating step was eliminated.

Next, another design-of-experiments (DOE) set was started, working with unplated OCPP packages. Various epoxies were evaluated, and a newly formulated product, Ablebond QMI529HT, was selected. This epoxy is designed specifically for copper, features min-

imal bleed-out, and doesn't affect the adhesion of encapsulation to the copper, as CSAM indicates. The epoxy is also compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment directive (RoHS). In addition to EU RoHS guidelines, QP Tech adheres to California's own RoHS laws governing electronic devices sold in the state.

Once the optimal epoxy and OCPP type were determined, QP Technologies pursued multiple iterations to develop the ideal recipe for building packages that would pass all-important MSL testing. The packages passed MSL-3 / 235°C solder stress tests with no evidence of delamination, with results equivalent to factory-fresh parts.

To ensure repeatability of the process, a traveler was created to document the recipe, including the exact steps and order in which they must be performed—epoxy type, how the package is opened, the wire bonding process, encapsulation, material, etc.

First, a lot of 50 packages was developed, on which DEI performed pre-compliance (confidence) reliability testing. After passing this testing, several hundred packages were assembled as a qualification lot. These were produc-

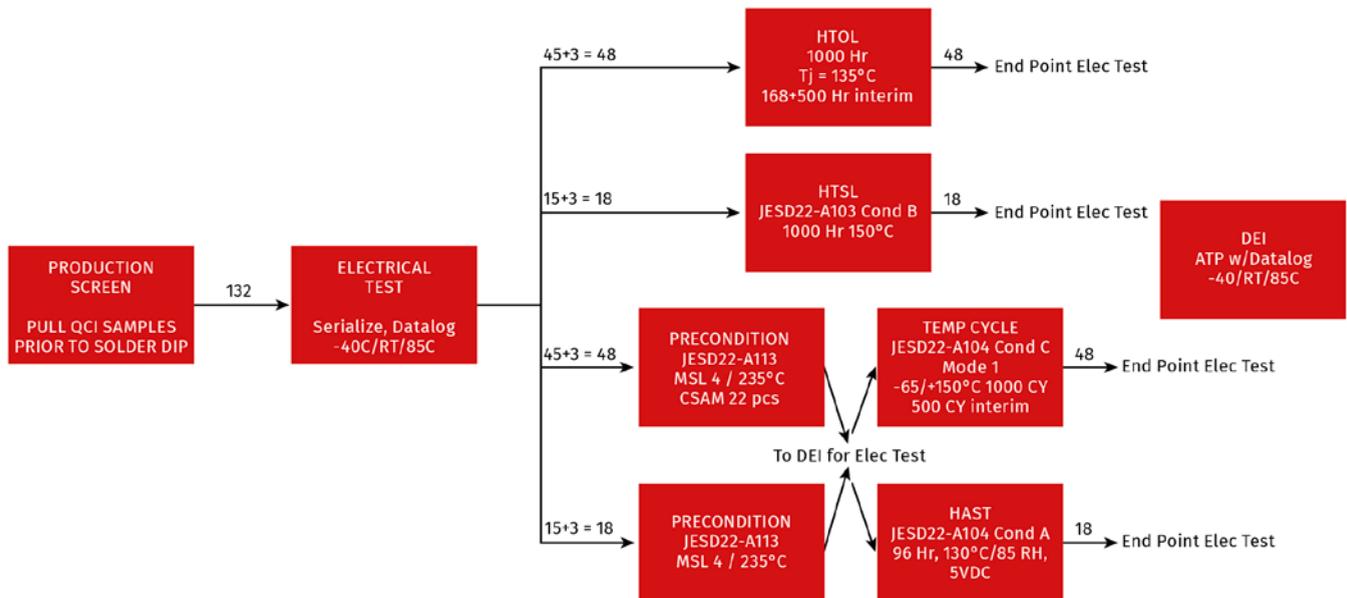


Figure 2: Qualification test plan for 64 QFP OCPP.



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Package Assembly Tests

QC Lot				
Test	Min Limit	SS	Range	Result
Die Shear	2.5 kg	6 units	12.3-27.8 kg	Pass
Destructive Wire Pull	4.0 gr	2 units 12 wires each	7.4-14.3 gr	Pass

Tin Mitigation SnPb Hot Solder Dip Tests

HSD of "Dummy Packages" no die			
Test	SS	Notes	Results
CSAM Inspection	4 units	No delamination	Pass
XRF Composition/ Thickness	3 units 4 readings each	SnPB% OK Thickness OK	Pass

QC Lot ¹						
Test	Condition	Duration	Sample Size	Reject	Date	Notes
Electrical ASL Test	DC Characteristics and Function -40°C, 25°C, +85°C	N/A	132	0	4Q20	
RF Test	RF Function -40°C, 25°C, +85°C	N/A	132	0	4Q20	
PC Precondition	JESD22-A113 MSL4 / 235°C, CSAM, qty 22	24 hours	66	0	4Q20	
PC+HAST	JESD22-A110 Cond A 130°C, 85% RH, Biased, Cycled Power	96 hours	18	0	4Q20	
HTOL	883 Grp C TM1005 Tj>125°C, Ta=90°C, 5 V Constant Bias	1000 hours	47	0	4Q20	(2)
HTSL	JESD22-A103 cond B Ta = 150°C	1000 hours	18	0	4Q20	
PC+TC	JESD22-A104 cond C Mode 1 -65°C to +150°C	1000 cycles	48	0	4Q20	

1. QCI samples are without SnPb HSD.

2. One of 48 HTOL samples was pulled at the HTOL 500 hr interim test due to a non-relevant failure. It failed electrical continuity due to lead/socket issues. The leads were cleaned with IPA/sonic and the unit then passed electrical test but was too late to return to the oven.

Figure 3: Qualification test summary for OCPP.

tion screened by DEI, including temperature cycling, burn-in and electrical tests. Finally, the leads and ePads were hot solder dipped to remove the native matte tin plating. Several of the screened parts were submitted for qualification testing. Figure 2 illustrates the qualification tests and flow. The reliability tests were performed with MSL 4 / 235 °C preconditioning per the product requirement.

DEI Project Results

The OCPP packages were tested and qualified for production with results meeting the requirements of factory-fresh parts. The tables shown in Figure 3 provide further insight into the qualification testing process, conditions, and results.

Parts were subjected to a range of component level environmental stress tests and conditions. Not only did the parts pass these tests, but also the end item equipment production and final assembly qualification tests. This case study illustrates the robustness of the OCPP solution and highlights its effectiveness in a mil-aero application. **SMT007**



Sam Sadri is a senior packaging engineer at QP Technologies.

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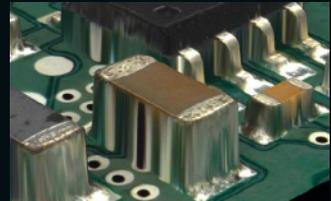
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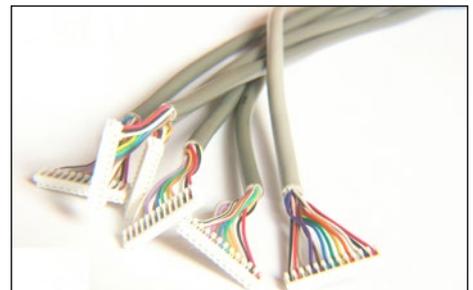
by **Blackfox Training**

Electronics manufacturing companies need skilled and certified workers to perform the intricate and important tasks required to build modern electronic equipment. Here, we explain five ways to gain these workers:

1 Train and Certify Manufacturing Employees and Support Staff to the IPC Standards

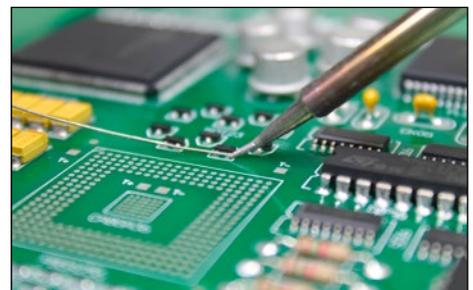


2 Fill Training Gaps with Customized Courses that Focus on Basic Knowledge and Skills



3 Access Tools and Resources to Assess Your Workforce and Maintain Skill Levels

4 Stay Up to Date with Constant Changes in the Electronics Manufacturing Industry



5 Hire U.S. Military Veterans Who Have Already Completed Immense Training

1 Train and Certify Manufacturing Employees and Support Staff to the IPC Standards

IPC certification is an internationally recognized credential that proves an employee's knowledge and skill level. IPC training and certification is industry developed and covers electronic manufacturing quality concerns, including PCB assembly and soldering, rework and repair, wire and cable harness production, and bare PCB fabrication. Having an IPC-certified workforce demonstrates an attention to detail and commitment to quality.

2 Fill Training Gaps with Customized Courses that Focus on Basic Knowledge and Skills

IPC training and other standardized courses don't cover every aspect of electronics manufacturing. Therefore, it is important to have customized courses that fill those missed gaps. Basic soldering, ESD, and electronic component identification are just a few examples of the many courses that complement IPC certification and ensure that your workforce is prepared for any challenges that may come their way.

3 Access Tools and Resources to Assess Your Workforce and Maintain Skill Levels

Assessing your workforce before and after training is an essential part of a proper man-

ufacturing training program. The effectiveness of training and the retention of knowledge gained can be gauged through assessments that are computer-based, interview-based, or audit-based. In addition to assessments, both students and trainers need to have complete access to resource documents and training materials after training has been completed.

4 Stay Up to Date with Constant Changes in the Electronics Manufacturing Industry

Technological advances and new discoveries are occurring constantly that greatly impact how we manufacture electronic products and evaluate them for quality. This makes maintaining your IPC Certifications through renewal and recertification critically important. In addition, attending industry meetings and participating in IPC committees will ensure access to the latest information.

5 Hire U.S. Military Veterans Who Have Already Completed Immense Training

Now more than ever, highly skilled and efficient employees are needed in manufacturing. The U.S. military invests an enormous amount of training in our soldiers. They are equipped with a framework of skills and attributes such as loyalty, integrity, leadership, and excellent work ethic. They know how to learn new skills quickly and adapt to changing environments, which are highly desirable qualities for manufacturing.



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2 Registration, Alignment, Accuracy

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4 Automation Possibilities

5 Features for Automation to Increase Utilization



1 Automation in PCB Production

PCB manufacturers worldwide are investing in new equipment to improve technology and production, especially in the field of automation. In Europe, the automation of drilling machines is already standard to increase productivity and achieve a higher degree of utilization. The current talent shortage in the U.S. and Canada is accelerating the demand for automation as well. Drill and rout machines with shuttle system and loaders; direct imaging machines with robot arms; and X-ray capabilities with drill and inline automation already allow the automatic loading and unloading of PCBs and ensure contact-free panel handling in the factory, which results in both labor cost savings and quality assurance in the PCB.

2 Registration, Alignment, Accuracy

Highly technologized devices such as spindles, lighting-heads, laser sources, cameras, code readers, and sensors are built-up on solid granite and then connected to the machine controller to deliver perfect results and ensure highly accurate PCB processing. For high-end panels, machines with CCD are an option, as any inaccuracies of the panel will be corrected. A two-pin system on panels is mandatory for automated drilling and a well-proven process to support the needed accuracy.

3 Maximum Productivity with the Right Application

Track and trace technology is also being adopted in the handling of PCBs. With a barcode or 2D code, panels can be uniquely identified and processed according to the specific CAD/CAM program. Integrated CCDs and scanner systems in the machines handle the reading of specific part programs.

Automated calibration procedures ensure machine accuracies at the highest level to

ensure quality of drilled, routed, and imaged products. Automated spindle maintenance reduces machine down-time and increases productivity.

4 Automation Possibilities

The engineering industry has recently advanced with Industry 4.0 and the building up of several new standards. Drill, rout, and laser machines can be equipped with a loader to feed the panels automatically—one of the new simplified solutions. X-ray and direct imaging machines can now be put into a production line with belt conveyors and run at a constant speed, resulting in increased output. Panels are then handled with robot arms. More robotics have also been introduced to the market, including automated guided vehicles, automated line systems, and shuttle systems.

5 Features for Automation to Increase Utilization

Standard SW interfaces to the MES allow bi-directional communication between machines and high-level production controls, which allows for real-time status information. An operator can have remote access to all machines from the control room, allowing them to monitor automated PCB production, run statistics, and react quickly to any error message or breakdowns.

Bürkle North America distributes and services Bürkle GmbH and Schmoll Maschinen equipment which includes IMPEX and LHMT. BNA distributes equipment lines for multilayer lamination, drilling, cutting, routing, imaging, registration, automation and measuring. Visit [Burkle North America](#) online.

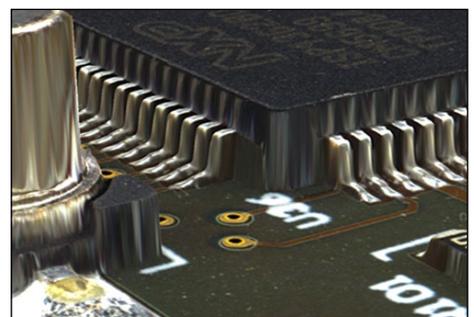
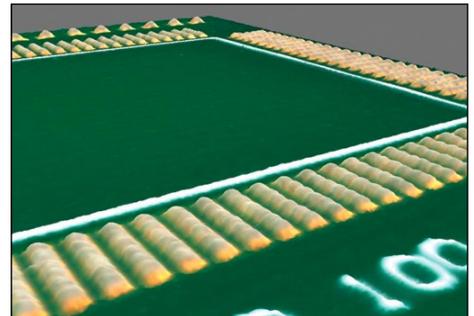


The Top Five Things You Need to Know About **INSPECTION**

by **Mycronic**

Inline 3D SPI and 3D AOI are the most cost-effective ways to control and optimize process efficiency. To get the most from your investment, here are five things to consider:

- 1 AI-assisted Software for Easier and Faster Programming**
- 2 Reliable and Approximation-free Volume Measurement of Paste Deposits for Highest SPI Efficiency**
- 3 Real-time Auto-control of 3D AOI Program Efficiency to Prevent False Calls and Escapes**
- 4 Flexible and Agile 3D AOI Technology to Ensure Consistent Performance**
- 5 Process Control Based on Inspection Data Analysis to Maintain Highest First-pass Yield**



1 AI-assisted Software for Easier and Faster Programming

Today, AI technologies make it possible to program 3D SPI and 3D AOI in record time, regardless of the operator's experience level. With MYPro Create, SPI and AOI programming is not only easier, faster, and more cost effective, but also less operator dependent. This brings inspection within the reach of low-volume/high-mix electronics manufacturers for whom speed and flexibility are prerequisites.

2 Reliable and Approximation-free Volume Measurement for Highest SPI Efficiency

Accurate Z-referencing is key to reliable inspection for increasingly miniaturized solder paste deposits. The PI series 3D SPI processes hundreds of references across its ultra-large field of view, positioning the Z-reference at the surface of each pad without applying thresholds or approximations. Regardless of board warpage, you always know the exact volume of paste deposited on even the smallest pads.

3 Real-time Auto-control of 3D AOI Program Efficiency to Prevent False Calls and Escapes

When programming your 3D AOI, how can you ensure that your last library modifica-

tions will not generate excess false defects, or worse, miss real defects? With Escape Tracker, the MYPro I series 3D AOI alerts to potential escapes and false calls generated during both programming and fine-tuning and points out the corrections necessary to avoid them.

4 Flexible and Agile 3D AOI Technology to Ensure Consistent Performance

An all-in-one 3D AOI technology needs to be extremely reliable and as flexible as possible to address changing customer requests. Mycronic's MYPro I series includes the industry's most comprehensive standard toolbox to help users manage the broadest range of applications, enabling: state-of-the-art test coverage; top and bottom THT and odd-shaped component inspection; and metrological testing, all with the same standard equipment.

5 Process Control Based on Inspection Data Analysis To Maintain Highest First-Pass Yield

Inspection equipment is the sensor of an SMT assembly line. MYPro Link, a real-time web-based interface, correlates and analyzes SPI and AOI data to transform this information into useful KPIs for monitoring production performance. Add detailed root-cause analysis from MYPro Analyze, and you can anticipate process variation and correct process drift in real-time.

MYCRONIC

Mycronic is a global high-tech company that develops, manufactures, and markets production equipment that meets the electronics industry's highest expectations for precision, flexibility, and efficiency. Visit us online at: mycronic.com.

The Top Five Things You Need to Know About

SOLDER MASKS

by Taiyo America

The main function of solder mask is to insulate and prevent the copper surface from oxidizing/corroding and prevent solder bridging. While these are the main objectives for solder mask, in the electronics industry there is a misconception that all solder masks are alike.

- 1 Selecting the Right Solder Mask**
- 2 Solder Mask Applications Evolve**
- 3 Advances in Solder Mask Imaging**
- 4 To Flex or Not to Flex**
- 5 Solder Masks Are Not Only Green**



1 Selecting the Right Solder Mask

In the world of electronics there are multiple industries each with their own requirements when it comes to solder mask. For the automotive sector, solder masks are required to withstand harsh environments. In the aerospace industry, solder masks must meet out-gassing requirements. Over the years, white solder masks have been developed that provide a high degree of reflectivity for the LED market.

2 Solder Mask Applications Evolve

Solder mask and the methods by which they were applied have evolved over the years. When non-photoimageable solder resists were introduced to the printed circuit board (PCB) industry, silk screen printing was the common method of application. As the demand for real estate on PCB designs increased, photoimageable solder masks were developed. The popularity of photoimageable solder masks introduced new application systems such as double-sided screen printing, curtain coating and spray systems. These methods of application have been around for many years and are still being used today. In the past five years, several other application processes have been reintroduced to the market including ink jet and photoimageable dry film.

3 Advances in Solder Mask Imaging

As technologies advance and offer more functions, PCBs have become more populated with the miniaturization of key components. The advancements have pushed the boundaries on image registration using conventional exposing units. Over the years, direct imaging (DI) systems were introduced to the PCB industry to help alleviate the challenge. The DI systems provide different wavelengths in comparison to conventional exposing units. Solder mask manufacturers, working side-by-side with equipment manufacturers, developed DI solder masks that are better suited for these types of imaging systems.

4 To Flex or Not to Flex

Solder masks have some degree of pliability. Thinner PCBs that are not categorized as a flex build can sometimes encounter a degree of bending due to handling or manufacturing processes. Depending on the amount the substrates are bent, they can exhibit a degree of fracturing. Fracturing of the solder mask is not the same as corner cracking caused by exposure to harsh environments. In cases such as this, PCB manufacturers and contract electronics manufacturers (CEM) should consider the use of a flexible solder mask.

5 Solder Masks Are Not Only Green

Solder masks have evolved from green to several other colors over the years. The most common colors besides green are black, blue, red, white, and yellow—all of which fall in the family of primary colors. Colors were developed and brought to market at the request of original equipment manufacturers (OEMs). Colored solder mask can be used for identifying prototypes, revision changes, manufacturing facilities, or for cosmetic reasons. Colored solder masks can also be combined in measured amounts to create a vast number of other colors such as orange, purple and brown. Solder masks can also have various surface finishes such as matte, glossy, or somewhere in between, depending on customers' requirements.



Established 30 years ago, Taiyo America Inc. is a subsidiary of Taiyo Holdings Co. Ltd., the world's leading manufacturer of specialty inks and solder masks for printed circuit boards.

Taiyo offers conductive inks for manufacturing printed electronics. Visit us online at: Taiyo-america.com.

The Top Five Things You Need to Know About **LONG-LASTING PARTNERSHIPS**

by Technica, U.S.A.

A good supply partner becomes an extension of your business. Having the right one gives you an advantage and peace of mind. Choose wisely.

- 1 Create Long and Strong Partnerships**
- 2 Low Risk of Interruption of Support**
- 3 Visibility Into Local and OEM Parts Inventory**
- 4 Constantly Advancing Quality and Technology**
- 5 Service Staff With Product, Process and Application Experience**



1 Create Long and Strong Partnerships

Partnership is a word often used in business relationships but a true partnership is built on trust and visibility. The investment of our people's time and effort has provided us with the privilege to share in true partnerships with our suppliers and customers. True partnerships withstand tough times from either side of the partnership and when the challenges arise, a True partnership comes alive.

2 Low Risk of Interruption of Support

Downtime in this environment is extremely costly and finding technical support when you need it is critical to any manufacturing business. Working with supply partners to help develop innovative programs and methods for responding to issues is important. Making sound decisions on where our supply partners are located allows us to minimize the risk of interruption caused by geopolitical concerns.

3 Visibility Into Local and OEM Parts Inventory

There is nothing more important than having 24/7 visibility to spare parts inventory. Working with a supplier that carries a large inventory of spare parts is essential in eliminating down

time. Having ongoing dialogue between all parties to match inventories of critical spare parts is important part of a partnership.

4 Constantly Advancing Quality and Technology

R&D is key to maintaining your competitive advantage. It improves your quality, capability, and market growth opportunities. Suppliers that are committed to working with us and our customers towards advancement and improvement is essential to the future of our businesses.

5 Service Staff with Product, Process and Application Experience

There is no substitute for experience when it comes to a service team. Make sure your suppliers are providing you with expert knowledge that you can trust and rely on.

About Technica

Since 1985, Technica, U.S.A. has been providing the electronics marketplace with innovative products manufactured by the world's leading suppliers that provide our customers with technological advantages for producing complex electronic products.



TECHNICA, U.S.A.

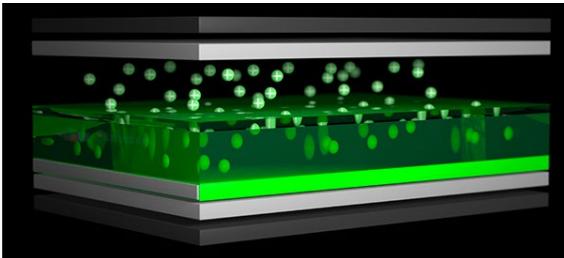
Find us online at: technica.com



SMT Perspectives and Prospects: Cybersecurity Requires an Active Approach

A cyberattack can be surreptitiously detrimental, crippling business operation, the national economy and security, or just jeopardizing an individual laptop. This pervasive and persistent security threat is one of the most formidable challenges of our times.

X-Rayted Files: Battery-Powered Advancements Keep on Ticking



Understanding that batteries will power our increasingly electrified future is an important focus for the electronics manufacturing industry, and is crucial to the success of this enterprise.

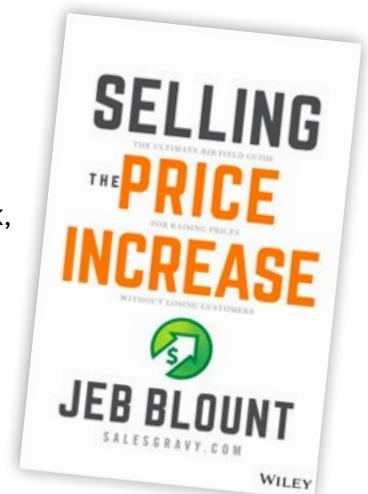
Smart Factory Insights: Clinging to Best Practices in Worst-case Scenarios

We must take a more modern approach to best practices, one that embraces the ability to change, and is flexible and adaptable to cope with the unexpected (which are actually expected) issues. Knowing how to create change-centric manufacturing best practices comes from experience.

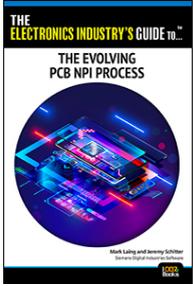


Dan's Biz Bookshelf: A Timely Book on a Timely Subject—'Selling the Price Increase'

Prices for everything are on the rise. This means many companies will be or are facing the challenging need to raise prices. It's a daunting task, especially for salespeople. This new book by Jeb Blount is a true "must have" for anyone who must face telling their customers that prices are about to rise.



Excerpt: The Evolving PCB NPI Process, Chapter 2



Managing the supply chain for electronics manufacturing has always been challenging. About 70–80% of the cost of building an electronic product is for the parts, while the remaining cost is in the process to assemble and test the product. However, during the worldwide pandemic, the strain on the overall supply chain for any product has been stretched to the breaking point.

Maggie Benson's Journey: An 'Engaging' Conversation

In this month's column, Andy and Sue prepare to take two journeys—one to Mexico to tour a facility that Maggie is interested in buying, and one of a more personal nature that will mean a more permanent union between them both. It's an exciting time in the lives of these two young professionals.



The 'Intel' on Advanced Packaging Options



Dr. Tom Rucker is vice president in technology development at Intel and was a keynote speaker at the IPC Advanced Packaging Symposium, which helped set the table for the rest of the agenda.

Tom understands this “radical and seismic” shift in terms of technology and breaks down what it means for the semiconductor and PCB fab industries. There's absolutely a place at the table for PCB fabricators.

Material Management and Control

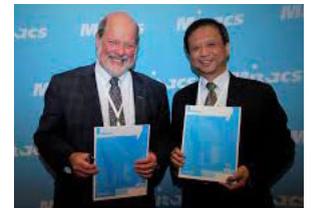
In a market that is trying to catch up with increasing customer demands and quickly ship products out the back door, no electronics manufacturing plant can afford to lose any time or resources during the production process.

Knocking Down the Bone Pile: Eliminating Solder Balls in Hand Soldering

While solder balls can be produced during both SMT reflow and wave soldering, PCB hand soldering during touch up or rework can also result in solder ball formation. When moisture or other impurities entrapped in or on the surface of the PCB or component outgas during the hand soldering process, solder balls form.

Mitacs, Hon Hai Research Institute Announce New Canadian Quantum Research Project

Mitacs, a non-profit organization committed to fostering innovation in Canada, and Hon Hai Research Institute, the research arm of Hon Hai Technology Group, signed a memorandum of understanding to advance quantum technology in Canada, with the active support of the Canadian Trade Office in Taipei.



For the latest news and information, visit SMT007.com

Career Opportunities



Find industry-experienced candidates at jobConnect007.

For just \$750, your 200-word, full-column ad will appear in the Career Opportunities section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs, suppliers and the academic community.

In addition, your ad will:

- be featured in at least one of our newsletters
- appear on our jobConnect007.com board, which is promoted in every newsletter
- appear in our monthly [Careers Guide](#), emailed to 26,000 potential candidates

Potential candidates can click on your ad and submit a resume directly to the email address you provide, or be directed to the URL of your choice.

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GOOD FOR THE INDUSTRY



Career Opportunities



Technical Sales Manager

Objectives

Provide sales leadership and management for a regional sales territory. Responsible for retaining current customers as well as developing and attracting new customers and markets. Responsible for selling current and new products, keeping abreast of new technologies, market trends, and customer product needs.

Essential Functions and Responsibilities

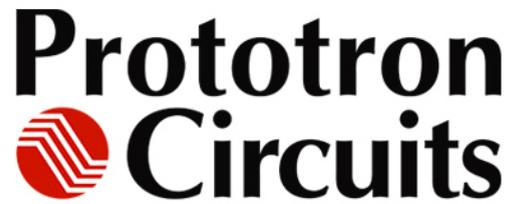
- Develop and service assigned geographic region
- Actively and consistently seek new customers
- Visit customers and potential customers to develop relationships, deliver sales presentations, follow up on leads, and close sales
- Provide technical support and product recommendations in person, by email, and phone
- Manage major accounts; establish long-term, ongoing relationships with key individuals
- Provide feedback to Chemcut as well as sales peers regarding competition, pricing, and marketing opportunities

Qualifications

- Bachelor's degree in mechanical, electrical, chemical engineering or related fields
- 3-5 years of field sales experience with technology driven industrial products
- Well-developed sales and customer relations skills
- Ability to make decisions and evaluations to determine customer needs
- Ability to travel up to 50% of the time
- Excellent oral and written communication skills
- Knowledge of target market industries

To apply, please submit a cover letter and resume to hr@chemcut.net.

[apply now](#)



Sales Representatives

Prototron Circuits, a market-leading, quick-turn PCB manufacturer located in Tucson, AZ, is looking for sales representatives for the Utah/Colorado, and Northern California territories. With 35+ years of experience, our PCB manufacturing capabilities reach far beyond that of your typical fabricator.

Reasons you should work with Prototron:

- Solid reputation for on-time delivery (98+% on-time)
- Capacity for growth
- Excellent quality
- Production quality quick-turn services in as little as 24 hours
- 5-day standard lead time
- RF/microwave and special materials
- AS9100D
- MIL-PRF- 31032
- ITAR
- Global sourcing option (Taiwan)
- Engineering consultation, impedance modeling
- Completely customer focused team

Interested? Please contact Russ Adams at (206) 351-0281 or russa@prototron.com.

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Career Opportunities



Test Engineer, Electronics Engineer, and Senior PCB Designer

Keytronic is a dynamic, team-based contract manufacturer with facilities worldwide. Innovation defines us. Come join us in Spokane, Washington! We invite you to bring your engineering expertise and passion for excellence. In turn, we provide meaningful opportunities for you to implement these attributes to their fullest while working together to bring our customer's high-tech automotive, aerospace, medical and commercial products to full production.

We encourage you to apply to one of our open positions below if you enjoy being challenged, working in a dynamic work setting and being a part of a team creating products to improve our world.

- **Test Engineer**—You will assist in conducting electrical test engineering support involving automation, assembly, maintenance, and data collection.
- **Electronics Engineer**—You will work on a team creating electronic circuitry, writing firmware for microprocessors and interfacing with customer development teams producing a wide array of products.
- **Senior PCB Designer**—You will perform PCB layout and documentation of complex printed circuit assembly products as part of a project team including procurement, electrical & mechanical engineering, PCB fabrication, Assembly and Test engineering stakeholders.

To learn more and apply for any of these openings please visit keytronic.com/join-us or email your resume to: llitsheim@keytronic.com.

apply now



Regional Manager Midwest Region

General Summary: Manages sales of the company's products and services, Electronics and Industrial, within the Carolinas and Mid-Atlantic Region. Reports directly to Americas Manager. Collaborates with the Americas Manager to ensure consistent, profitable growth in sales revenues through positive planning, deployment and management of sales reps. Identifies objectives, strategies and action plans to improve short- and long-term sales and earnings for all product lines.

DETAILS OF FUNCTION:

- Develops and maintains strategic partner relationships
- Manages and develops sales reps:
 - Reviews progress of sales performance
 - Provides quarterly results assessments of sales reps' performance
 - Works with sales reps to identify and contact decision-makers
 - Setting growth targets for sales reps
 - Educates sales reps by conducting programs/ seminars in the needed areas of knowledge
- Collects customer feedback and market research (products and competitors)
- Coordinates with other company departments to provide superior customer service

QUALIFICATIONS:

- 5-7+ years of related experience in the manufacturing sector or equivalent combination of formal education and experience
- Excellent oral and written communication skills
- Business-to-business sales experience a plus
- Good working knowledge of Microsoft Office Suite and common smart phone apps
- Valid driver's license
- 75-80% regional travel required

To apply, please submit a COVER LETTER and RESUME to: Fernando Rueda, Americas Manager

fernando_rueda@kyzen.com

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Career Opportunities



Field Service Technician

Taiyo Circuit Automation designs and manufactures the world's finest dual sided soldermask coating and vertical drying equipment. Since 1981, we have served the printed circuit board industry with highly reliable innovative machinery, engineered to exceed.

PRIMARY FUNCTION:

The Field Service Technician is responsible for troubleshooting and providing technical services on Taiyo Circuit Automation's mechanical and electro-mechanical products and systems.

ESSENTIAL DUTIES:

1. Identify mechanical issues and implement process control solutions for process improvement and new projects
2. Consult with maintenance, operations, engineering, and management concerning process control and instrumentation
3. Specify, install, configure, calibrate, and maintain instrumentation, control system and electrical protection equipment

QUALIFICATIONS/SKILLS:

1. 3 years of experience with equipment, preferably in PCB or related electronics industry
2. 3 years of experience in similar process industries with hands-on experience in operations, maintenance and project implementation—OMRON, Koyo, Allen Bradley experience preferred
3. Experience in installation and calibration of process control elements and electrical measurement devices
4. The ability to read and understand electrical, pneumatic diagrams and control systems

REQUIRED EDUCATION/EXPERIENCE:

1. High school graduate
2. Associate degree in Industrial Engineering Technology, Mechanical or Electrical Engineering, preferred.
3. PLC experience

Email: BobW@Taiyo-america.com (Subject: "Application for Field Service Technician for TCA")

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Application Engineer

Flexible Circuit Technologies (FCT) is a global supplier providing design, prototyping and production of flexible circuits, rigid flex circuits, flexible heaters and full assembly services.

Responsibilities

- Gain understanding for customer/specific project requirements
- Review customer files, analyze - application, design, stack up, materials, mechanical requirements; develop cost-effective design to meet requirements
- Quote and follow-up to secure business
- Work with CAD: finalize files, attain customer approval prior to build
- Track timeline/provide customers with updates
- Follow up on prototype, assist with design changes (if needed), and push forward to production
- Work as the lead technician/program manager or as part of FCT team working with an assigned application engineer
- Help customer understand FCT's assembly, testing, and box build services
- Understand manufacturing and build process for flexible and rigid-flex circuits

Qualifications

- Demonstrated experience: flex circuit/rigid-flex design including design rules, IPC; flex heater design +
- Ability to work in fast-paced environment, broad range of projects, maintain sense of urgency
- Ability to work as a team player
- Excellent written and verbal communication skills
- Willing to travel for sales support and customer support activities if needed

Competitive salary, bonus program, and benefits package. Preferred location Minneapolis, MN area.

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Career Opportunities



Technical Marketing Engineer

EMA Design Automation, a leader in product development solutions, is in search of a detail-oriented individual who can apply their knowledge of electrical design and CAD software to assist marketing in the creation of videos, training materials, blog posts, and more. This Technical Marketing Engineer role is ideal for analytical problem-solvers who enjoy educating and teaching others.

Requirements:

- Bachelor's degree in electrical engineering or related field with a basic understanding of engineering theories and terminology required
- Basic knowledge of schematic design, PCB design, and simulation with experience in OrCAD or Allegro preferred
- Candidates must possess excellent writing skills with an understanding of sentence structure and grammar
- Basic knowledge of video editing and experience using Camtasia or Adobe Premiere Pro is preferred but not required
- Must be able to collaborate well with others and have excellent written and verbal communication skills for this remote position

EMA Design Automation is a small, family-owned company that fosters a flexible, collaborative environment and promotes professional growth.

Send Resumes to: resumes@ema-eda.com

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MACHINES FOR PRINTED CIRCUIT BOARDS

Field Service Engineer

Location: West Coast, Midwest

Pluritec North America, Ltd., an innovative leader in drilling, routing, and automated inspection in the printed circuit board industry, is seeking a full-time field service engineer.

This individual will support service for North America in printed circuit board drill/routing and x-ray inspection equipment.

Duties included: Installation, training, maintenance, and repair. Must be able to troubleshoot electrical and mechanical issues in the field as well as calibrate products, perform modifications and retrofits. Diagnose effectively with customer via telephone support. Assist in optimization of machine operations.

A technical degree is preferred, along with strong verbal and written communication skills. Read and interpret schematics, collect data, write technical reports.

Valid driver's license is required, as well as a passport, and major credit card for travel.

Must be able to travel extensively.

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Career Opportunities



ventec
INTERNATIONAL GROUP
騰輝電子

European Product Manager Taiyo Inks, Germany

We are looking for a European product manager to serve as the primary point of contact for product technical sales activities specifically for Taiyo Inks in Europe.

Duties include:

- Business development & sales growth in Europe
- Subject matter expert for Taiyo ink solutions
- Frequent travel to targeted strategic customers/OEMs in Europe
- Technical support to customers to solve application issues
- Liaising with operational and supply chain teams to support customer service

Skills and abilities required:

- Extensive sales, product management, product application experience
- European citizenship (or authorization to work in Europe/Germany)
- Fluency in English language (spoken & written)
- Good written & verbal communications skills
- Printed circuit board industry experience an advantage
- Ability to work well both independently and as part of a team
- Good user knowledge of common Microsoft Office programs
- Full driving license essential

What's on offer:

- Salary & sales commission--competitive and commensurate with experience
- Pension and health insurance following satisfactory probation
- Company car or car allowance

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits. Please forward your resume to jobs@ventec-europe.com.

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**KOH
YOUNG
AMERICA**

Technical Service & Applications Engineer Full-Time – Midwest (WI, IL, MI)

Koh Young Technology, founded in 2002 in Seoul, South Korea, is the world leader in 3D measurement-based inspection technology for electronics manufacturing. Located in Duluth, GA, Koh Young America has been serving its partners since 2010 and is expanding the team with an Applications Engineer to provide helpdesk support by delivering guidance on operation, maintenance, and programming remotely or on-site.

Responsibilities

- Provide support, preventive and corrective maintenance, process audits, and related services
- Train users on proper operation, maintenance, programming, and best practices
- Recommend and oversee operational, process, or other performance improvements
- Effectively troubleshoot and resolve machine, system, and process issues

Skills and Qualifications

- Bachelor's in a technical discipline, relevant Associate's, or equivalent vocational or military training
- Knowledge of electronics manufacturing, robotics, PCB assembly, and/or AI; 2-4 years of experience
- SPI/AOI programming, operation, and maintenance experience preferred
- 75% domestic and international travel (valid U.S. or Canadian passport, required)
- Able to work effectively and independently with minimal supervision
- Able to readily understand and interpret detailed documents, drawings, and specifications

Benefits

- Health/Dental/Vision/Life Insurance with no employee premium (including dependent coverage)
- 401K retirement plan
- Generous PTO and paid holidays

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Career Opportunities



Arlon EMD, located in Rancho Cucamonga, California, is currently interviewing candidates for open positions in:

- Engineering
- Quality
- Various Manufacturing

All interested candidates should contact Arlon's HR department at 909-987-9533 or email resumes to careers.ranch@arlonemd.com.

Arlon is a major manufacturer of specialty high-performance laminate and prepreg materials for use in a wide variety of printed circuit board applications. Arlon specializes in thermoset resin technology, including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, High Density Interconnect (HDI) and microvia PCBs (i.e. in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2015 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customers' requirements.

For additional information please visit our website at www.arlonemd.com

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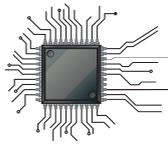
Are You Our Next Superstar?!

Insulectro, the largest national distributor of printed circuit board materials, is looking to add superstars to our dynamic technical and sales teams. We are always looking for good talent to enhance our service level to our customers and drive our purpose to enable our customers to build better boards faster. Our nationwide network provides many opportunities for a rewarding career within our company.

We are looking for talent with solid background in the PCB or PE industry and proven sales experience with a drive and attitude that match our company culture. This is a great opportunity to join an industry leader in the PCB and PE world and work with a terrific team driven to be vital in the design and manufacture of future circuits.

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Career Opportunities



MivaTek

Global

Field Service Technician

MivaTek Global is focused on providing a quality customer service experience to our current and future customers in the printed circuit board and microelectronic industries. We are looking for bright and talented people who share that mindset and are energized by hard work who are looking to be part of our continued growth.

Do you enjoy diagnosing machines and processes to determine how to solve our customers' challenges? Your 5 years working with direct imaging machinery, capital equipment, or PCBs will be leveraged as you support our customers in the field and from your home office. Each day is different, you may be:

- Installing a direct imaging machine
- Diagnosing customer issues from both your home office and customer site
- Upgrading a used machine
- Performing preventive maintenance
- Providing virtual and on-site training
- Updating documentation

Do you have 3 years' experience working with direct imaging or capital equipment? Enjoy travel? Want to make a difference to our customers? Send your resume to N.Hogan@MivaTek.Global for consideration.

More About Us

MivaTek Global is a distributor of Miva Technologies' imaging systems. We currently have 55 installations in the Americas and have machine installations in China, Singapore, Korea, and India.

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Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

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- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

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- Training and certifications provided and maintained by EPTAC

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Career Opportunities



Rewarding Careers

Take advantage of the opportunities we are offering for careers with a growing test engineering firm. We currently have several openings at every stage of our operation.

The Test Connection, Inc. is a test engineering firm. We are family owned and operated with solid growth goals and strategies. We have an established workforce with seasoned professionals who are committed to meeting the demands of high-quality, low-cost and fast delivery.

TTCI is an Equal Opportunity Employer. We offer careers that include skills-based compensation. We are always looking for talented, experienced test engineers, test technicians, quote technicians, electronics interns, and front office staff to further our customer-oriented mission.

Associate Electronics Technician/Engineer (ATE-MD)

TTCI is adding electronics technician/engineer to our team for production test support.

- Candidates would operate the test systems and inspect circuit card assemblies (CCA) and will work under the direction of engineering staff, following established procedures to accomplish assigned tasks.
- Test, troubleshoot, repair, and modify developmental and production electronics.
- Working knowledge of theories of electronics, electrical circuitry, engineering mathematics, electronic and electrical testing desired.
- Advancement opportunities available.
- Must be a US citizen or resident.

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Test Engineer (TE-MD)

In this role, you will specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly HP) and/or Teradyne (formerly GenRad) TestStation/228X test systems.

- Candidates must have at least three years of experience with in-circuit test equipment. A candidate would develop and debug our test systems and install in-circuit test sets remotely online or at customer's manufactur-

ing locations nationwide.

- Candidates would also help support production testing and implement Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks.
- Some travel required and these positions are available in the Hunt Valley, Md., office.

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Sr. Test Engineer (STE-MD)

- Candidate would specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly Agilent & HP), Teradyne/GenRad, and Flying Probe test systems.
- Strong candidates will have more than five years of experience with in-circuit test equipment. Some experience with flying probe test equipment is preferred. A candidate would develop, and debug on our test systems and install in-circuit test sets remotely online or at customer's manufacturing locations nationwide.
- Proficient working knowledge of Flash/ISP programming, MAC Address and Boundary Scan required. The candidate would also help support production testing implementing Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks. An understanding of stand-alone boundary scan and flying probe desired.
- Some travel required. Positions are available in the Hunt Valley, Md., office.

Contact us today to learn about the rewarding careers we are offering. Please email resumes with a short message describing your relevant experience and any questions to careers@ttci.com. Please, no phone calls.

We proudly serve customers nationwide and around the world.

TTCI is an ITAR registered and JCP DD2345 certified company that is NIST 800-171 compliant.

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Career Opportunities



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Job Description

This position is responsible for delivering effective electronics manufacturing training, including IPC Certification, to students from the electronics manufacturing industry. IPC instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC Certification Programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will conduct training at one of our public training centers or will travel directly to the customer's facility. A candidate's close proximity to Longmont, CO, or Phoenix, AZ, is a plus. Several IPC Certification Courses can be taught remotely and require no travel.

Qualifications

Candidates must have a minimum of five years of electronics manufacturing experience. This experience can include printed circuit board fabrication, circuit board assembly, and/or wire and cable harness assembly. Soldering experience of through-hole and/or surface-mount components is highly preferred.

Candidate must have IPC training experience, either currently or in the past. A current and valid certified IPC trainer certificate holder is highly preferred.

Applicants must have the ability to work with little to no supervision and make appropriate and professional decisions.

Send resumes to Sharon Montana-Beard at
sharonm@blackfox.com.

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American Standard Circuits

Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, penalization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

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Career Opportunities



U.S. CIRCUIT

Plating Supervisor

Escondido, California-based PCB fabricator U.S. Circuit is now hiring for the position of plating supervisor. Candidate must have a minimum of five years' experience working in a wet process environment. Must have good communication skills, bilingual is a plus. Must have working knowledge of a plating lab and hands-on experience running an electrolytic plating line. Responsibilities include, but are not limited to, scheduling work, enforcing safety rules, scheduling/maintaining equipment and maintenance of records.

Competitive benefits package.

Pay will be commensurate with experience.

Mail to:
mfariba@uscircuit.com

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APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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Jan. 24-26

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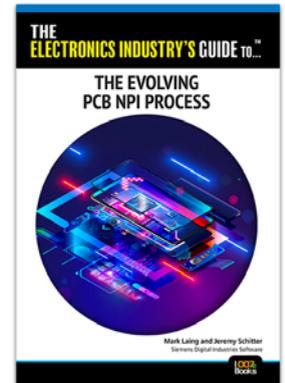
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MEET AND GREET AT OUR SOCIAL RECEPTIONS INCLUDING THE NEW CAREER CONNECTIONS NETWORKING EVENT WEDNESDAY, JANUARY 25!

The Electronics Industry's Guide to... The Evolving PCB NPI Process

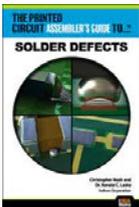
by Mark Laing and Jeremy Schitter, Siemens Digital Industries Software

In this book, the authors look at how market changes in the past 15 years, plus the slowdown of production and delivery of materials and components in recent years, have affected the process for new product introduction (NPI) in the global marketplace. As a result, we feel that PCB production companies need to adapt and take a new direction to navigate and thrive in an uncertain and rapidly evolving future.



I-007e
Books

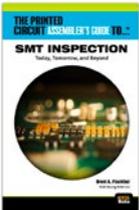
The Printed Circuit Assembler's Guide to...



Solder Defects

by Christopher Nash and Dr. Ronald C. Lasky, Indium Corporation

This book is specifically dedicated to educating the printed circuit board assembly sector and serves as a valuable resource for people seeking the most relevant information available.



SMT Inspection: Today, Tomorrow, and Beyond

by Brent Fischthal, Koh Young America

An in-depth insight into new and exciting true 3D inspection technology is provided in this book, along with a look into the future of leveraging big data management and autonomous manufacturing for a smarter factory.



Smart Data: Using Data to Improve Manufacturing

by Sagi Reuven and Zac Elliott, Siemens Digital Industries Software

Manufacturers need to ensure their factory operations work properly, but analyzing data is simply not enough. Companies must take efficiency and waste-reduction efforts to the next phase using big data and advanced analytics to diagnose and correct process flaws.



Process Validation

by Graham K. Naisbitt, Gen3

This book explores how establishing acceptable electrochemical reliability can be achieved by using both CAF and SIR testing. This is a must-read for those in the industry who are concerned about ECM and want to adopt a better and more rigorous approach to ensuring electrochemical reliability.



Advanced Manufacturing in the Digital Age

by Oren Manor, Siemens Digital Industries Software

A must-read for anyone looking for a holistic, systematic approach to leverage new and emerging technologies. The benefits are clear: fewer machine failures, reduced scrap and downtime issues, and improved throughput and productivity.

Our library is open 24/7/365. Visit us at: I-007eBooks.com

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