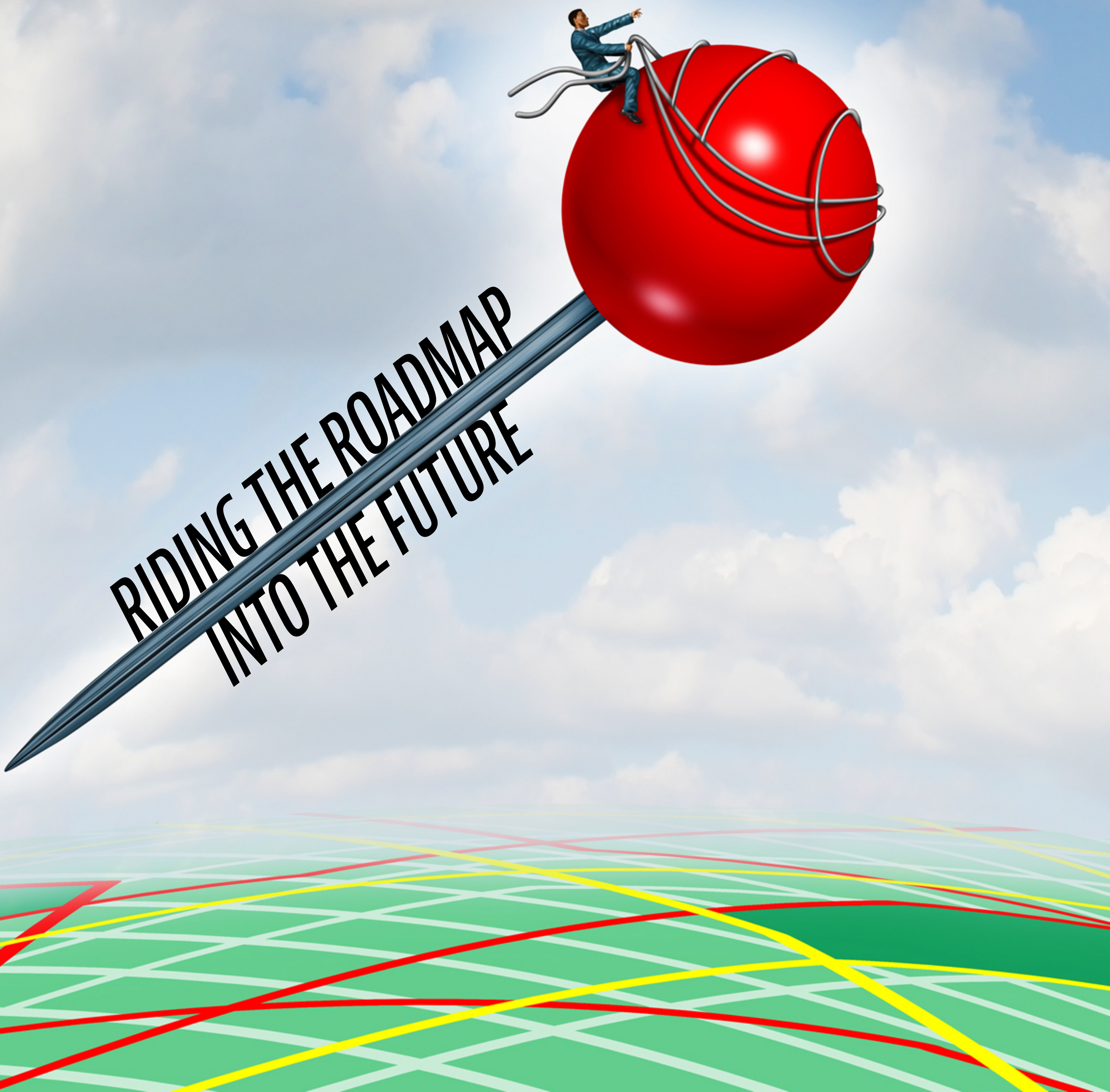
OCTOBER 2020

I-Connect007
GOOD FOR THE INDUSTRY

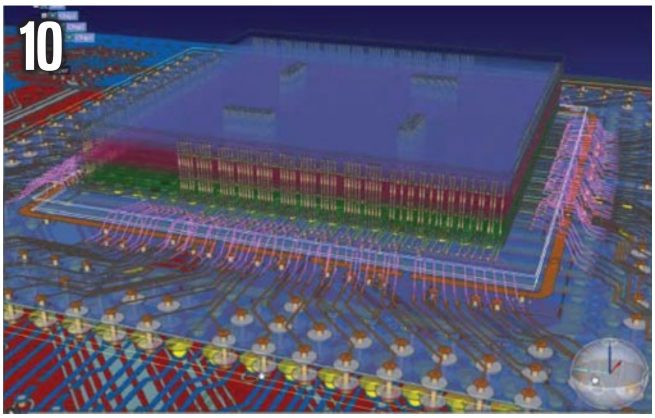
PCB007 MAGAZINE

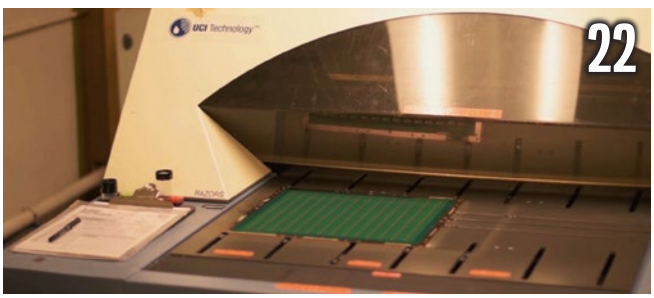


PCB007 MAGAZINE

Roadmaps: Into the Future

I-Connect007 has been exploring the effect of roadmaps on business planning and operations. As we conclude our three-part coverage of the IEEE Heterogeneous Integration Roadmap, we explore roadmapping as a tactical tool, not only a long-range strategic plan.





FEATURES:

FEATURE COLUMNS:

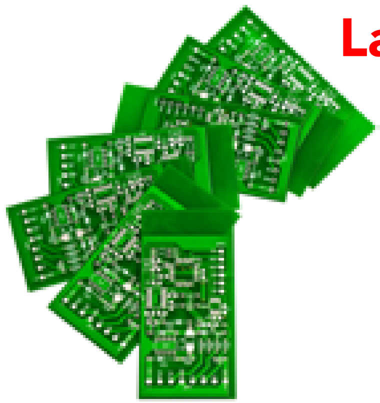
INSULECTRO

WORLD-CLASS SUPPLIERS

Insulectro, the largest distributor in North America of materials used in the manufacture of printed circuit boards and printed electronics, salutes our premier suppliers.

CALL 949.587.3200 FOR MORE INFORMATION

PACOTHANE TECHNOLOGIES



Lamination Assist For Flex & Rigid PCBs

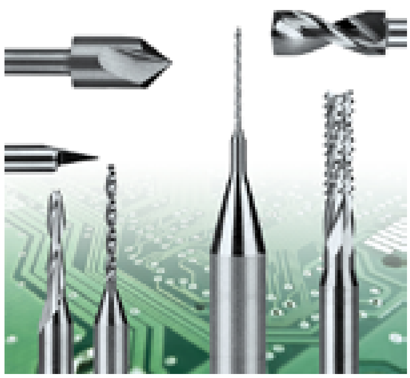
PACOTHANE TECHNOLOGIES is the world's leading manufacturer of products to enhance and assist the production and quality assurance process for the lamination and manufacture of printed circuit boards [PCB].

Providing innovative lamination processing solutions including TRIPAK (PACOTHERM™), a releasable Press Pad that is specifically engineered to control the variables associated with the lamination processes.

Denkai America

Denkai America is a leader in the manufacture of high-quality electrodeposited copper foils for printed circuit board (PCB), industrial, and energy storage applications. With the strength of domestic manufacturing, and backed by a global presence, Denkai America delivers both conventional cladding and application specific copper foils.

KEMMER PRÄZISION



High precision tools for processing printed circuit board: Drills, Routers, & Endmills.

TADCO

Let us Make a World of Difference!

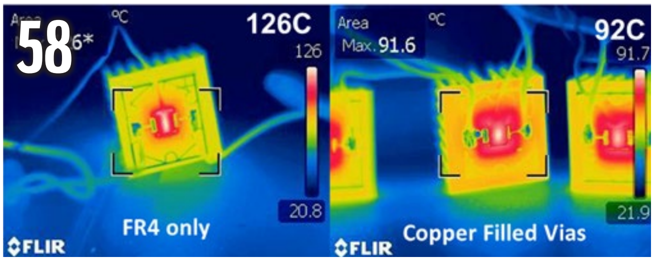
TADCO PRODUCTS: the most precise Lamination Tooling in the industry.

- **Lamination Plates,**
- **Precision Pins & Bushings**
- **Release Agents**
- **Pin Cleaners**
- **Brushes**

Precision is our specialty!

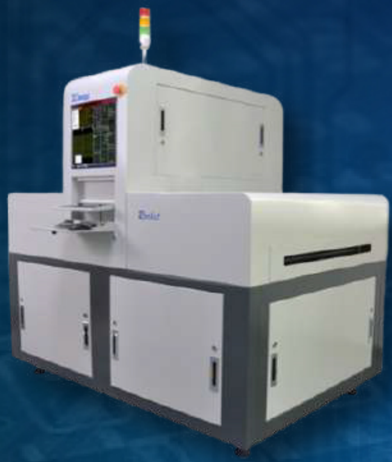
OCTOBER 2020 • ADDITIONAL CONTENT

PCB007 MAGAZINE



FINAL INSPECTION AT THE HIGHEST STANDARDS

Gardien



AVI Rocket

GET MORE INFO

AVI Leo

GET MORE INFO

AVI SMART

GET MORE INFO

FOR EVERY NEED THE PERFECT SOLUTION

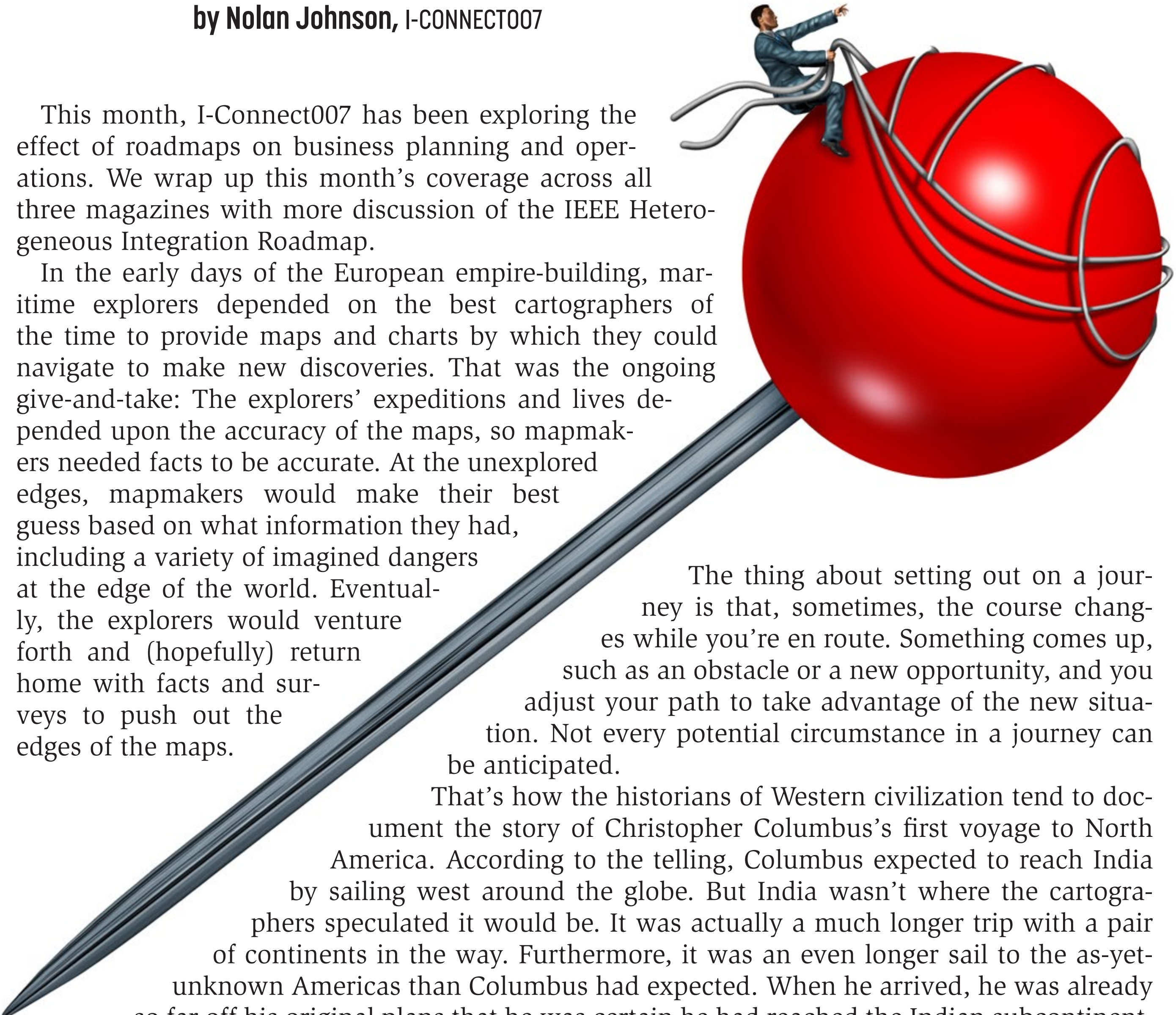
- Largest board to be handled in the range
- Smallest feature / highest resolution
- Simple data preparation
- Offline verification with error code database
- No material limitations
- Range from affordable single-camera single-side to multiple cameras double-sided fully automated solution

Want to learn more?

COMPLETE AVI SMART SERIES INFO

Roadmaps in Uncharted Territory

Nolan's Notes
by Nolan Johnson, I-CONNECT007



This month, I-Connect007 has been exploring the effect of roadmaps on business planning and operations. We wrap up this month's coverage across all three magazines with more discussion of the IEEE Heterogeneous Integration Roadmap.

In the early days of the European empire-building, maritime explorers depended on the best cartographers of the time to provide maps and charts by which they could navigate to make new discoveries. That was the ongoing give-and-take: The explorers' expeditions and lives depended upon the accuracy of the maps, so mapmakers needed facts to be accurate. At the unexplored edges, mapmakers would make their best guess based on what information they had, including a variety of imagined dangers at the edge of the world. Eventually, the explorers would venture forth and (hopefully) return home with facts and surveys to push out the edges of the maps.

The thing about setting out on a journey is that, sometimes, the course changes while you're en route. Something comes up, such as an obstacle or a new opportunity, and you adjust your path to take advantage of the new situation. Not every potential circumstance in a journey can be anticipated.

That's how the historians of Western civilization tend to document the story of Christopher Columbus's first voyage to North America. According to the telling, Columbus expected to reach India by sailing west around the globe. But India wasn't where the cartographers speculated it would be. It was actually a much longer trip with a pair of continents in the way. Furthermore, it was an even longer sail to the as-yet-unknown Americas than Columbus had expected. When he arrived, he was already so far off his original plans that he was certain he had reached the Indian subcontinent.

I wonder what it was like for him the moment he fully realized where he made landfall. How did he respond to that massive paradigm shift?

I recently saw this in action. The I-Connect007 team recently finished covering the SMTA International conference and tradeshow in its 2020 virtual format. Hats off to the SMTA staff for their perseverance and can-do attitude in choosing to hold SMTAI as a virtual conference and exposition. The pandemic changed the landscape under all of us.

SMTA responded by making a new roadmap rather than abandoning the event altogether. Similar to Columbus, the SMTA crew consciously chose to go into new, uncharted territory to deliver on their original objective, no matter the challenges. This changed the roadmaps for virtually every individual and company participating in the event. Ours was a very different worldview in the virtual tradeshow environment.

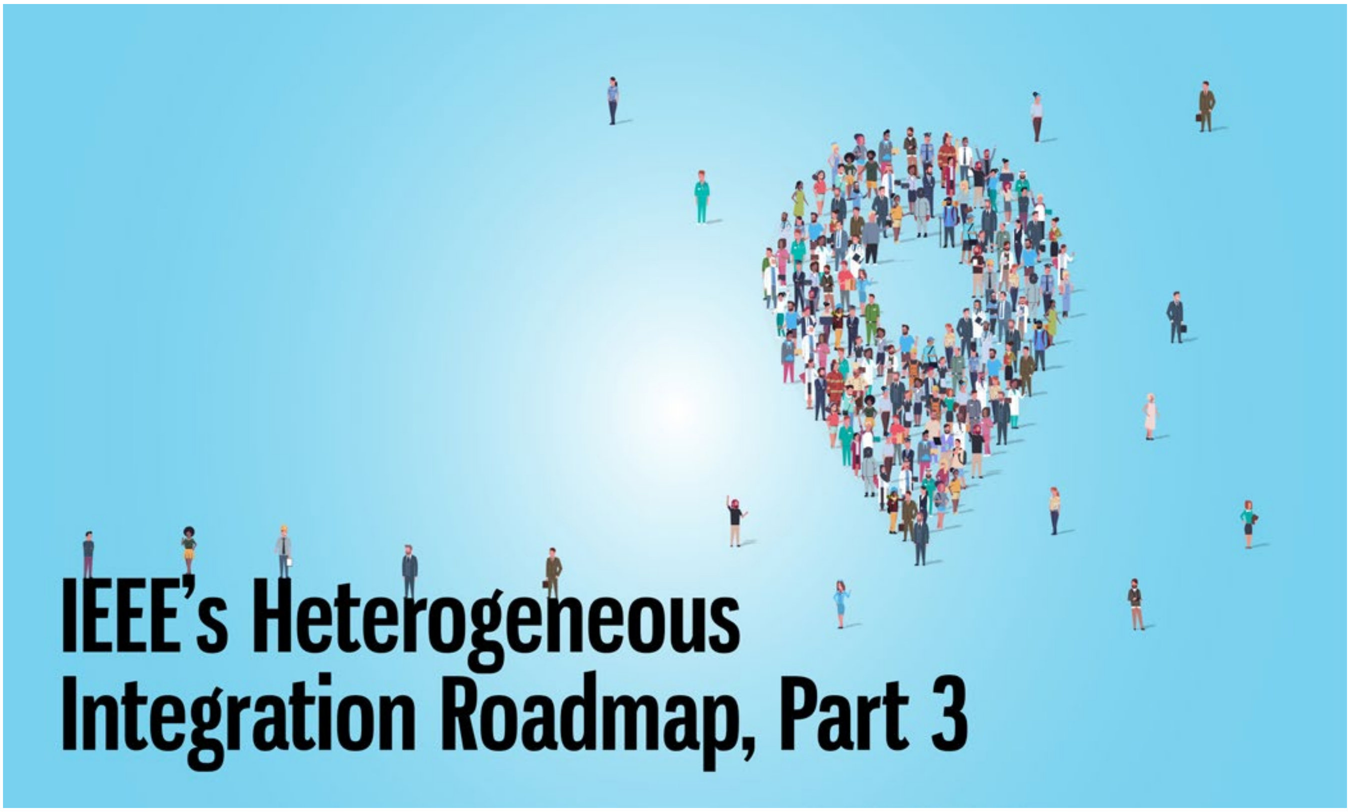
In this issue, we conclude our three-part interview with Rita Horner on the significance of the IEEE's Heterogeneous Integration Roadmap. MacDermid Alpha weighs in with an article that considers the impact heterogeneous integration will have on substrate metallization, and Dr. John Mitchell's column ponders "Navigating Around the Future."

We also talk to a fabricator—Sunstone Circuits—about how they use roadmapping for strategic planning, and we share technical research on plating issues that have a direct tie to the fabrication demands that heterogeneous integration will ultimately bring to the industry.

Pete Starkey talks with Taiyo's Don Monn. George Milad posts a discussion on plating pretreatment. Todd Kolmodin and Michael Carano post their columns, and Marc Carter shares an article on reliability. Graham Naisbitt considers IPC standards development, and Dan Feinberg charts the changing velocities in technology innovation.

This issue's thoughtful, pragmatic, and sometimes philosophical take on roadmapping—combined with our discussion of the topic in the October issues of *SMT007 Magazine* and *Design007 Magazine*—concludes our roadmap coverage. As always, we welcome your suggestions, comments, and ideas. I-Connect007's mission is to publish content that advances the conversations in our industry; if you're talking about it, we want to cover it, so let us know. **PCB007**

Nolan Johnson is managing editor of *PCB007 Magazine*. Nolan brings 30 years of career experience focused almost entirely on electronics design and manufacturing.
To contact Johnson, click here.



IEEE's Heterogeneous Integration Roadmap, Part 3

Feature Interview by the I-Connect007 Editorial Team

In Part 1 and Part 2 of this conversation, Rita Horner of Synopsys provided a general overview of the IEEE Heterogeneous Integration Roadmap (HIR)—a document that provides guidance for IC, PCB, and package designers, broken down by industry segment and performance requirements. Rita also shares her perspective from the IC side, as well as how the HIR might affect what happens on the PCB design and manufacturing side in the next few years. Here, we share the final segment of this interview series.

Happy Holden: In creating a roadmap, the IEEE is talking about the needs over time for performance and then trying to expose the gap. The HIR isn't telling us the solution, but it is telling us what is needed and what we have to work with from right now going forward. The various chapters explain where each part of the industry is right now. Our interest in it is we know that people have made the silicon interposers work, but they can be expensive, so you have glass coming up because of its density, low cost, and very large panel size.

Right now, common PCBs are getting to be 50- and 60-micron geometries. Twenty years ago, that was semiconductor geometry, but now it's PCB geometry. Ten years from now, we may be talking about PCBs that are micron or sub-micron geometry because it all just keeps rolling down the hill.

Rita Horner: Right. People need to participate. Like any other standard, it's contribution-driven. If you are interested in a certain market space—like 5G, aerospace, or high-performance computing—join those groups to provide input and learn. Every one of these markets has different needs. They face various levels of trade-offs between technological and economic challenges that HIR is trying to address for that market space. The HIR is working on a roadmap. As Happy said, they're not giving an answer; they're just saying where the market is, what the market needs are, and what some of the challenges are.

In terms of 5G, it's very new. Since 5G took so long, it had a lot of challenges, and I would

think we learned a lot along the way. But it's not unusual for a standard to have a short life or even be skipped. It may take a long time; it may have a very short cycle or duration, and then the market may jump to adopting the next generation quickly.

I saw that in PCI Express. It took almost six or seven years to come up with one generation, and the next generation came within a year and a half because there was so much detail learning that was done while its previous generation was being defined. Moving from one generation to the next was so challenging that they had to do a lot of due diligence to get all the information that was used for the generation after.

Then, they started looking at all the different angles, and those areas opened up new insight in terms of improvement and maybe even skipping a generation. It's not unusual for some of these interfaces or definitions to be short-lived after it's taken so long to implement or define, and then the next step takes over quickly.

Holden: Why did the IEEE invest all this time in creating the HIR? Because I don't remember IEEE roadmaps before this. The overall consensus is that this is so important and going in many different directions that we need to have standards, and the IEEE pioneered and championed the standards. And whatever those standards are, the HIR roadmap indicates a greater need for those standards. Otherwise, we're going to have a Tower of Babel, and costs aren't going to come down.

Horner: Correct. If you look at the HIR, there's a lot of collaboration, even between the subtopics. Each has its own focus, but it's all under the same umbrella so that they can benefit from each other's knowledge and shared learnings.

Holden: If we're going to have multinational standards, without this kind of cooperation, people will create their own.

Rita Horner

Horner: Like when people can't speak the same language, misunderstanding happens. If the two ends of the interface don't follow the same specification, communication will not be effective.

Dan Feinberg: And just like with any other international group, that doesn't mean that what they're doing is going to be agreed upon by everybody.

Horner: Our CEO, Aart de Geus, gave a keynote at SEMICON West talking about globalization and coming together, and he said that we all need to collaborate and make this world a better place. There are many angles on many fronts.

Nolan Johnson: The collaboration that's necessary to make HIR type components work in the future becomes a part of the whole design process to make the design work. That's going to change the role of the fab house, and they're going to have to be more consultative and involved in the design process.

Horner: This die-to-die integration packaging is not going to be cheap. It's going to get more expensive as it becomes more complex. It needs to be collaborative to get the optimal solution, and that's the main driver for collaboration. The IC designer can design in their own IC silo, the board designer can design their board, and the package designer can design their package independent of the other disciplines. You cannot get to the market fast enough if you have to wait for the IC to be defined, designed, and characterized, and then design a package for it. That's how it used to be done. We can't afford to wait for a sequential implementation.

Johnson: That's going to change the way we do business. OEMs will need to line up with the fabricators early, be a part of the engineering team, and then manufacture it once they're done.

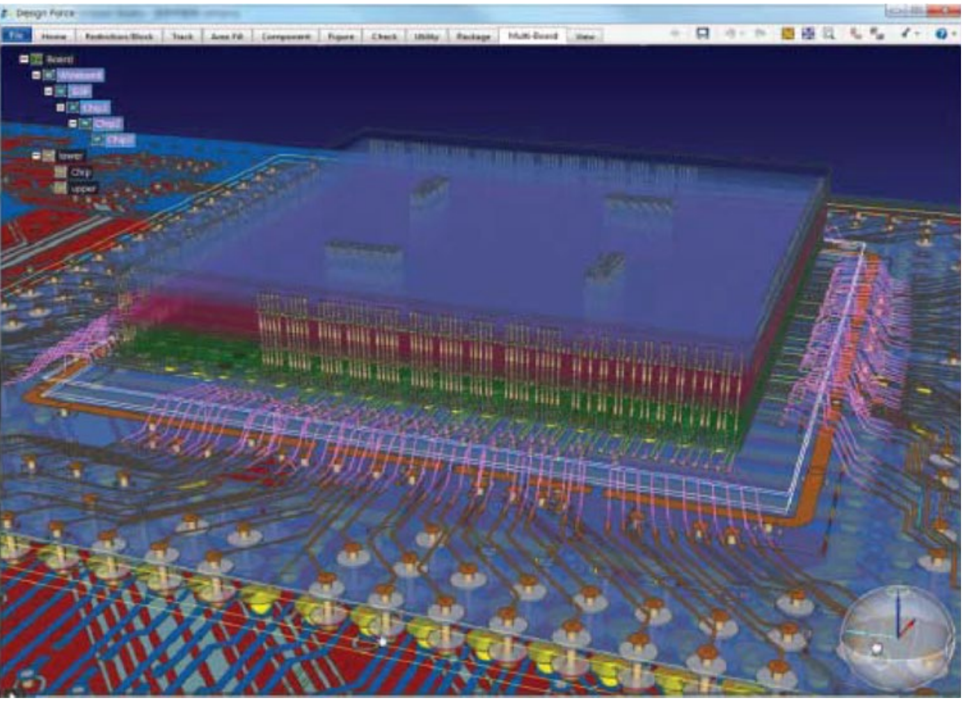


Figure 1: The need for heterogeneous integration has fostered interest in 3D stacking and packaging strategies. (Source: HIR 2019)

Horner: Time to market is becoming very critical. Catching up is getting harder and harder because technology is moving so fast, so being involved is critical. Some vendors are approaching this by just putting everything under the same umbrella. We see foundries doing the IC design, fabrication, and the package. Is that the right approach? I don't know. That would eliminate others from entering the market.

But at the same time, by having some of these standards or having tools that enable the collaboration, you can have a chance to succeed in having an optimal solution in a timely manager. By having unified interfaces, tools can talk to each other. That's another thing because when you have so many point tools, getting the information from one stage of the design to another stage gets inefficient. Most IC design tools do not communicate with PCB design tools. The PCB design tools are usually driven off of PCs using Microsoft operating systems, whereas IC designs run off Linux-based operating systems.

Johnson: If you have people with various job functions in different companies who need to talk together, then the design tools they use are going to need to enable that collaboration.

Horner: Right now, I see a big need around analysis, as I mentioned. I can model the PCB and extract the parasitic and the traces, model it, bring it into the same environment, and do an end-to-end analysis of my simulation. I can bring a clump of information that represents a PCB, another chunk of information that represents the package, and a chunk of information that represents the silicon and simulate all of them together.

This ensures that the signal that is intended to leave the silicon gets to the board and maybe to the other side or to another device, or whatever is supposed to drive a cable or something to somewhere else. Modeling becomes very critical. There are tools that allow you to do an extraction of either S-parameter models or SPICE extractive models that allow you to do a SPICE simulation or any of the other analysis that uses those inputs to do the simulations.

Johnson: You need to bring together the manufacturing supply chain as a part of the design process. Passing that information to all of those different domains of expertise is going to be important. Are we going to see heterogeneous integration chips in large scale consumer products?

Horner: We are moving to that. As I said, this is expensive, and it's very customized right now. But I envision that we are going to move to the consumer level. We're talking to people who are looking at some of the consumer-level applications. Automotive is going to need it as well. The need for high levels of performance and integration is driving us out of the single die concept. We're going to see exponential growth in the need for multi-die in a package. IoT already needs antennas and such, and

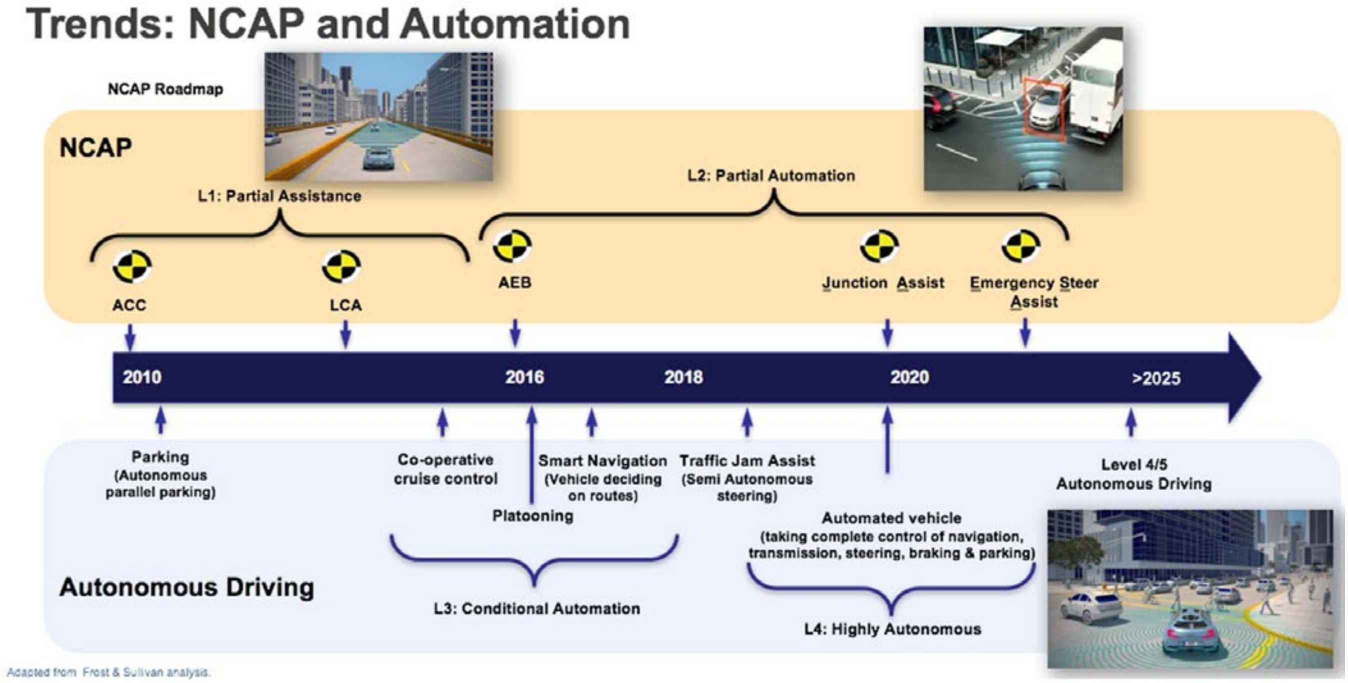


Figure 2: Five levels of autonomous driving and one example of a roadmap to 2025. (Source: HIR 2019)

there are many levels of IoT out there. It's going to be everywhere. High-performance OEMs are going to be the first adopters.

Autonomous vehicles are driving high levels of integration. When you cannot get the capability in one device, you have to integrate more. Cellphones are becoming more powerful than our desktop or laptop in a smaller device. Miniaturization is happening. If you have an iPhone, there's a 3D IC in it. If you have any of the later ones, they're already stacked devices. We are already using heterogeneous integration in even consumer applications. People are putting antennas on the same devices for many of these applications.

Andy Shaughnessy: What challenges do you think a CAD manager or PCB designer should know?

Horner: They need to maybe open their vocabulary horizon. Thermal is becoming critical. We used to put heat sinks on a package or have all this heating and cooling and the fans in a system to cool the different parts. Warpage is not limited to the package. The boards are warping because of the heat; they're delaminating devices off of the board. The HIR provides a map of all the potential issues that will surface. Maybe it's focusing more on the package level right now, but it's affecting the board level, too. Sooner or later, the package will become what the old PCB was.

Again, there are only so many of these 100- by 100-millimeter package parts these boards can handle in terms of the mechanical stress or the thermal impact. There may be multiples of these 100- by 100-millimeter square devices connected on one board. Is back drilling going to do it? No. Maybe blind vias are better. Those are some of the things that I'm thinking about on a high-speed side that are already being raised by a lot of high-end standards.

Holden: Who's going to create some of the tools that collaborate and lead that connection between these isolated silos? Is it going to be the OEMs because they want the final product, university students working on their Ph.D.s, or top EDA companies, which will begin as startups and then be bought by large EDA companies and incorporated into their tools?

Horner: The product that I manage is to bring unity to the fronts that can be managed. The tool brings our expertise on the die design, extraction, validation, and analysis capabilities of EDA tools to the package level. Without a defined standard, it's easier to allow people to continue with their silos and using point tools. Moving forward, we need more collaboration to get those end-to-end solutions in place. But to collaborate, you also need to define a standard language between the different pieces of the puzzle. There are attempts happening. Even IEEE is defining some of these interfaces. IEEE has 2401, which is defining the XML language that the data is transferred in. Over time, as people realize there is a need for collaboration, it's going to happen. And it's already happening on the die-to-die connection with the standard-based electrical specifications, all the way to the package. We need EDA tools that can easily be communicated to each other, from die level to package and PCB level, for faster design convergence.

Shaughnessy: Thanks for speaking with us, Rita. We appreciate it.

Horner: You're welcome. PCB007

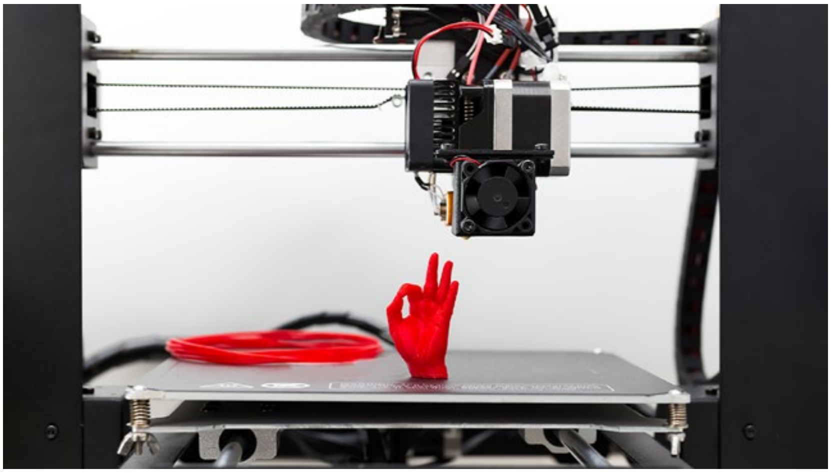
How to Make 3D Printing Better

With 3D-printing technologies increasingly becoming a mainstay in modern manufacturing operations, original equipment manufacturers (OEMs), software houses, 3D-printing factories, and contract manufacturers are striving to fine-tune the efficiency and repeatability of these production methods. Variability in the 3D printing of products has been a major concern of management for decades. Production engineers and managers pay special attention to product consistency with respect to dimensional accuracy and material properties, such as porosity, strength, temperature, and chemical resistance.

Current levels of consistency in 3D printing—also known as "additive manufacturing"—are sufficient for many products. They include molds, toys, dental devices, optical lenses, eyewear, printed circuit boards (PCBs), some antennae and sensors, and non-weight-bearing metal and plastic spare parts for locomotives, heavy industrial equipment, airplanes, and military equipment.

However, that is still a relatively small portion of the potential market where this manufacturing technology could be applied if the consistency of its output could be raised. Understanding this, the additive manufacturing industry is launching a full-scale assault on the problem. The assault is a three-pronged effort using hardware, software, and management systems to reduce the variability of the objects printed.

Hardware: It's hard to improve the output of 3D printing without considering the hardware of the printers themselves (e.g., motors, print heads, lasers), as well as hardware devices such as temperature sensors, humidity sensors, and X-ray cameras to monitor quality and catch errors layer by layer during the printing process. Velo3D, a Californian printer manufacturer, is one example of a company whose machines can monitor metal parts during the printing process. Through the use of sensors, its printers can be augmented with a system that monitors things such as oxygen levels, humidity, and unused powder levels. This level of visibility and control allows them to achieve higher yields and greater repeatability for many types of products without the need for post-processing (refining the product after it has come out of the 3D printer).



(Source: Richard A. D'Aveni and Ankush Venkatesh, Harvard Business Review)

Navigating Around the Future

One World, One Industry

Feature Column by Dr. John Mitchell, IPC—ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

Predicting the future is always dangerous. Happily, those predictions are rarely held to much scrutiny—perhaps because we all know that whatever is shared will, at least in some aspect, be wrong. There is much value in an ever-evolving conversation, enabling us to see and observe trends as well as the data that points to those trends. There are some paths that seem very likely, but the tricky bit is the timing. That being said, let me dip my toe into the world of prognostication for a little bit, but realize I know that nothing is certain.

There are several very exciting, game-changing electronics industry technologies at the forefront. Any one of these would merit days of exploration, but out of necessity, I will just barely scratch the surface of each. As Dr. Humphries, my EE professor, used to say, "I will leave the details of that problem up to the interested and dedicated student."

The development of true 5G communications, additive manufacturing, artificial intelligence, new materials (graphene and other nanomaterials), quantum computing, and others is happening as you read this. Any one of these areas individually has the potential to greatly impact the future of electronics, the economy, and how we live our daily lives. However, the combination of two or more of these technologies could have awe-inspiring, and potentially fundamental, shifts in the way electronics are both used and made.

As much as I am sure we would like to spend some time geeking out over what some of those potentials are, I only have so many words available, and we also have to discuss

some business shifts that will have as great an impact on our industry as upcoming technological advances.

The global marketplace is changing. How much or how drastically it will change remains to be seen. But let me share one scenario that I feel is likely. A great degree of distrust has risen up between countries and regions (e.g., Brexit and various tariff disputes). This unrest and distrust likely will result in more regional and national approaches to the building of electronics.

What might this look like? As more regional resiliency is desired, at a minimum, I expect a deeper expectation from the large component distributors to have more vast stores available regionally. A more costly approach also may be to create a local version of the total supply chain, so if something breaks down with a partner, local options could be expanded as required.

Given the tensions between nations, I expect this regional trend to last through the 2020s. After some time has passed and trust has been developed or enforced, the costliness of a heavy regional and local approach to manufacturing will become less tolerable, and a purer globalized supply chain will begin to advance once more. As a global association, we work closely with our international partners to maintain awareness of international events that affect the electronics industry.

As I mentioned earlier, the danger of predicting the future is that there are so many variables to consider. Think back to just last year. Those who thought 2020 would have the economic performance we've seen would have likely pointed to a tariff war or perhaps even actual war as the impetus that might cause such a shift. I don't know of anyone who predicted that we should watch out for a killer virus.

Because none of us can see into the future, we need a deep knowledge of our own industry, how it changes so rapidly, and how it reflects the upheaval in the world. When holding a roadmap that points to excessive change and disruption, we can more easily deal with those difficult situations as they arise. **PCB007**

Dr. John Mitchell is president and CEO of IPC. To read past columns or contact him, click here.

UCLA Scientists Create World's Smallest 'Refrigerator'

How do you keep the world's tiniest soda cold? UCLA scientists may have the answer.

A team led by UCLA physics professor Chris Regan has succeeded in creating thermoelectric coolers that are only 100 nanometers thick—roughly one ten-millionth of a meter—and have developed an innovative new technique for measuring their cooling performance.

"We have made the world's smallest refrigerator," said Regan, the lead author of a paper on the research published recently in the journal *ACS Nano*.

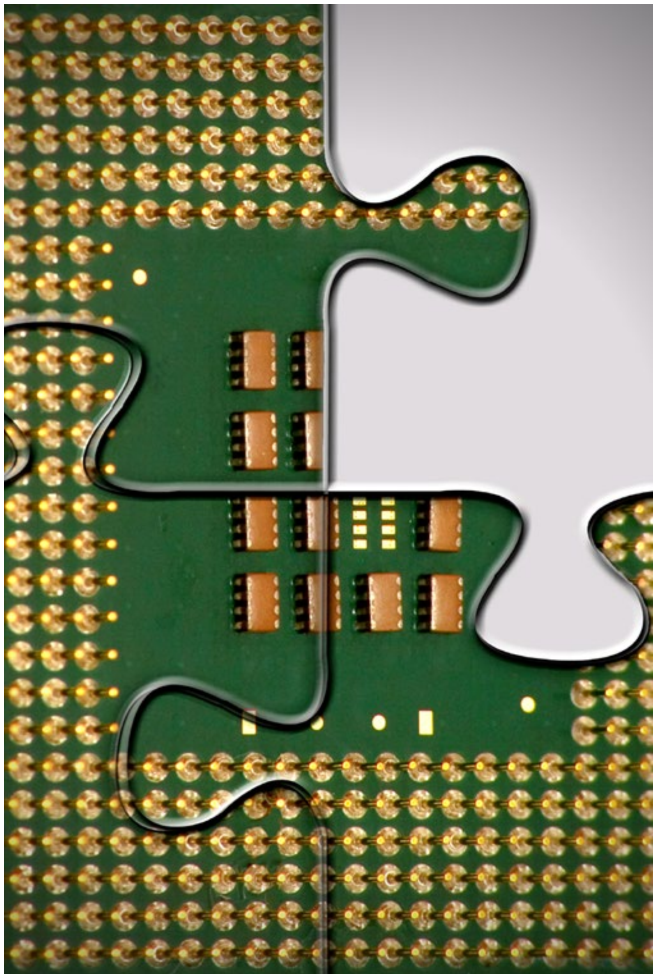
To be clear, these minuscule devices aren't refrigerators in the everyday sense–there are no doors or crisper drawers. But at larger scales, the same technology is used to cool computers and other electronic devices, to regulate the temperature in fiber-optic networks, and to reduce image "noise" in high-end telescopes and digital cameras.

Made by sandwiching two different semiconductors between metalized plates, these devices work in two ways. When heat is applied, one side becomes hot, and the other remains cool; that temperature difference can be used to generate electricity. The scientific instruments on NASA's Voyager spacecraft, for instance, have been powered for 40 years by electricity from thermoelectric devices wrapped around heat-producing plutonium. In the future, similar devices might be used to help capture heat from your car's exhaust to power its air conditioner.

But that process can also be run in reverse. When an electrical current is applied to the device, one side becomes hot and the other cold, enabling it to serve as a cooler or refrigerator. This technology scaled up might one day replace the vapor-compression system in your fridge and keep your real-life soda frosty.

(Source: UCLA)

Sunstone Circuits Sees Roadmaps as Practical and Collaborative



Feature Interview by Nolan Johnson
I-CONNECT007

I spoke with Matt Stevenson, VP of sales and marketing and a Design007 columnist, about what roadmapping looks like for Sunstone Circuits, a PCB prototype fabricator whose best value might come a step behind the bleeding edge. Stevenson also describes how Sunstone works internally within its departments and externally with its customers to make roadmaps work best for them.

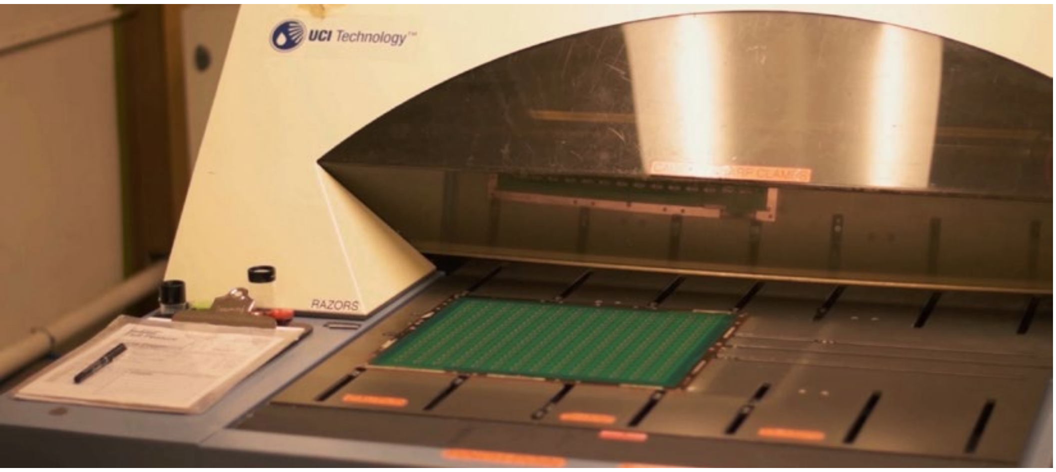
Nolan Johnson: We've been talking about roadmaps and how they help you do your long-range strategic planning. External roadmaps, like the IEEE Heterogeneous Integration Roadmap (HIR) or the roadmap from iNEMI, are being put together by associations to allow businesses in the sector to do their strategic planning. I want to start this conversation on the manufacturing floor, where you're planning for capabilities. You use roadmapping to plan for the new capabilities you're targeting. Walk me through the overall process you use at Sunstone Circuits.

Matt Stevenson: Our roadmaps are not necessarily driven by association roadmaps. We generally go to our customers; what they want defines our roadmap. We may be a little behind the pace of some of the association roadmaps, but we see what customers adopt and clamor for in terms of new capabilities and technologies. We get their feedback and their input before we physically add that on to our manufacturing or technology roadmap.

Johnson: As a fabricator, what your customers are asking for is your roadmap of reality.

Stevenson: Correct. If they decide not to adopt something that's on the IEEE roadmap, then we haven't lost any time. They've weeded out what they think is important for their business, and that flows down to us.

Johnson: What's the value of industry association roadmaps for Sunstone?



An LDI machine.

Stevenson: The association roadmaps are anecdotal for us. It's like, "This is the stuff that is possible," which is more pie in the sky than anything. This will be for the companies whose technology lives on the leading edge, but probably not the mainstream companies that typically are our type of customers. We're looking at more established companies that are prototyping for new designs, hobbyists, students, etc. They use more mainstream technology, and it's getting a little bit closer to some of the leading-edge stuff, but their bread and butter is within the main constructs of current technology.

And we don't have large business relationships with those leading-edge manufacturers that are doing some of that crazy new stuff. A few PCB manufacturers are known for being on that leading edge and make a living off that. But we focus more on what is mainstream technology today, what is becoming mainstream tomorrow, and how we can best utilize that to get customers to great quality products and fast.

Johnson: What's your manufacturing sweet spot?

Stevenson: At this point, we are pretty much industry agnostic. We have products that are attractive to every aspect of nearly all industries, but it's usually companies that have an established technology set that they like to use and design with. They'll innovate a little bit on this type of chip or passive, but it's not the company with the philosophy that says, "We're going to go to ultra-HDI this month and need you to conform to that."

We are very well-positioned in that area. We're known as a solid manufacturer for those types of technologies. We have been moving capabilities toward the HDI realm for several years. Strategically, we are not targeting the entire blind/buried via type of HDI products, but the smaller via, smaller holes, higher aspect ratio, and smaller finer lines and traces. Every purchase that we make for equipment gets us one step closer to being able to really offer these products as we did 10 years ago with the six-mil trace and space and the 13.5-mil drill very fast with very high yields. We offer five-mil trace and space with our limited review PCBExpress products. Four and four is becoming to us what five and five was two years ago. Ten-mil and eight-mil holes are becoming commonplace. Almost every design has those on there now, and we're appropriately able to do that within our sweet spot.

The challenges for us become when we're stretching aspect ratios now. Eight- and 10-mil drills, most of the time, not a big deal. Start putting that into a 0.125" panel or a 0.093" panel, and you're getting those double-digit aspect ratios. The challenges then shift to the chemical processes and away from the mechanical processes. It takes an entire manufacturing team working in harmony to have success when building these in 48 hours or less.

Johnson: Sunstone tends to work in a niche providing an affordable solution for prototypes and small lot sizes, which is a great value. On the technology adoption curve, from bleeding edge to early adopters, late adopters, and laggards, I hear you saying that the industry roadmap work really is valuable to those early adopter companies. You're one step back from the early adopters in the big part of the bell. As these techniques move out of the early-adopter phase and become more mainstream, it shows up on your roadmap. You're bringing the tried and true technology.

Stevenson: That's fair. Our manufacturing model is not necessarily engineering-driven for customer fulfillment; it's product fulfillment-driven and not about what we can do better, faster, cheaper. It is also customer-driven for us and depends on what people are willing to purchase and what we can do in a very quick amount of time.

Johnson: At the same time, you're working on things that also generate good products and high yields even in a high-mix environment, leaving that lower-yield, experimental, bleeding-edge stuff to other providers. I can see your point. Watching the association roadmap is not as valuable as it is to some of the other providers. Instead, tracking what's going on with some of the leading-edge fabricators might be a good source of forecasting for you.

Stevenson: Once a technique has dropped down to that first tier of adopter fabricators, then we can be pretty confident that it will be moving toward our part of the bell curve within a few years. Depending on what the thing looks like, we may start to research these processes to be better positioned when our customers start asking for them. The association's roadmap is a bit too early and not always a good predictor of what will actually be adopted for Sunstone to be watching them very closely.

Johnson: It makes sense that the customers tell you what they want. Since you're operating back from where the industry roadmaps are focused, how much G2 are you getting from other fabricators? Do you share that sort of information back and forth?

Sunstone Circuits' support team.

Stevenson: We have a number of PCB fabricators that we have pretty good relationships with. We'll send work back and forth, etc. Generally, we'll have monthly check-ins where we'll always ask those questions, "What's the state of your business? What are you working on next?" Sometimes, they're at liberty to discuss that with us. Other times, they say, "Talk to me again next month, and I'll have something for you."

For the most part, we have a pretty good open relationship where we're able to give a little bit of G2 before the press releases come out, even if it's just, "We're working toward this." If it's something that my customer's interested in and that my partner is working on, it's not as high a priority for me to bring that inhouse at Sunstone now when I know that I'm going to have a partner to develop that ahead of us and we can get there in due course, rather than, "I need it tomorrow."

Johnson: That gives you a chance to bridge the gap as it's moving into the mainstream.

Stevenson: Typically, the way that it's worked for us is we can implement it faster with a higher success rate if we wait once the beta testing is over within the fabricators.

Johnson: What's a recent example of using your roadmapping process that made things better for Sunstone?

Stevenson: We updated our imaging to laser direct imaging over the past handful of years. It was a high-dollar ticket item for us to buy, but even with that, it paid for itself relatively quickly in terms of quality, repeatability, and throughput, even more than we had anticipated. It allowed some of our immediate imaging staff to move to other areas where they could use that expertise to do other things, but their hands-on in the image department drastically decreased.

That is one that had been on our roadmap for quite a while. We started and stopped on that process several times until we said, "Technology is getting to a point, and cost structures are such that it makes really good sense to implement this," so we did. We paid for the piece of equipment in less than a year, and that's not a cheap piece of equipment.

Johnson: Was there a clear decision point somewhere?

Stevenson: All signs pointed toward this as somewhere we needed to go, but early on, they just couldn't support the high mix and panel throughput that we needed. Once those technology barriers were bridged, we picked up the project again. There wasn't one thing that said, "If we want to do this kind of work, we have to do it. If we want to keep the customer, we have to do it." It was just incrementally everything pointed in that direction. The ROI was there, we had the cash and the cash flow to do it, and it made good sense for us.

Johnson: You looked at all of the different vectors on all of the different business factors, and they all went through the same spot. Rather than trying to justify it for some other reason, which maybe wasn't a well-thought-out strategic decision, you held on to what they were doing and what worked well until it was clear that it was time to go to something else.

Stevenson: Exactly. One of our main charters is being profitable and making good products for customers. A lot of those things come down to, "Can it be profitable right out of the gate, and can we not miss a beat with on-time deliveries and quality." It may not need to be a proven technology, but it needs to be solid technology.

Johnson: Sunstone works to preserve your on-time and overall yield or lack of scrap. What are your on-time and scrap metrics right now?

Stevenson: Wildfires aside, we are still running an on-time delivery close to 99.5%, and that includes one-day and two-day turns. Our production yield at this point has been trending right around 98.5% yield. It's a really low scrap rate with few late deliveries.

Sunstone Circuits' office.

Johnson: That's the value-add for you. You're not on the expensive leading edge, but you're just enough forward that you can deliver high reliability, schedule clarity, and security for your customers. They're going to get their boards when they need them.

Stevenson: Our biggest value proposition is, "You're going to get what you need when you need it." That brings peace of mind.

Johnson: Do you have a second example you might want to share with regard to roadmapping?

Stevenson: Data security, cybersecurity, the NIST requirements, and the DFARS type of requirements have been floating out there for a while. Security for us and our customers, especially in the military and defense sectors, requires those certifications, as well as auditing to those types of statutes. A little over a year ago, we put some of those cybersecurity things on our roadmap. We are just finishing up the last two items on the NIST 800-171 statute as we speak. Especially with today's technology, it's very important for keeping our customers' data, files, and IP secure—all of our data and proprietary information from the outside world. The COVID-19 pandemic gave people more opportunities to do nefarious things. People were suddenly working from home or unemployed. They had more time for, "I can do some hacking. I can try and break through this firewall."

We noticed a pretty big upsurge in attempts at our systems with the global pandemic in March, April, and May. It was a good thing we were ahead of the curve on some of these cybersecurity things because it prevented anything from happening to us as it happened to others over the last year.

Johnson: You're roadmapping not just the technology on the manufacturing floor but also your overall portfolio of offerings and methods of doing business. Where do you see training and skill-building on the roadmap?

Stevenson: It's always a milestone within the items on the roadmap, but we really handle that type of training and cross-training more with our ISO continuous improvement and employee training activities within the ISO 9001 realm. It has a pretty big section on employee training and documentation of the training, etc. Usually, at least in terms of manufacturing skills training, we don't have anything on our roadmaps beyond individual department heads. We offer a good amount of opportunities for learning, outside of the manufacturing specifics, to our employees throughout the year on a voluntary basis.

In terms of employee development and continued knowledge base within our management team and our leadership teams, we do an HR roadmap with quarterly and annual items that we want. These could include leadership experience, project management, and other skills that will fit within our leadership team, ratcheting up to the next level. It's more of an HR-driven function and an individual manager's one-off basis for each of their team members. It has been a successful process over the years. We have had many of our employees take on increasing levels of responsibility as a result.

Johnson: I'm picking up that you do roadmaps on a departmental level.

Stevenson: Not as formally as we've done at the senior level, but each of our department supervisors has a piece of the overall roadmap that flows up to the corporate roadmap. Within our ISO quality management system, we call them dashboards or turtles. There are separate dashboards that feed into the main, overarching dashboard, which then becomes a line item on a roadmap at some point. Using the ISO methodologies, we're actually able to document that at the lower level and have it flow up nicely rather than, "Here's what I want everybody in my department to do. Here's the roadmap. Everybody pick a part and do it." This way, there are separate pieces, it makes sense for the individual departments, and it flows.

Johnson: You have a bottom-up roadmap process, which makes a lot of sense. Bringing in external factors is something of a top-down process. Who manages the two flows?

Stevenson: Part of it is really managed by the ISO process. There's a constant management review of the risks and the potential items out there, which will provide those prioritizations within the departmental roadmaps to flow up again. If a risk is identified on a strategic roadmap, it's able to be presented and addressed during those ISO reviews to get everybody back rowing in the same direction. Our process is to use monthly or quarterly reviews of those types of things to update it companywide.

Johnson: This conversation has got some good insight. Roadmapping isn't just a big picture process.

Stevenson: Exactly.

Johnson: Matt, it's always a pleasure speaking with you.

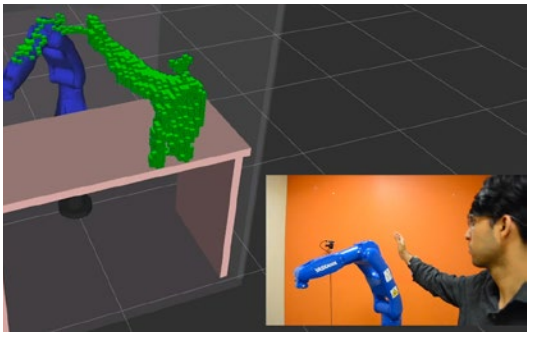
Stevenson: Thanks, Nolan. **PCB007**

Helping Robots Avoid Collisions

Most new roboticists want to program their robots to solve interesting, complex tasks, but it turns out that just moving them through space without colliding with objects is more difficult than it sounds.

Fortunately, George Konidaris is hopeful that future roboticists will have a more exciting start in the field. That's because roughly four years ago, he co-founded Realtime Robotics, a startup that's solving the "motion planning problem" for robots.

The company has invented a solution that gives robots the ability to quickly adjust their path to avoid objects as they move to a target. The Realtime controller is a box that can be connected to a variety of robots and deployed in dynamic environments.



"Our box simply runs the robot according to the customer's program," explains Konidaris, who currently serves as Realtime's chief roboticist. "It takes care of the movement, the speed of the robot, detecting obstacles, collision detection. All [our customers] need to say is, 'I want this robot to move here.'"

Realtime's key enabling technology is a unique circuit design that, when combined with proprietary software, has the effect of a plug-in motor cortex for robots. In addition to helping to fulfill the expectations of starry-eyed roboticists, the technology also represents a fundamental advance toward robots that can work effectively in changing environments.

(Source: MIT News)

Roadmap? First, Find the Road!

Testing Todd
Feature Column by Todd Kolmodin, GARDIEN SERVICES USA

This last month has been a challenge for yours truly. The hits keep coming in 2020. Living in Oregon is normally very beautiful. Sure, we have more than our fair share of rain, but it has been drier this year. Unfortunately, the Pacific Northwest September has been a nightmare. One would think COVID-19 would have been enough, but no, we have had the worst family of wildfires in our state's history.

I originally thought of discussing roadmaps and how they pertain to our industry and analyzing trends. However, it's difficult to work with the roadmap when you cannot find the road. For a time, our visibility was zero to one-fourth of a mile. For over a week, our area had the worst air quality index (AQI) in the world. Anything at 50 or below is considered normal. Where I live, we exceeded 500, and other places in the state reached values over 600. Mind you that the "hazardous" level tops out on the scale at 500.

For a brief time, the air quality and visibility were so bad in Portland that Alaska Airlines ceased all operations at the Portland Airport due to hazardous conditions. Local service providers modified delivery and pick up schedules due to the conditions and allowed employees in affected areas to take care of their homes and families.

For context, we have a yearly fire season, and there are typically one or two fires that consume forest timber. It happens. However, this year, it started by a once-in-a-millennium windstorm from the east. High winds against trees full of foliage started a chain of events that set Oregon ablaze. Places in the Cascade Mountains that I grew up visiting no longer exist as I knew them. Towns have been incinerated. There is nothing left in some places. In the county where I live, the Chehalem/Bald Peak fire was a mere six miles west of us. We were lucky. The winds were blowing away from us. It has since been contained. The picture of the Chehalem fire was taken by yours truly at midday, but it felt like it was dusk (Figure 1).

Figure 1: Chehalem fire at noon.

Figure 2: Molalla fire at 11:00 a.m.

The picture in Molalla (Riverside fire) was during the evacuation (Figure 2). The town had been evacuated, and this was the view at 11:00 a.m. There was no sun showing—only the red sky. The list goes on. Another fire to our northwest was the Powerline fire, which was southwest of Forest Grove, Oregon. This was close to a major recreational area known as Hagg Lake. The area was closed, and the nearby town of Cherry Grove was evacuated. This fire has also been contained.

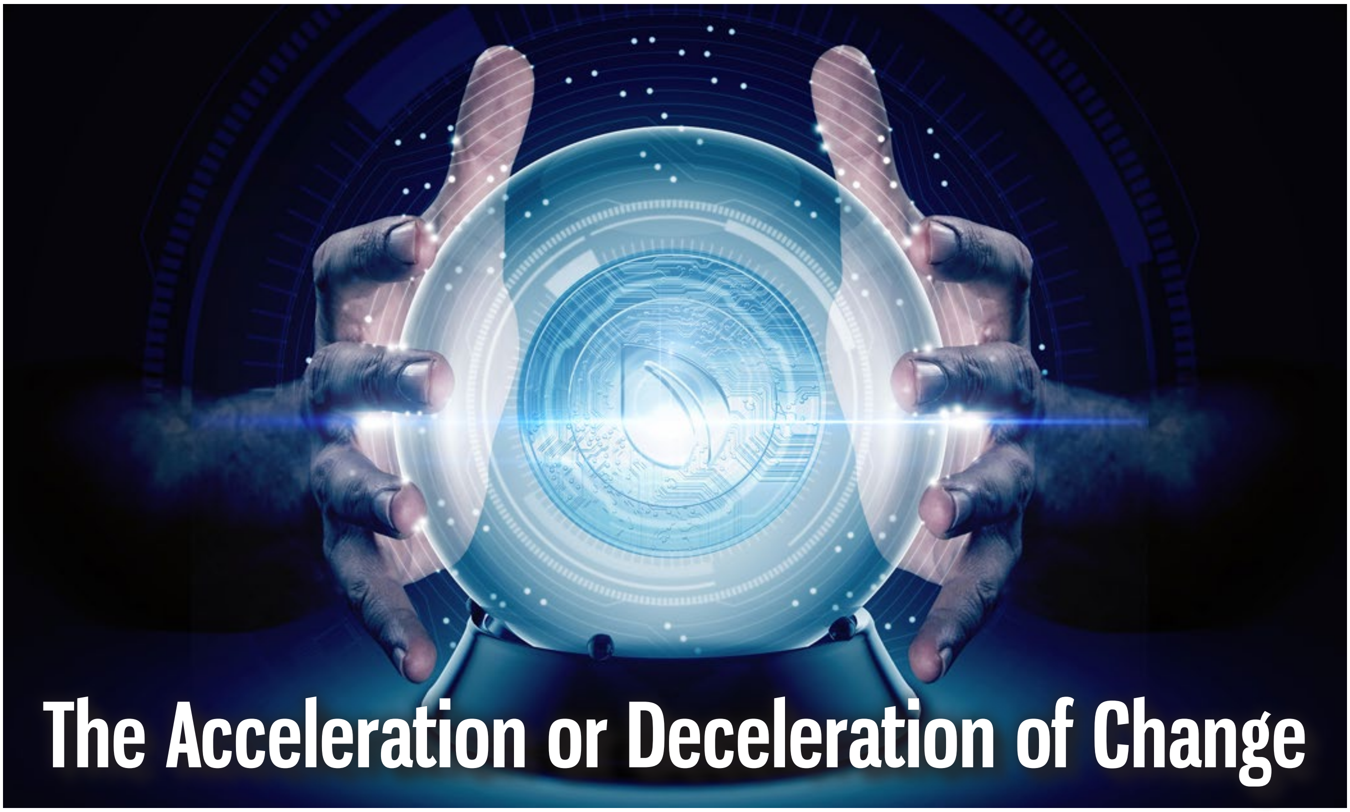
Figure 3: Salem, Oregon, on September 8 at 2:00 p.m.

However, at this writing, the two major fires (Riverside and Beachie Creek) remain very active and continue to ravage. These two fires have consumed over 1 million acres and countless structures. Towns nestled on two different scenic highways into the Cascade Mountains are gone. The smoke from the West Coast fires has been felt all across the U.S. and even detected in Europe. If it were not for the heroic efforts of all the first responders, firefighters, and townspeople coming together, the devastation would be much worse. Town shopping center lots have become evacuee camps. Fairgrounds have been opened for livestock evacuation. Volunteer food courts have sprung up. Farmers have opened their gates for RVs, trailers, and tents. No one asked for anything; it was just neighbors helping neighbors, which was beautiful to see.

It has been only a few days since the winds have changed. We have seen some rain, and the local air quality has dropped again to roughly normal levels. In 2020, "normal" has become a word that is a moving target. We still wear our masks, ash and soot blanket the roadways, and vehicles and smoke can still be seen where the fires still burn. It will take time—and the fall rains and snow—to fully extinguish these major fires. Our heroes can only control and stop their spread.

It has been a challenge. My heart goes out to all those who have lost their livestock, homes, and the ultimate loss of family. Again, from Oregon and the West Coast, thank you to all the first responders, firefighters, and support personnel who have come from all over the U.S. and abroad to battle these catastrophic fires. **PCB007**

Todd Kolmodin is VP of quality for Gardien Services USA and an expert in electrical test and reliability issues. To read past columns or contact Kolmodin, click here.



The Acceleration or Deceleration of Change

Feature by Dan Feinberg
FINE-LINE ASSOCIATES

Things have changed a lot in the last year, especially in the realm of technology.

Just a year ago, 5G networks were on a smooth path to unquestioned rapid growth dominance. Today, while there has been much progress, and while there are some 5G capable devices available, it is far from universal. In some areas, such as near schools and residential areas, people were putting up roadblocks to 5G towers. Overall, there has been much progress, but the pace seems slower than was expected just a year ago. Some limitations are being identified, and there is already talk of 6G becoming available well before the end of the decade.

Extended reality (XR)—or one of the various extended reality segments, such as virtual reality (VR), augmented reality (AR), mixed reality (MR), etc.—was making progress at light speed. It still is progressing, but much of the hardware that was about to become available during 2020 has been delayed. Areas where XR has true value—such as military, medical, and tech service—are progressing rapidly and with the 2020 shutdown areas, including XR-enabled gaming partially by next-generation graphic processing units (GPUs), is quickly accelerating. It has been reported that XR digital game spending reached over $10B in April 2020 and has continued to grow.

We all know that video conferencing has taken off. Is there anyone who has not been on a Zoom or Microsoft Teams call in the last week? Many of us are on two or more a day. So far, the use of XR in teleconferencing is mini-


Uniquely suited solutions for an increasingly demanding world.

mal, but I would expect that area to accelerate greatly in the next 18 months.

Last winter, some of us predicted that trade shows might have to be canceled, with the key indicator being what would happen with 2021 CES. This year's mega-event in Vegas will not take place, at least not in its usual way, but there will be a virtual show, demonstrations, and presentations. Other events have also followed that path. I predict that it will not slow down the introduction of new devices; in some cases, it will accelerate it. For example, the leading supplier of graphic processing technology, NVIDIA, just introduced their next generation of GPUs (more on that later).

Usually, one could expect that CES would be the perfect place to introduce this highly anticipated generation of devices, but with this show being different than the type we are used to, why not introduce the RTX 3000 series sooner? This introduction has been so successful that I would expect other similar accelerated introductions. Without major in-person trade shows, how will we focus on, stay up to date on, and easily compare all the new technology and devices?

With this preview, let's consider the specifics of some areas that demonstrate the acceleration or deceleration of change.

Graphics Processing

As mentioned, and as we have recently covered, NVIDIA introduced their next-generation GPU—the truly beastly RTX 3000 series. These devices are utterly amazing with multiple very high-definition monitor capabilities, advanced ray tracing, and exceptional FPS. Although it's expensive, the overall value as measured by capability vs. price vs. the last generation is quite good. One might ask why NVIDIA has kept the price reasonable (when compared to the last generation); perhaps it is because AMD also made progress and may announce new devices soon. For more details, you might wish to look at our NVIDIA product announcement coverage.

Apparently, the first shipments of these units have all sold out. Recently, I was at Micro Center for a totally different reason on the day when they were expecting to receive their first shipment of RTX3000 GPUs, and the line was literally around the block. On the negative side, there have now been some reports of some level of instability. NVIDIA just released a new driver to improve stability, but the issue may be hardware—perhaps it's a capacitor issue. Still, it's definitely accelerating.

Autonomous Transportation and Driving

An area where there was a tremendous predicted acceleration of change, and then an unexpected deceleration about a year and a half ago, was in autonomous transportation. This is an area that now seems to be getting past its pause. It could be the advances in AI and the abilities of the upcoming 5G network, especially in the area of rapid data transfer. It feels like we are about to step on the gas (or the potentiometer acceleration pedal) once again. There has been modest acceleration, but it's about to increase.

Blockchain, Bitcoin, and Other Types of Cryptocurrency

First of all, what is blockchain? According to one online definition, "A blockchain is a digitized, decentralized, public ledger of cryptocurrency transactions. Constantly growing as 'completed' blocks, the most recent transactions are recorded and added to it in chronological order. It allows market participants to keep track of digital currency transactions without central recordkeeping."

Basically, a blockchain is made up of blocks that include time-stamped encrypted transactions that are locked to all except the owner who holds a private key. Once a transaction has been entered in the ledger, it cannot be changed unless a new transaction is added that reverses or changes that specific transaction.

It is looking like blockchain—not just one of the currencies based on blockchain, such as Bitcoin, but blockchain itself—may very well change how the world does business. Using blockchain has become a priority for many companies' senior executives. Will the rate of use accelerate? That is a good question. I feel that the upcoming election and the economic results thereafter will catalyze its use and possibly accelerate its acceptance in both business and society. Please remember that we are discussing blockchain and not a single specific currency based on it.

Online Meetings, Discussions, Webinars, and Presentations

Early in 2000, I wrote a commentary regarding the then-upcoming trend to working and communicating online. As predicted, the scheduling (or overscheduling) of online meetings and events has become part of the new normal. Even when this pandemic is just a bad memory, I expect that when an event is announced, those interested or involved with the event will now have three choices to make: whether to attend, which ones are the traditional options, and which one is the new additional choice—which is to attend virtually.

The rate of online events and meetings has accelerated, which has mostly been caused by the COVID-19 pandemic. I cannot conceive of any major trade show or event not having its keynotes and presentations online, as well as the ability to visit booths and talk with exhibitors via the web. That is a good thing, especially for the real events where you can also choose to attend.

One problem is that there are so many online events now being put forth that have been created to take advantage of the online opportunity trend. Some of these people are now signing up, knowing that they can decide to attend later, and many do not. It's an accelerating trend, especially for the high-quality events, but for the rest, expect it to level off within the next year and for attendance to decline for those that are partly infomercials.

3D Printing and Manufacturing of Circuits and Devices

3D additive manufacturing of electronic components and devices is something that has been on an up-and-down trajectory for the last decade. The first rise was the feeling that this would allow for a mini-factory in every home, but due to the limited materials that could be printed at that time, this soon fizzled out. Today, however, with the ability of the new mixed-material printers, the return of 3D printers for many areas of manufacturing,

from parts to full devices printed on a wide variety of substrates, this is no longer the case. It seems almost certain that additive manufacturing is here to stay.

In addition, there are many signs that point to increased investments in additive manufacturing recently due to the increased capabilities, the expanded applications, and the need for less wasted space in electronic devices due to the desire for additional capabilities. Areas where you can expect to see increased use of 3D additive fab are aerospace (Airbus and Boeing have recently chosen to implement it), healthcare, dental VR devices, and others that have recently begun use of this process.

In general, there has been increased acceleration but be prepared for a few occasional taps on the brakes. This is a topic that we have followed closely over the last few years, and we intend to continue to watch and report on it.

Higher-End Monitors

I do not believe we have seen as much improvement in graphics screens, either TV or computer monitors, since the advent of LED screens and the vertical deceleration and death of the vacuum picture tube in the '80s. Everything about a video screen has improved, including the size, as well as huge advances in resolution with many now over 4K (with the new GPU technology supporting 8K), higher frequency, lighter weight, and HDR—you name it.

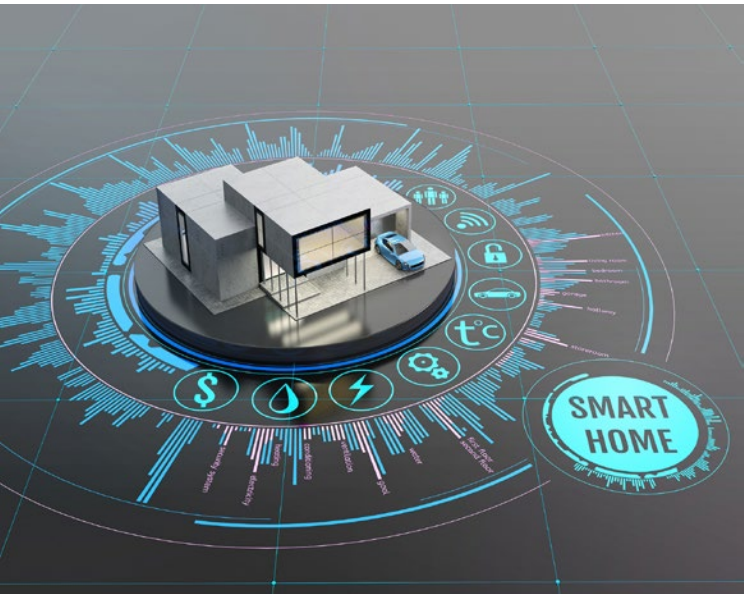
If you have a TV that is a few years old, it is out of date. If you have a computer monitor (you only have one connected to your comput-

er?), it is out of date. Screens for smartphones and tablets are now amazingly clear and flexible, and there is more to come. Also, expect to see prices continue to decline. We are in the middle of a significant acceleration not only in capability but also in quantity, as many of the lower capability devices are now being replaced. I expect to see this acceleration continue for a while.

New and Improved Smart Home Devices

Smart home devices—or as some call them, "Big Brother is watching"—"Alexa" and "Hey Google" are some of the most commonly used words spoken in many homes today. Yes, there are others, but these two are by far the most widely used. As for devices that connect to them, there are now many other companies making accessories. For example, you do not have to use Amazon's low-to-moderate quality sounding speakers to listen to the song you just asked Alexa to play. Now, you can get high-quality smart speakers from companies like Bose that are specifically designed to work with your Amazon or Google ecosystem.

Should you install a smart home system? That is up to you. There are many nice features, but there is also the issue of privacy. How many times have you mentioned in private to someone that you are thinking of buying or considering a purchase and/or project, only to receive an ad on that very thing? That is a topic for another discussion, but the point is that the use of smart home systems—ranging from just turning on the lights all the way



to controlling everything else—is increasing. The number of things that can be done with the system and the quality of the result, as well as the numerous choices available to you, are accelerating greatly.

New Smartphones Every Two Years

For the last decade, everyone has had to carry a smartphone. For much of that time, the phone you had was a measurement of your self-esteem, so many people had to get a new phone at least every few years. I believe that is changing. So many of the added features of the latest and greatest are no longer must-haves or provide added value. Thus, many of the phones look alike and perform in a similar manner.

They also seem to be more durable and last longer. Many of the teens who had to get a new phone every few years now have to buy their own. I predict that the “get a new phone every two years” trend is decelerating, but the demand for 5G phones may delay that deceleration, and the interest in dual-screen phones may accelerate this segment for a while.

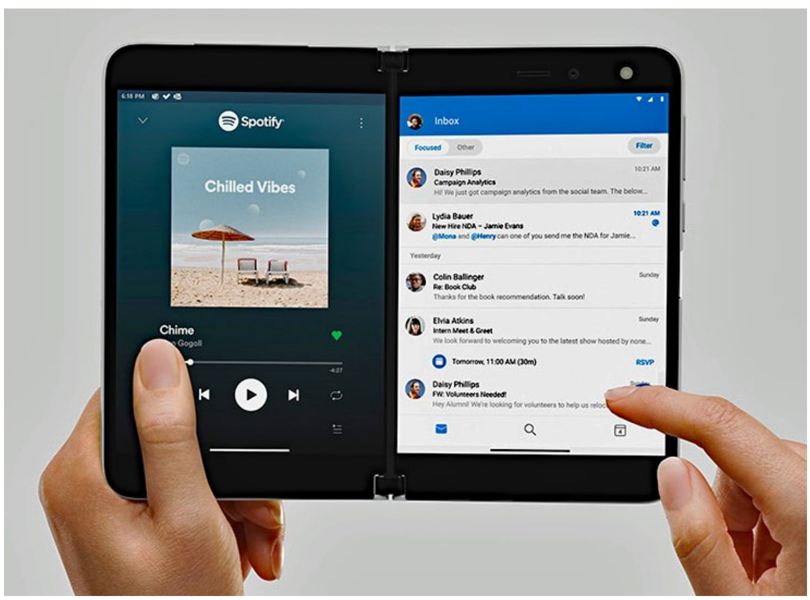
XR and More

VR use has been an up and down trend for the last few years, but now XR is one of the key areas to watch. The use of the XR description started at the AWE show a few years ago. XR is now used to describe the overall usage of VR, MR, and AR. XR is a technology that made significant strides in the last two years. XR use has become easier, and its incorporation in many industry segments has rapidly increased in the last two years.

The XR industry was reported by MarketWatch [1] to reach “USD 393 billion globally by 2025 with a CAGR of 69.4% during the forecast period. It was valued at USD 27 billion in 2018. Based on type, the XR market is categorized into mobile XR and PC-tethered XR. The former is expected to display a stellar growth rate during the forecast period owing to the procurement of portable devices. On the other hand, the PC-tethered XR segment is estimated to dominate the market due to the use of cloud services.”

Recent advances and product announcements show a significant reduction in the size, weight, and comfort of XR wearables, with some of the very capable ones becoming wireless, making them more user-friendly. Capability is improving, and prices are dropping, which is a typical indication of significant growth.

The areas that will see a major effect of the use of XR include interactive learning, employee and customer training, tech service, and retail sales—such as letting you see what your living room will look like when you in-



sert the new furniture you are looking at; exploring your backyard with a possible new pool installed; or considering focused education, hands-on virtual classroom training, partner company, or customer collaborations (let us show you our research labs or manufacturing lines through XR), as well as entertainment, movies, gaming, travel or potential travel tours, virtual attendance at concerts, sporting events, etc.

The combination of all the above and more will be even more real with the advent of the lightning-fast data transmission made possible with 5G. Did XR accelerate? Bet on it big time!

Medical and Military

These are two areas that are subsets of the previous topic, but all of these are related in one way or another. These two will continue to grow with or without significant advances in technology, but the change we have discussed so far—especially XR enhanced by 5G—will play a big role making military and medical missions far more effective and, for some, even possible, and add to that the improvements in flexible electronic manufacturing.

Imagine being able to perform robotic surgery from hundreds or even thousands of miles away. Imagine the world's top surgeon located in Atlanta being able to perform full robotic surgery using VR on a patient in Delaware, or being able to do the same on a patient in Tokyo. What if you could have your own eyes as part of a missile launched at a critical target and steer it to the exact location, right to the inch, or you could flight train with the most amazingly realistic virtual surroundings?

These are just general examples, but you get the idea. With accelerated growth in XR, the spread of 5G, and even when you include 3D additive to reduce the size and improve the reliability, this is another area where you can bet on accelerated growth.

Battery Technology

With so many new improvements in portable devices, including next-generation phones—such as the upcoming super-thin dual-screen devices—and electric-powered vehicles, a slow but growing trend in the use of electric rather than fossil fuels. There is a need for smaller, longer-lasting, faster-charging batteries. I believe that the growth in this segment is obvious, but currently, it is hard to predict the rate of change in the short term. Eventually, yes, but for the next year or two, we will have to wait and see.

Conclusion

The topics where I have projected that the rate of change is accelerating are the topics I will focus on in future articles over the next few years. Feel free to look at my opinions again in a few years and tell me if and where I missed the boat. **PCB007**

Reference

1. Market Watch, "Extended Reality (XR) Market is Rising Due to its Remote Presentation During COVID-19 Lockdown | XR Market Size, Share, Trends, Opportunities, and Challenges," September 9, 2020.

Electronics Industry News and Market Highlights

Mitsubishi Chemical Develops Electrolyte for Tesla ▶

A Mitsubishi Chemical technical expert revealed that the important innovations of Tesla's new battery are the positive and negative electrodes and the new electrolyte.

NVIDIA's Three Next-Generation GPUs Excite Consumers ▶

Finally, the product release that many had been waiting for. NVIDIA recently announced its next-generation RTX 3000 Series GPUs, and the stated capabilities are amazing. Dan Feinberg has all of the details.

Aeva and ZF Bring First FMCW LiDAR to Automotive Production ▶

Aeva, a leader in next-generation sensing and perception systems, and ZF, a top global automotive Tier-1 supplier, are partnering to bring the world's first Frequency Modulated Continuous Wave LiDAR to the automotive market.

GLOBALFOUNDRIES, Mentor Launch Semiconductor Verification Solution ▶

GLOBALFOUNDRIES, a leading specialty foundry, announced at its annual Global Technology Conference a significantly enhanced design for manufacturability kit embedded with advanced machine learning capabilities.

UVD Robots Makes a Quantum Leap for Disinfection Robots ▶

The COVID-19 pandemic has permanently increased cleanliness and disinfection requirements on a global scale. In more than 60 countries around the world, UVD Robots' distributors are experiencing high demand from hospitals, airports, hotels, shopping malls, food companies, cleaning industries, cruise ships, pharmaceutical companies, office complexes, and many others seeking to procure solutions to ensure infection-free environments.

Qualcomm Snapdragon XR2 Platform Commercially Debuts in Oculus Quest 2 ▶

Qualcomm Technologies Inc., a subsidiary of Qualcomm Incorporated, is powering better-than-ever virtual reality gameplay and experiences with the launch of Oculus Quest 2, the first-to-launch VR device powered by the QualcommÒ Snapdragon™ XR2 Platform.

DigiLens Brings Ultra-Compact CrystalClear AR HUD to Any Auto Dashboard ▶

DigiLens Inc., an innovator in holographic waveguide display technology for extended reality, announced the availability of its CrystalClear™ Augmented Reality Heads-up Display (HUD), boasting the largest field-of-view (FOV) HUD up to 15° x 5° and packaged into approximately 5 liters of volume.

Deloitte and Wichita State University Join Forces to Launch New Smart Factory ▶

Deloitte and Wichita State University announced the launch of The Smart Factory @ Wichita, a groundbreaking and immersive experiential learning environment that will accelerate the future of manufacturing as innovation and new technologies continue to reshape operations and the modern enterprise.

Keysight Technologies Bolsters Technical Support Services ▶

Keysight Technologies Inc. announced it expanded the company's KeysightCare program to provide a growing customer base with fast, reliable access to priority technical support.

An Update From Taiyo America's Don Monn

Interview by Pete Starkey
I-CONNECT007

Taiyo America's Don Monn explains new product developments based on understanding challenges that OEMs are looking for suppliers to overcome on their behalf and discusses the attributes of a crack-resistant white solder mask for automotive LED applications.

Pete Starkey: I'm delighted to have the opportunity to catch up with Don Monn, sales manager with Taiyo America. It's wonderful to get the chance to talk to you again. It has been ages since I saw you last. I remember it was at the EIPC conference in Rotterdam.

Don Monn: It has been a while, but this gives us a great opportunity to talk about some things that are going on. I am looking forward to the chance to get to another conference so we can all sit down and have a Pepsi.

Starkey: I look forward to it, too. What have your development people been working on in the meantime? What's new at Taiyo America?

Monn: Thanks for asking. Over the last several months, we have had weekly, monthly, and quarterly meetings to talk about what's needed in the industry. Typically, when you have a big R&D group, you need to look at the things that aren't currently available. In other words, we would go to customers and OEMs and ask, "What do you need that you don't currently have? What's moving forward?" In a nutshell, we're working on some thermal management materials for the surface of circuit boards, as well as the holes.

We're working on low Dk and low Df solder masks to help with the speed of high-speed circuitry. We're working on a new high-temperature solder mask for the automotive industry that will reach heat numbers that we haven't seen to date because, as you know, in the automotive industry, they're starting to put packages in solution. And when I say a solution, I mean transmission fluid and oil, which is very hot for very long periods of time. Then, there's always the inkjet solder mask that we've been talking about for years; that's a growing industry right now, as we all knew it would be. And last but not least, we

Don Monn

have introduced a photoimageable coverlay to the industry with great acceptance.

Solder masks and consumables are growing, so that's a market we were counting on, and it's coming to fruition. One of my favorite subjects is LED solder mask, or white solder masks, for different industries because of reflectivity and color stability. The automotive industry uses a lot of white solder masks that a lot of people are not even aware of.

Starkey: Is the white mask that you just mentioned a crack-resistant version?

Monn: You nailed it. We were very fortunate when we started looking at this. We went to some OEMs and said, "What do you need that you don't have?" In the automotive industry, crack resistance is very important. But what we weren't aware of, and they educated us on, is not only do they need white solder masks that have crack resistance, but they still require color stability and some high-temperature applications. Simply making it crack-resistant and losing other characteristics wouldn't be acceptable. We had to keep those other good capabilities and make it crack-resistant as well.

Starkey: I can visualize the sort of harsh service conditions that such a product would have to endure. Tell us a little more about what drove the development and what specific problems it overcomes.

Monn: When you talk about crack resistance, there are a lot of different ways to view cracks. Typically, in circuit board manufacturing, when we think about a crack, we think about a surface crack based on temperature, reflow temperatures, and contaminants on the surface, but there are many kinds of cracks. When you're talking about LED boards, a lot of these boards are single-sided with copper or aluminum backs. They don't typically always get routed; some of them get punched.

The punching process, which is especially dependent on the size of the parts, can cause a tremendous strain on the board, the panel, and the solder mask. That was something we never considered initially, but once we learned more about what our customers were doing and how they were doing it, the little light bulb went off in our head, and it was another problem to solve.

Starkey: You're looking at the mechanical stresses involved in fabrication, as well as the stresses induced by a CTE mismatch.

Monn: Right. You phrased it a lot better than I did.

Starkey: As I said before, I know the automotive market is getting more and more demanding, and the service conditions of these materials become more and more and more severe. We've talked about overcoming the mechanical stresses and the thermal expansion mismatches between the coating and the substrate. Also, because it's in an LED application, it's going to get hot, so it has to have high-temperature resistance, as well as to get alternately hot and cold, depending on whether the system is switched on or not. It's also white and has to stay that way. There's not a big advantage if it yellows upon long-term exposure to intense white and UV light.

Monn: You hit on all the major factors. You absolutely spelled it out, and that's why it's really great to have people working in our lab who are a lot smarter than me who can figure out how to create something that will stay white, not crack or break down, and stay constant through the CTE mismatches, as you mentioned.

Starkey: But these people in the lab rely on people like you as the interface between themselves and the customer. You need to talk to the customer, find out what the customer really wants, and to back to the development people and say, "These are our requirements. These are the challenges we want you to address."

Monn: That's where Taiyo is very fortunate to have opportunities to go to the EIPC conference or IPC APEX EXPO and to do interviews with I-Connect007 because that gets the word out. OEMs listen to this and realize, "If I don't talk to my suppliers and tell them what I need, how are the manufacturers going to know what to design and make?"

Starkey: You can't do your product development on spec. You have to do your product development focused on what the market's demanding or what challenges the market is looking for you to overcome on their behalf.

Monn: Exactly, and that's where, instead of me running around the country or around the world talking to one OEM at a time, the conference gives me an opportunity to have access to people and see them.

Starkey: At the conferences, you've become quite famous as a presenter. And I've certainly had a lot of experience of the European conferences where you're presenting to an audience of perhaps 120 top people from the industry who are hanging on every word you say.

Monn: The EIPC conference gives me a great format to speak, and I truly appreciate it. But what I really like is, as you mentioned, there are some big players and important people who understand the value. One of the things we've always preached is doing things right the first time and doing things with the best materials possible because you can't sustain business doing things a second and third time. The people at the EIPC conferences grasp and understand that aspect maybe more than some others.

Starkey: I've always been very impressed by the two sides. On the one side is the quality of the presenters, but on the other side, the caliber of the audience. It's a well-balanced setup.

Monn: Again, especially as boards get more and more complex, and their material bills get more and more expensive, yields and doing things right the first time become even more important. That message that we've been trying to deliver becomes more relevant every day.

...as boards get more and more complex, and their material bills get more and more expensive, yields and doing things right the first time become even more important.

Starkey: Going back to the crack-resistant white solder mask, how is it printed and cured?

Monn: The nice thing about it is that it's still photoimageable, which is a trick in itself. As far as application, it was very important that we had multiple application technologies, so this product can be screen-printed or sprayed. It works very well, either way. And then it's a simple tack dry, expose, develop, and cure just like a standard photoimageable solder mask.

Starkey: Does the PCB fabricator need any additional equipment to process this material?

Monn: No, sir. It's a drop-in. The one thing about Taiyo America is our product's base chemistry, and our thought patterns have not altered, so if you look at our product line with photoimageable solder mask, the processability, setpoints, and robustness—whether it's white, green, HFX, or solder mask for the Cadillac and Lexus versus entry-level products—the processing is extremely similar from one product to the next.

Starkey: It sounds like a very positive response to a significant market requirement. Thanks for the update on that.

Monn: And with COVID-19 and all of us not traveling nearly as much, it's giving us more time to work on some of these projects, get them right, and get the testing done before we introduce them to the marketplace.

Starkey: That was actually going to be my next question. It's the "elephant in the room" question. This coronavirus pandemic continues to affect us all. You've given us a sort of flavor of how Taiyo America is dealing with it. Do you have any further comments? You did say that you were not able to travel as much as you did.

Monn: That's a great question. Our sales managers and our service group have always been remote. We don't work at the main office. We live where our customer base is and the territory we manage. But when you go to the office, we found that many of the functions done at the facility could be done remotely. Our customer service group now works remotely. They set up offices in their homes and have not missed a beat. They're doing everything they need to do from home, so we've eliminated a lot of headcount in the office.

For the people that need to be in the office, all of a sudden, instead of having a small area, it allowed us to double and triple the space between desks, so distancing is much easier in the office. We're doing everything as best we can and staying as healthy as we can. Like everybody, face masks are required in the building. If anyone has to go somewhere where they quarantine for 14 days, we follow the guidelines the best that we can.

Starkey: It's clear that you're taking a very sensible approach to it. In the circumstances, you're certainly doing the best that it is possible to do. Thank you, Don. As ever, it's a great pleasure to talk with you. I hope it's not too long before we get the chance to meet face to face again.

Monn: As soon as that works out, we'll get together and talk about it.

Starkey: That sounds good to me. Thank you. **PCB007**

Pete Starkey is technical editor for I-Connect007. Based in the UK, Starkey has more than 40 years experience in PCB manufacturing technology, with a background in process development and technical service. To contact Starkey, click here.

The Critical Role of Pretreatment for Plating

The Plating Forum
by George Milad, UYEMURA

Electrodeposition can be traced back to the 1800s. Plating decorative gold on a silver surface using a voltaic cell was exciting at that time. Along with electrodeposition, surface prep or pretreatment was an integral part of the process.

Pretreatment is usually customized to the incoming substrate and the plated metal. It is designed to clean organic and inorganic contaminants from the surface. In addition, pretreatment may alter the surface morphology of the substrate for adhesion enhancement. It is a critical step and must be completed before plating to achieve the desired adhesion and to enhance the quality of the deposited metal.

Pretreatment utilizes cleaners and etching steps. In some applications, pretreatment is used to modify the substrate to allow plating to initiate. Chemistries used in pretreatment are not compatible with the plating process and must be thoroughly rinsed before plating. Rinsing for electronic manufacturing is usually done in a two- or three-step cascading flowing rinse.

The following is a description of the desired pretreatment for the following applications:

1. General metal finishing
2. Plating for electronics manufacturing:
   - Electroless copper plating
   - Acid copper plating
   - Surface finish

1. General Metal Finishing

Metal surfaces must be pretreated before plating. The objective is to remove contaminants from the surface. Contaminants may be organic (oils, grease, fingerprints) or inorganic (scale, stains, and oxides).

The process is referred to as "pickling" and usually involves the use of strong acids like sulfuric or hydrochloric. The pickling liquor may contain other acids as well as specific additives like wetting agents and corrosion inhibitors. The pickling chemistry must be compatible with the specific basis metal and effective at removing the associated impurities and or contaminants.

The choice of pickling liquor chemistry (type, concentration, and bath life) and the conditions under which it is used—like temperature, dwell time, and part agitation—must be well-defined and adhered to for efficient surface preparation. The pickling solution must be thoroughly rinsed before the introduction into the plating electrolyte.

2. Plating for Electronics Manufacturing

Electroless Copper

The electroless copper process is used in electronic manufacturing to metalize the dielectric in the drilled holes. The deposition is autocatalytic or electroless and does not require rectification.

Pretreatment is very critical in this process as it serves multiple functions. It starts with a cleaner/conditioner that cleans the surface and modifies the fiberglass in the FR-4 dielectric by altering its negative charge to neutrality so that it will adsorb the catalyst that initiates the copper deposition.

The cleaner is followed by a micro-etch that refreshes the copper on the surface, as well as in the inner layer interconnects in the hole. It ensures good adhesion on the copper surface and the interconnect integrity with no separation between the plated copper and the inner layer. This step is followed by the catalyst and its rinse.

If the pretreatment is compromised, voiding in the deposit may occur as well as a separation in the interconnect at the inner layers. The electroless copper process is preceded by "desmear." Desmear is considered a process in its own right and not a pretreatment.

Acid Copper Electroplate

The copper electroplate process is the backbone of printed circuit manufacturing. It forms the circuitry that carries the current throughout the board. Parts coming to the electroplating line have already been through the electroless copper process. Pretreatment here involves a cleaning step, micro-etch, and acid predip.

The "cleaner" serves a series of functions: the detergent component removes soils and organic residues (fingerprints), the acidic component removes oxidation, and the surfactant present wets the surface. A properly wetted surface will help dislodge any entrapped air in the narrower vias. Entrapped air leads to voiding and discontinuity. Vibrating the parts in the cleaner bath is recommended for high aspect ratio holes and blind vias. Vendor recommendations of make-up, bath life, operating temperature, and dwell time, should be followed. Good rinsing should follow the "cleaner."

The micro-etch step is mild and removes 5–10 micro-inches of copper, exposing a fresh surface for plating. Excessive etching is not recommended, as it may dissolve the electroless metallization resulting in voiding.

The last step in pretreatment is an acid predip. This serves two functions. First, it ensures no oxidation on the copper surface; second, it acidifies the surface to match the acidity of the copper electrolyte.

Surface Finish

For the purpose of this column, I chose to break down surface finish to:

1. Single-layer finishes: Hot air solder leveling (HASL), organic solderability preservative (OSP), immersion silver, and immersion tin
2. Multilayer finishes: ENIG, ENEPIG, and EPIG/EPAG

Single-Layer Finishes

The pretreatment for this class of finishes is based on creating a clean surface that is contaminant/oxide free. In addition, for immersion silver and immersion tin, the surface morphology of the copper surface is also addressed.

For HASL to produce a contiguous intermetallic (IMC) with no dewetting, the copper

surface must be clean and pristine. For pretreatment, the parts go through a cleaner and a micro-etch in a horizontal conveyorized manner; this is followed by a flux dip before introduction into the molten solder. Inadequate pretreatment results in dewetting of the solder on the copper surface.

For OSP, the same principle of cleaning the copper surface applies. OSP is usually run in continuous horizontal equipment. OSP is specific to the copper surface and forms a complex with the clean copper.

Immersion silver, as the name of the process implies, is an immersion or displacement reaction. It is driven by electromotive force. Pretreatment involves a cleaner and a micro-etch. The micro-etch is hydrogen-peroxide-based to produce a smoother copper morphology. A smoother topography eliminates the probability of bubble voids at the IMC after soldering.

Immersion tin pretreatment is based on cleaning and micro-etching. It is important that the immersion reaction initiates uniformly for better continuity of the tin deposit.

Multilayer Finishes

The pretreatment for ENIG, ENEPIG, and EPIG/EPAG has been addressed in detail in a previous column titled "ENIG and the Plating Process." What applied to ENIG is the same for ENEPIG and EPIG/EPAG.

Conclusion

Pretreatment plays a key role in the success of the process that it is designed for. Special attention to the front end of the line (pretreatment) is needed. Adhere to the supplier's instructions per the datasheet. A compromised or incomplete pretreatment could have devastating results that may lead to scrapping products. **PCB007**

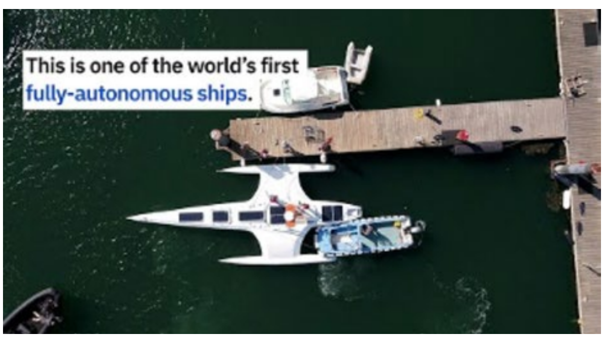
George Milad is the national accounts manager for technology at Uyemura. To read past columns or contact Milad, click here.

Mayflower Autonomous Ship Launches

Ocean research non-profit ProMare and IBM have completed and launched the Mayflower Autonomous Ship (MAS), an AI and solar-powered marine research vessel which will traverse oceans gathering vital environmental data.

Following two years of design, construction, and training of its AI models, the new fully-autonomous trimaran was lifted into the waters off the coast of Plymouth, England.

Designed to provide a safe, flexible, and cost-effective way of gathering data about the ocean, the new-generation Mayflower promises to transform oceanography by working in tandem with scientists and other autonomous vessels to help understand critical issues such as global warming, micro-plastic pollution, and marine mammal conservation. ProMare is coordinating the scientific studies working with IBM Research and a number of leading scientific organizations.



MAS features an AI Captain built by ProMare and IBM developers, which gives MAS the ability to sense, think, and make decisions at sea with no human captain or onboard crew. The new class of marine AI is underpinned by IBM's latest advanced edge computing systems, automation software, computer vision technology, and Red Hat open-source software.

"Able to scan the horizon for possible hazards, make informed decisions and change its course based on a fusion of live data, the Mayflower Autonomous Ship has more in common with a modern bank than its 17th century namesake," said Andy Stanford-Clark, chief technology officer, IBM U.K. and Ireland. «With its ability to keep running in the face of the most challenging conditions, this small ship is a microcosm for every aspiring 21st-century business."

(Source: IBM)

PCB007 Supplier Highlights

Rogers Corporation Introduces SpeedWave 300P Ultra-Low Loss Prepreg ▶

Rogers Corporation is pleased to introduce SpeedWave™ 300P Ultra-Low Loss Prepreg, which addresses the increasing need for stack-up flexibility in high layer count designs for 5G mmWave, high-resolution 77-GHz automotive radar, aerospace and defense, and high-speed digital designs.

Ventec Launches High-Speed Material Option Cladded With Thin-Film Resistor Foil ▶

For enhanced high-speed signal-handling performance required by the world's most demanding high-frequency PCB applications, Ventec International Group has launched a laminate option to its tec-speed 20.0 glass-reinforced hydrocarbon and ceramic laminate cladded with thin-film resistor material from Ticer.

Limata Launches X1000 Direct Imaging System Platform ▶

Limata, a provider of direct imaging systems for PCB manufacturing and adjacent markets, introduces the X1000, a flexible cost-efficient system platform for dry-film patterning and solder mask imaging designed for PCB manufacturers with quick turnaround production configurations.

Burkle North America Announces Headquarters Move to Greensboro Technology Center ▶

Burkle North America moved its headquarters from Cypress, California, to the Greensboro Technology Center, effective September 30, 2020. Strategically located service technicians and application support personnel will remain in their respective field offices located throughout the United States.

Aismalibar Adds Steven Calvert as Field Applications Engineer ▶

Steven Calvert joins the Aismalibar team with over 25 years' experience working within the European and North American manufacturing industries.

Isola Exhibits High-Reliability Copper-Clad Laminates at Virtual PCB West ▶

Isola Group, the leading global and local manufacturer of copper-clad laminates and dielectric prepregs for use in PCBs, participated in the virtual PCB West conference.

MacDermid Alpha to Revolutionize mSAP With New HDI Compatible Low Etch Direct Metallization Processes ▶

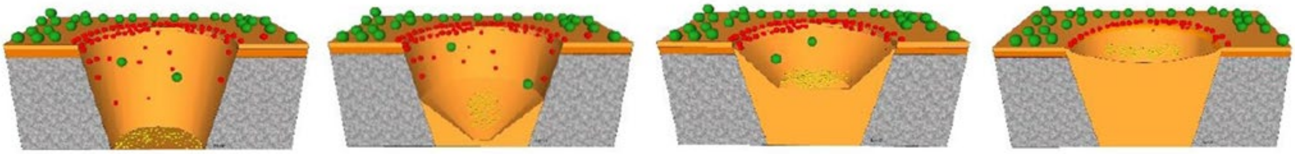
MacDermid Alpha Electronics Solutions, a global leader in specialty materials for electronics, announced the release of Blackhole LE and Eclipse LE, significantly upgraded direct metallization technologies for use in the manufacture of high-density mobile PCBs.

TSK Schill GmbH Supplies Rohde & Schwarz With New Chemical Tin Line ▶

After on-schedule delivery and successful installation of a horizontal chemical tin line at Rohde & Schwarz's Teisnach plant, the customer is now equipped for the future. TSK has also succeeded in implementing the requirements of this project with high precision and quality.

Ucamco Releases Integr8tor v2020.08, Introduces UcamX Workflow Edition ▶

Ucamco is happy and proud to present Integr8tor v2020.08. The newest release comes with a series of significant improvements, including the brand new UcamX Workflow Edition (WE) Graphics Editor.



Advanced Packaging Substrate Metallization Processes in the Age of Heterogeneous Integration

Article by Leslie Kim, Jordan Kologe, Bill Bowerman, Kesheng Feng, and Richard Bellemare
MACDERMID ALPHA ELECTRONICS SOLUTIONS

Introduction

In the first half of 2020, FC-BGA substrates have shown 30% YoY growth, with continued growth alongside FC-CSP expected in the upcoming years due to robust demand and increasing complexity of package designs. Package complexity is being driven by market growth in servers, storage, 5G network infrastructure, various AI acceleration, and with the increasing adoption of heterogeneous integration in chip design.

Heterogeneous integration addresses the increasing requirements for low-power, low-latency, and real-time data processing in devices by combining multiple components or chips on a substrate. The success of the system-in-package (SiP) in mobile electronics is a famous example of this. The reduced power and increased processing capability that is enabled by these types of designs enable the current generation of 5G-enabled smartphones and IoT devices, which will see major growth as we progress through the 5G and Industry 4.0 automation rollouts, respectively.

To meet the ever-increasing routing density requirements needed by all of this, today's organic substrate manufacturers are using a selection of advanced metallization technologies to create line and space dimensions approaching that of wafer-level packaging.

In this article, we examine the metallization processes for the formation of fine lines and spaces on IC substrates. We touch on circuit formation and starting materials and key technological aspects of the semi-additive process (SAP) for IC substrate primary metallization. We also discuss electroplating technologies for RDL, coreless substrates, and thermal management; plating equipment for large area panel-level packaging substrates; and the anisotropic final etch for circuit definition.

Starting Copper Foil Thickness or Lack Thereof

High-end packages tend to have larger die sizes (200 mm^{2+}) with many I/O (1,000 up to 10,000) and may be combined with other dies or devices on the same substrate. The resulting routing requirements for these systems involve extremely high circuit density, very fine line/space geometries, and one or more redistribution layers. In contrast to HDI for PCBs,

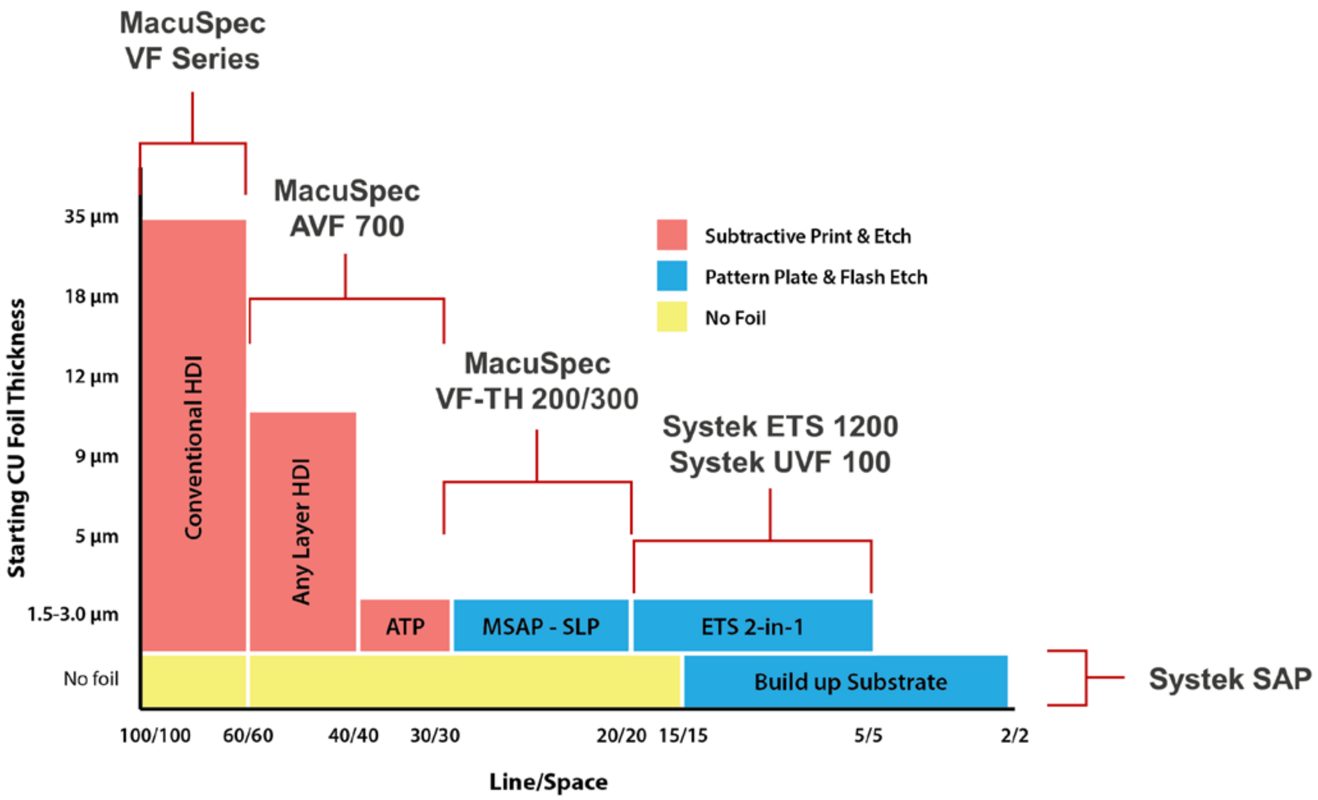


Figure 1: Starting copper foil thickness vs. line/space dimensions for various advanced PCB manufacturing applications and commercial metallization processes associated with them.

high-density circuitry for IC substrate manufacturing utilizes extremely thin or no copper foil on the starting substrate. For comparison, Figure 1 shows the trends in starting copper foil thickness for the various HDI manufacturing technologies used in PCB and IC substrate manufacturing.

SAP vs. mSAP

To achieve the electrical routing requirements for the highest-density interposers, SAP uses electroless copper to create an initial seed layer for buildup. Comparatively lower density IC substrate designs (and extremely high-density PCBs like those used in mobile boards) are done on thin copper foil laminate using the modified semi-additive process (mSAP).

SAP enables the finest line/space structures by building directly onto an organic laminate substrate material. The process starts on bare organic buildup material, such as ABF, that has been laminated onto the previous layer or core layer. After laser drilling microvias, the substrate is desmeared and metallized with a thin seed layer of electroless copper, pattern electroplated to create the copper required for the layer function, and then etched to remove the extra electroplated surface copper and the initial seed layer.

SAP technology allows for 10/10 µm line/space to be achieved. mSAP is in mass production today at dimensions below 30/30 µm line/space. The process uses conventional prepreg and ultra-thin copper foil (~3 µm) as the starting substrate. Microvias are laser-drilled, and then the panels are desmeared, processed through a primary metallization process—such as electroless copper or a carbon direct metallization process—imaged, pattern plated, and then etched down to the laminate between the features.

In both processes, an anisotropic final etch is utilized, which preferentially etches away the copper at lower areas faster than higher areas, limiting the amount of surface copper removed from traces and other features while

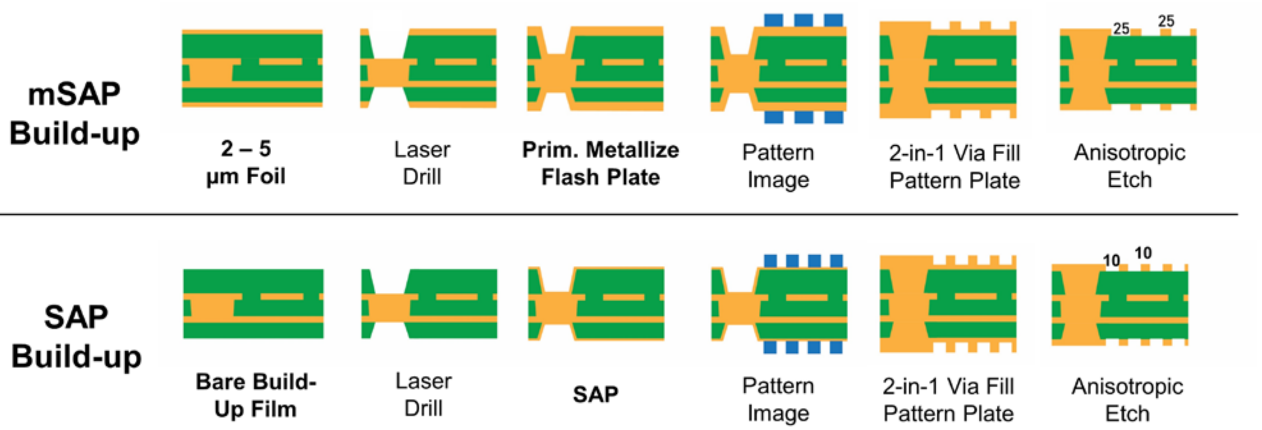


Figure 2: SAP enables finer lines and spaces for IC substrate RDL.

cleaning out and defining the spaces between the lines. SAP allows for finer lines and spaces than mSAP primarily since it requires fewer additive steps of copper plating and less etching to achieve the final definition of the plated features. Figure 2 shows the key differences in the two processes.

SAP: Key Primary Metallization Technology Considerations

SAP is a production-proven process for the metallization of buildup dielectric layers with electroless copper directly on polymer resin. The advantage of eliminating copper foil followed by subtractive etch is the capability to achieve finer line/space tracks and smaller land pads required for IC Substrates. High yields can be obtained at 12/12 µm line/space with continued development going forward below 10/10 µm.

The SAP electroless copper metallization process is similar to conventional metallization of rigid and flexible PCBs. The process has a desmear sequence, followed by surface conditioning and activation and finally an electroless copper seed layer between 0.7 and 1.0 µm. It is essential the seed layer of electroless copper has sufficient adhesion to the organic buildup material and to the blind microvia copper target pad. This is to provide support during electrolytic plating of the circuitry and to withstand thermal-mechanical stresses on the features during assembly and reflow. Figure 3 shows the SAP copper-to-resin interface.

A combination of chemical and mechanical adhesion is required to prepare the substrate for electroless copper adhesion. The permanganate desmear chemistry is used to oxidize the epoxy resin surface, providing more hydrophilicity. As the density of pin count increases, the line widths and land sizes decrease to accommodate the fan-out requirements.

Density requirements coupled with high-signal speeds mean that adhesion of the seed layer to the dielectric without significant roughening of the buildup material during desmear is a required attribute of SAP technology. This is challenging given the variety of epoxy resins, fillers, and glass beads or fibers available for buildup dielectrics. Commercial systems such as the Systek SAP Desmear process show compatibility with multiple commonly used substrates at below-specification roughness (Figure 3).

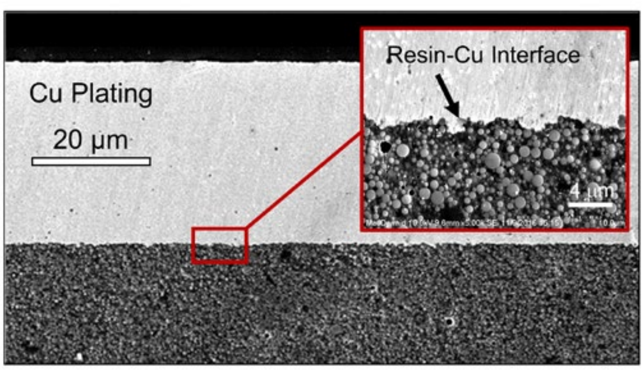


Figure 3: Copper adhesion at the resin-to-copper interface is a critically important metric for the semi-additive seed layer performance.

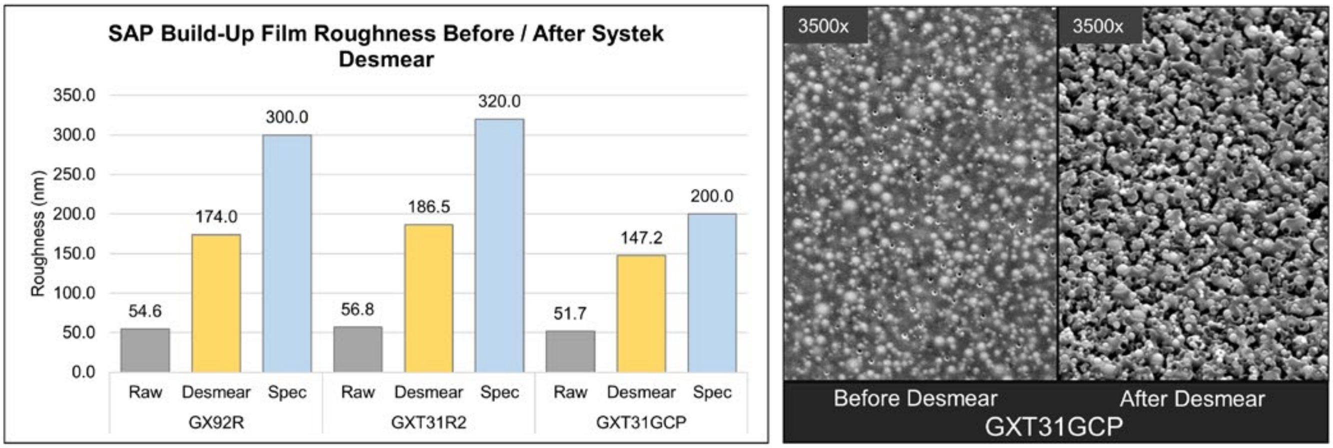
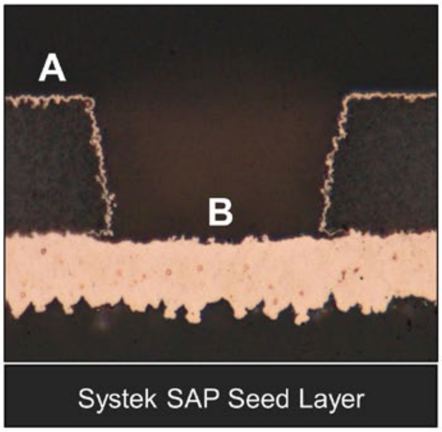


Figure 4: Below-spec roughness of substrate material is a desirable property for substrate electrical performance.



Location	Copper Thickness (μm)
Substrate Surface (A)	0.85
	0.82
	0.98
Via Target Pad (B)	0.81
	0.70
	0.93
Throwing Power	92.10%

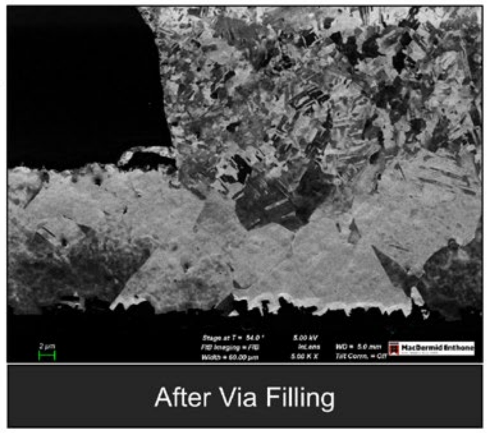


Figure 5: A uniform coating during the SAP seed layer plating is necessary for reliable via filling.

To promote chemical bonding to the resin surface, Systek SAP includes a conditioning step after desmear that adds functional groups to the resin surface, followed by a conventional cationic conditioner. The next step activates the surface with ionic palladium activator and reducer baths. The electroless copper seed layer plating can be done with Systek SAP Copper 850, an optimized formulation for near-zero internal stress with tensile strength up to 30,000 psi and elongation between 10–14%.

Throwing power of the electroless copper in an SAP process needs to be excellent so that a uniform coating is plated across the entirety of the microvia structure. Figure 5 shows the via structure after Systek SAP with Systek Copper 850, the copper thickness on the substrate surface and at the via target pad, and the subsequent filling after electroplating with Systek UVF 100.

Peel strength measurements are taken by plating a minimum of 30 µm of electrolytic copper and then peeling the foil from the dielectric surface with an Instron Universal Testing System. Peel strengths exceed the customer's target on the three buildup films tested.

A leading-edge advanced SAP for 1–2-µm line/space has been developed for R&D feasibility projects at this time. This advanced metallization uses a non-formaldehyde electroless copper and electrolytic flash for minimization of undercut after the final etch.

Electrolytic Copper Plating for RDL

The most common type of electroplated structure for package routing in IC substrates is the redistribution layer (RDL), which creates horizontal and vertical axis interconnects for relocating I/O pads of the integrated circuit. RDL is used to create connections within het-

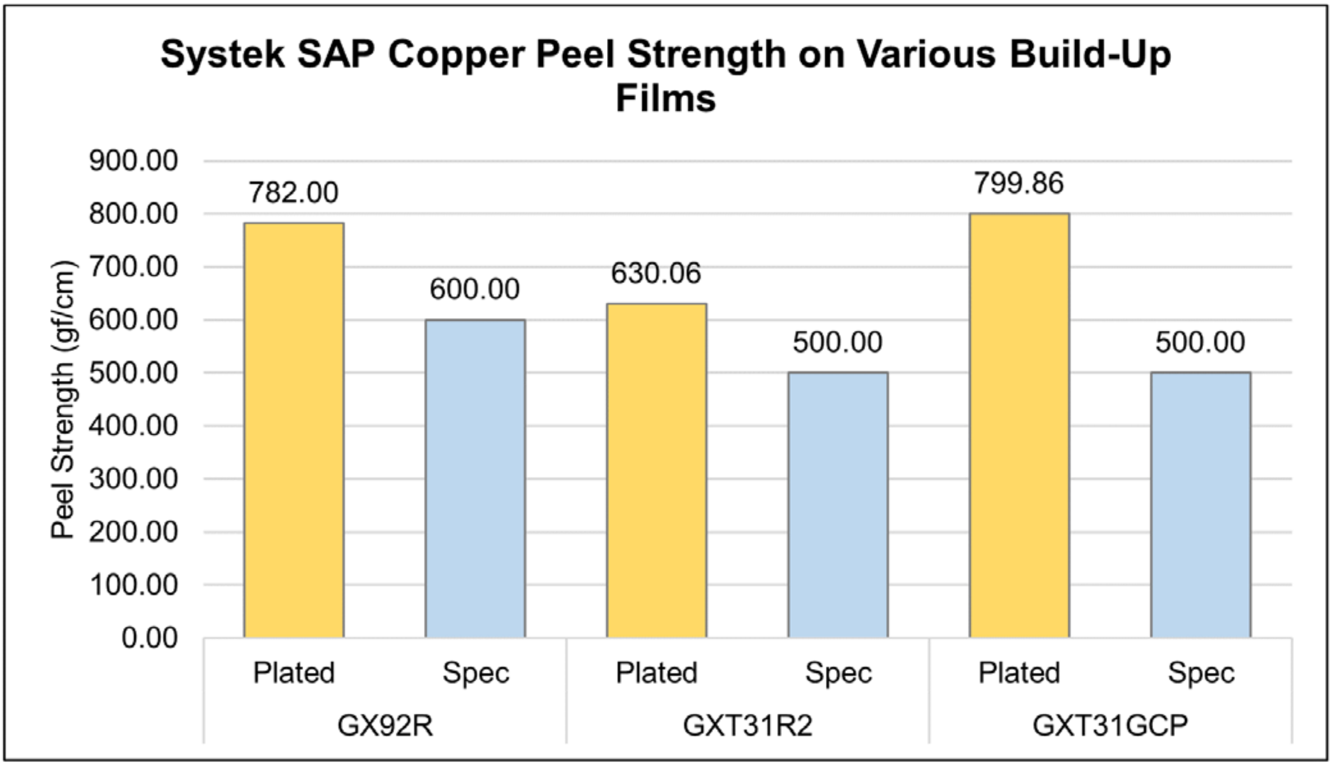


Figure 6: Peel strength of SAP copper plated on multiple ABF substrates.

erogeneous designs to other components, for high-density pitch and interposer routing in fan-out packaging and more.

At the leading edge of the technology are electroplating chemistries that can fill the vertical via connections while also plating the subsequent layer's fine line traces in a single step [1]. These processes build electrolytic copper to precise dimensions on both SAP buildup substrates and the ultra-thin foil substrates used in mSAP and advanced tenting processes (ATP) and are a tremendous enabler for advanced packaging. Figure 7 shows the location of the RDL plating in a chip package diagram.

RDL copper via filling baths have high concentrations of copper (up to 250 g/L), lower concentrations of sulfuric acid (50 g/L), and a combination of a wetter (or carrier), brightener, and leveler to promote rapid filling. The additives work together to control the plating rate, the flatness of the deposit, and overall physical properties of the copper. The brightener acts to accelerate the plating deposit. The wetter is a high molecular weight polyoxyalkyl compound that suppresses the plating by

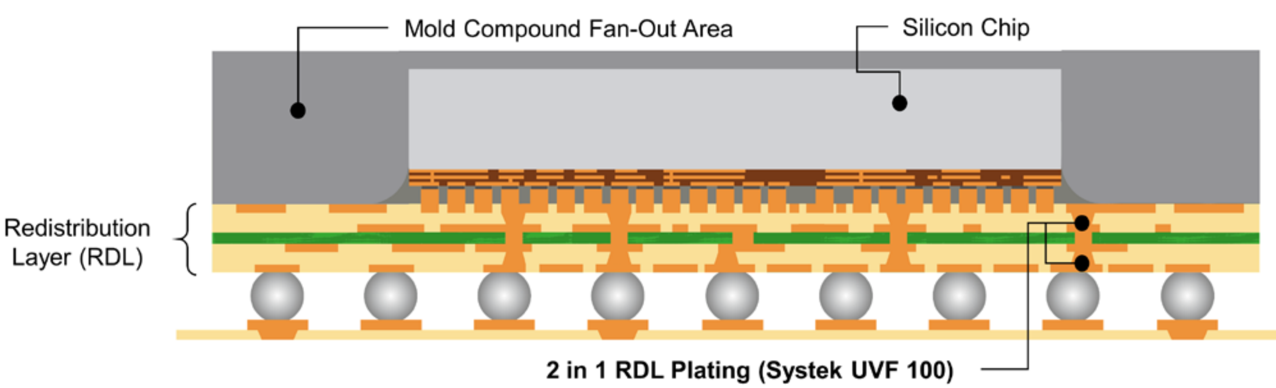


Figure 7: RDL features created with two-in-one via filling and fine-feature plating enable organic substrate buildup.

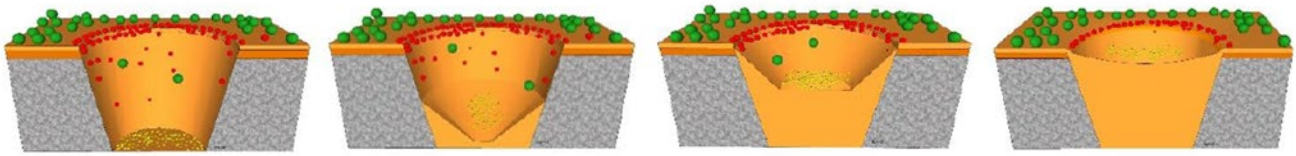


Figure 8: Curvature-enhanced-accelerator-coverage is the result of interactions of the wetter, brightener, and leveler over the course of bottom-up via filling.

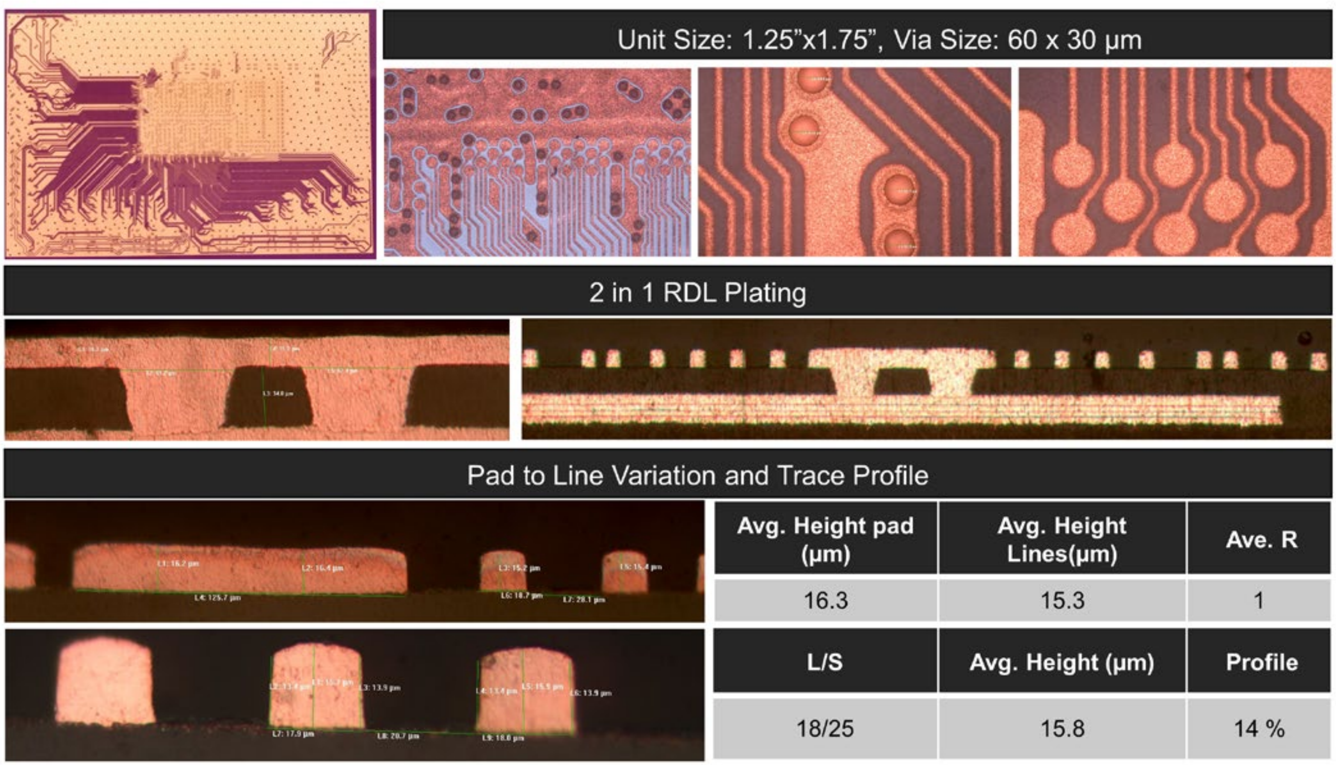
adsorbing on the copper surface through interaction with the chloride ion. The leveler suppresses plating rate by increasing the diffusion layer thickness.

Through the effect of their combined mechanisms, these chemical additives alter the electrical properties at multiple locations on the cathode surface as the via bottom-up fills, resulting in a leveling off of plating once the surface has become uniform. This is known as curvature-enhanced-accelerator-coverage (Figure 8).

Copper via fill additives are optimized for different plating methods. In any-layer plating, the carrier is formulated for high suppression of the surface copper. The plating process is done by panel plating, so there is little variation of the surface current density. Vias can be filled with as little as 10 µm of surface copper thickness. This is advantageous for use with ultra-thin mSAP foils and tent-and-etching in the advanced tenting process.

RDL via fill additives are optimized for pattern plating. The design of the carrier molecule is to promote straight wall pattern plating with a minimum of doming. RDL plating is designed to plate the conductor height uniformly regardless whether the structure is a fine line or land area. The panel shown in Figure 9 was pattern plated with Systek UVF-100 and featured 128 pieces (32 mm x 45 mm units) with vias 60 µm wide x 30 µm deep and 18/25 µm line/space, plated at 1.94 ASD (18 ASF) for 50 minutes in a VCP plating tool.

RDL plating baths are versatile tools for the IC substrate fabricator. The process is most typically run in a vertical continuous plater (VCP) with direct impingement by mini educ-



Avg. Height pad (µm)	Avg. Height Lines(µm)	Ave. R
16.3	15.3	1

L/S	Avg. Height (µm)	Profile
18/25	15.8	14 %

Figure 9: Systek UVF 100 pattern plating on IC substrate RDL.

Panasonic

Ultra-low Transmission Loss Multi-layer Circuit Board Materials for ICT Infrastructure Equipment

MEGTRON7 (G)type NEW

Laminate R-5785(GN), R-5785(GE)
Prepreg R-5680(GN), R-5680(GE)

(GN):Low Dk Glass cloth type (GE):Normal Glass cloth type

Features

- Improved lamination processability compare to MEGTRON7 R-5785(N)
- Glass transition temperature (Tg): 200℃ (DSC)
- Multi-site production in Japan/China

	Dk	Df
R-5785(GN)	3.4	0.002 @ 12GHz
R-5785(GE)	3.6	0.003 @ 12GHz

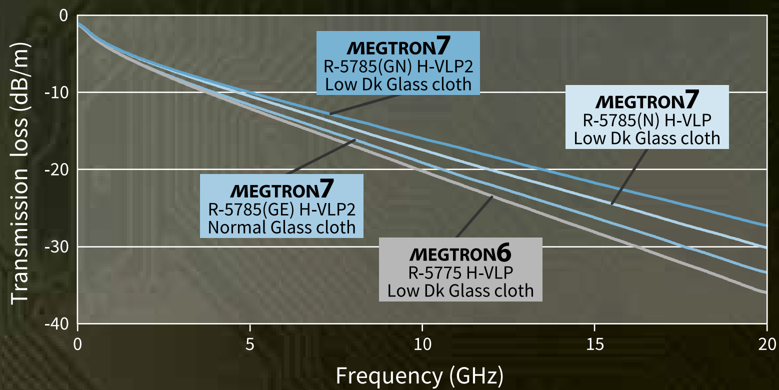
Applications

- High-end servers, High-end routers, Supercomputers, and other ICT infrastructure equipment, Antenna (Base station, Automotive millimeter-wave radar), etc.

Transmission Loss

- Construction

Trace thickness(t)	18μm
Dielectric thickness(h)	300μm
Copper thickness	18μm
Inner treatment	No-surface treatment
Core	0.15mm (#1078 x 2ply)
Prepreg	0.15mm (#1078 x 2ply)
Line length	1000mm
Impedance	50Ω



The above data are typical values and not guaranteed values.

Contact us

More information

DISTRIBUTOR IN NORTH AMERICA
MATRIX USA INC.
TORONTO • SANTA ANA • SANTA CLARA • CHICAGO • MINNESOTA
Visit our website at www.matrixusa.us

Partnering to go beyond.

Electronic Materials
Panasonic Corporation

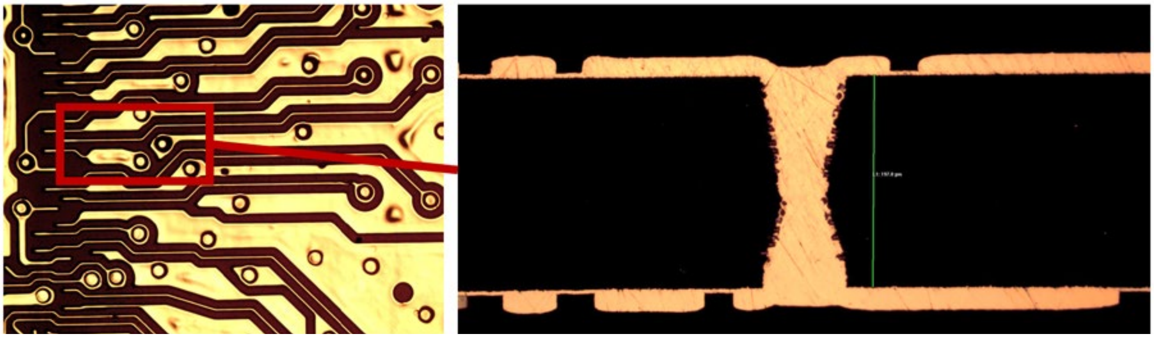


Figure 10: Double-shot laser-drilled core plated with Systek UVF 100 image before final etch.

tors mounted on vertical spargers. The impingement is ideal for solution exchange in the microvias and shortens plating times while promoting uniformity. The same RDL chemistry can be used to plate a wide variety of via diameters and depths as well as through-vias in cores without chemical adjustments. Figure 10 shows a core that was double-shot laser-drilled, metallized, and pattern plated in Systek UVF 100. Uniform height between traces of varying sizes and minimal dimple over filled vias is important for ease of buildup processing.

Coreless Package Substrates

Many flip-chip CSP packages use a two- or three-layer embedded trace substrate (ETS) that has a coreless design. The initial layer starts as a copper carrier that is imaged on a single side with line/space down to 7/7 µm. The panel is electrolytically plated with a specially formulated plating process to form very square trace corners without doming, have excellent co-planarity between fine line tracks and land areas and have low internal stress to prevent warpage [1]. After plating, the resist is removed, and the panel is backfilled with resin followed by one or two RDL layers. Figure 11 shows coreless processing.

Figure 12 shows a cross-sectional view of an initial M1 layer plated with Systek ETS 1200 on a VCP line. After these features are plated and the resist removed, the substrate is encapsulat-

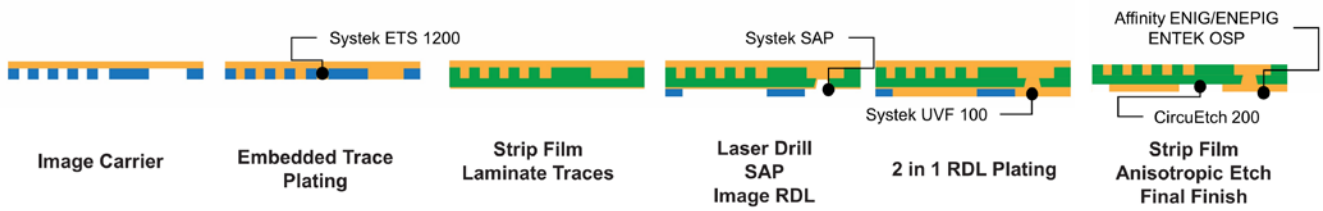


Figure 11: Coreless buildup process for IC substrate.

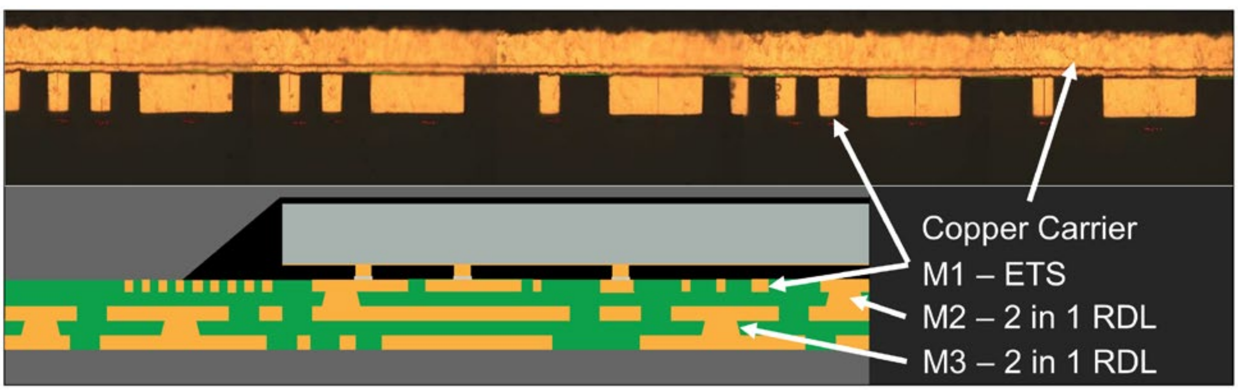


Figure 12: Coreless substrate buildup starts with ETS plating on a removable copper carrier, which is then encased into prepreg and built up with RDL plating.

ed in prepreg to encase the traces, laser-drilled, and then the M2 layer is metallized with a 2-in-1 plating system like the Systek UVF 100 to create the RDL. The copper carrier is stripped away, leaving extremely square traces after removal, providing an outer layer with fine line/space that has superb electrical properties.

Thermal Management With Through-Hole Fill

Due to increases in package density, thermal management has become a key area of focus for substrate designers in recent years. Thermal management of interconnect platforms requires heat extraction from hot spots and heat transfer through the package to maintain desired operating temperatures. As package architecture seeks to increase the power density into smaller form factors, the total heat dissipation becomes more challenging.

One tool available to designs is solid copper vias for IC substrate and board-level systems. Through-via fill with copper is already widely used in LED lighting substrates to remove heat from the contact pads and reduce package temperatures for long life reliability. In the example, the junction temperature of the LED package was lowered by 34°C with the use of copper-filled vias.

There are many advantages to using copper-filled vias compared to conventional plugging of the holes. The solid copper pillar-like structure is very structurally robust and will easily withstand the stresses of thermal excursions. The through-via copper has a consistent CTE with stacked vias to reduce thermal-mechanical stress on the substrate in assembly and life cycling.

Fabrication of through copper vias has recently seen an innovation using a unique single-step plating process that bridges mechanically or laser-drilled holes with electrolytic copper, forming two separate blind vias on either side, and then fills the structure to a flat surface [2]. The process is capable of filling vias with aspect ratios up to 3:1, cavity-free, with minimal surface copper plating. This reduces or even eliminates the need for planarization and minimizes the amount of etch to maintain tight trace geometries for controlled impedance.

Through-vias can be formed by double-shot laser or mechanical drilling. Currently, the only available commercial process that can

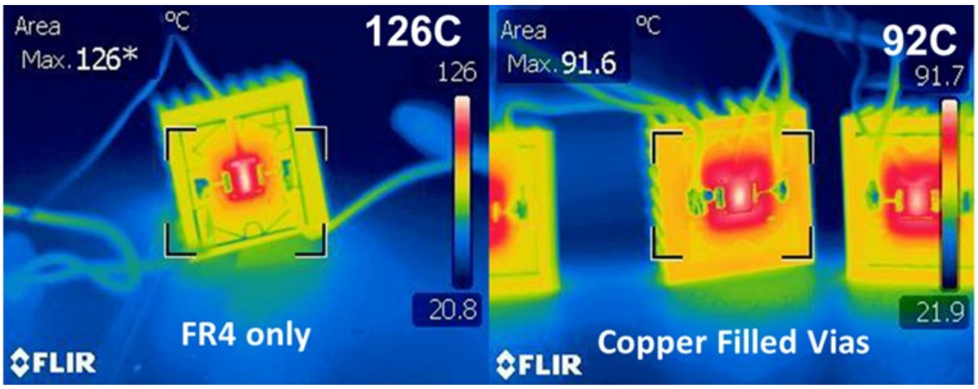


Figure 13: The addition of copper thermal vias significantly improves the operating LED junction temperature for longer operating life.

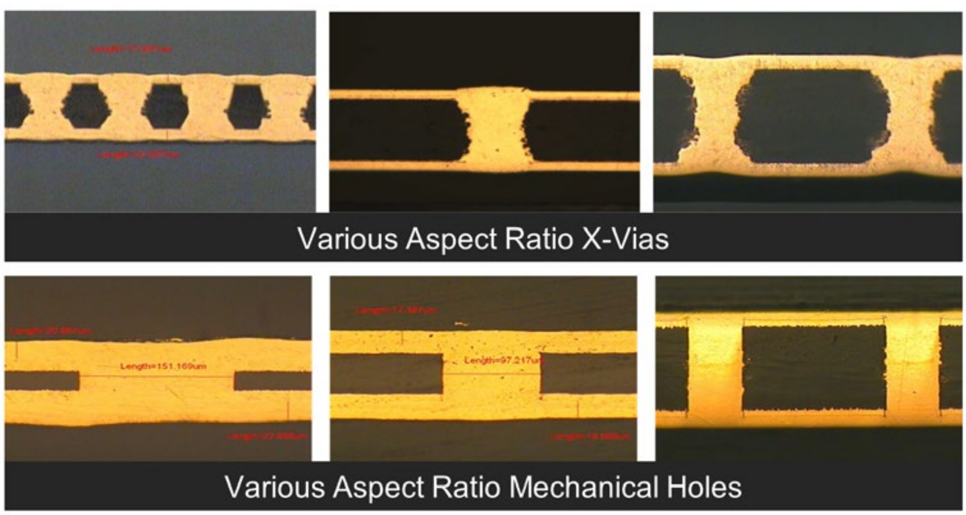


Figure 14: Single-step through-hole filling for the core layer of IC substrates has benefits, ranging from improved thermal management to improved structural stability.

achieve this in a single step is the MacuSpec THF 100 process, which can be installed in VCP plating lines or conventional hoist tanks with direct solution impingement and pulse rectification.

Large Area Plating Cells: Uniform High-Speed Copper Plating for Panel-Level Packaging

Large-area or panel-level format is driven by a quest for lower packaging costs. Large panel formats of 510 mm x 515 mm up to 600 mm x 600 mm and even larger sizes typical of display manufacturers present unique technical challenges for plating and tooling but offer new options for hybrid packaging and designs required with heterogeneous integration. Single-panel plating cells have been developed to control the current density over the large panel area, similar to a fountain plating tool for wafers. For organic and glass substrates, specific plating chemistries have been developed for use in SEMSYSCO HSP tools.

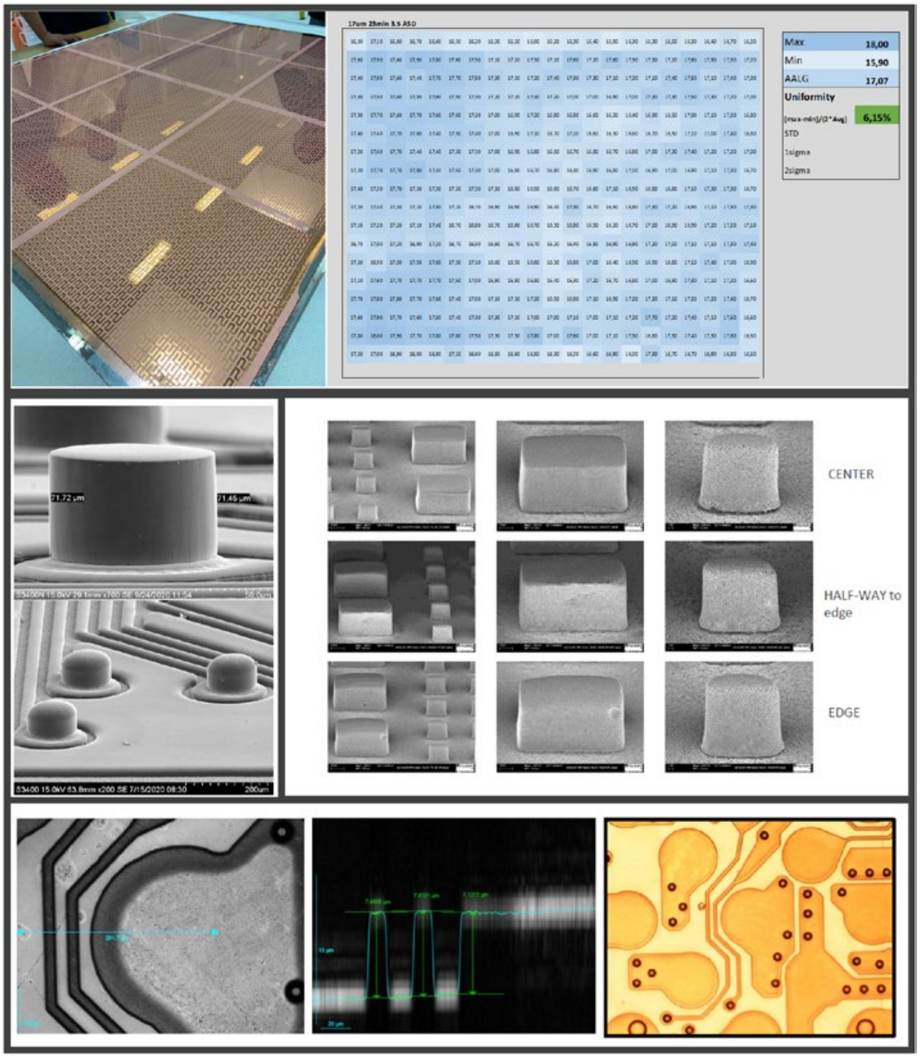


Figure 15: Panel-level equipment testing. Large-area Gen5 glass substrate (top left); large-area within-panel copper plating height distribution for panel-level plating equipment (top right); substrate-side copper pillar plating for advanced packaging (middle left); within-unit distribution photography of test panel for pillar plating chemistry (middle right); and panel-level scale RDL plating example, showing homogenous deposit on lines and pads, even height distribution between lines, and pads and flat shape profile on pad (bottom).

Large-scale RDL and copper pillar features can be obtained with the right match of plating additives and plating tool. These systems can control the Z-axis height within tight tolerances within the unit and across the panel and are successfully operating in mass production today. MacDermid Alpha and SEMSYSCO have partnered to develop an HSP tool that can handle 600 mm x 600 mm panels located in the MacDermid Alpha GDAC in Zhongli, Taiwan. This tool is utilized in conjunction with customers to test process chemistries on various panel designs and applications.

Figure 15 shows an example of a large area format on a Gen5 glass substrate, 1100 mm x 1300 mm in size. These substrates are plated at 3.5 ASD for 23 minutes for a target feature height of 17 µm. Results were an average of 17.1 µm with a range of 15.9 to 18 µm. The process chemistry was Systek BMP-LP for pillar plating, and Systek UVF 100 for RDL plating, while the plating tool was a SEMSYSCO HSP.

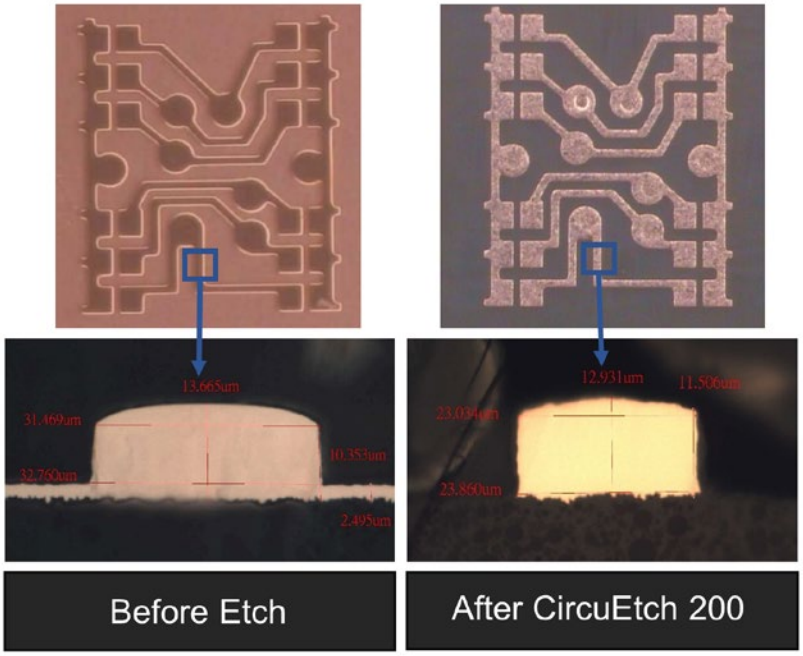


Figure 16: It is critically important that the final etch does not undercut the trace and retains a rectangular cross-section after etching, without removing significant amounts of surface copper.

Anisotropic Etching for SAP and mSAP

The final fabrication step for circuit formation is the final etch that removes the 1 µm of SAP electroless copper in the SAP process or 2–3 µm of ultra-thin foil in mSAP or ATP processing. High-performance sulfuric-peroxide etchant systems are utilized to ensure maximum circuit density, trace geometry, and excellent adhesion. A precision etching process that does not significantly reduce trace width is an enabler for circuit density because the line and space tracks can be placed closer together.

The anisotropic etching aspect of the process means that it etches, at a greater rate, the copper between the traces without reducing the surface height or impacting the square shape of the traces, maintaining electrical performance. Furthermore, these processes must also not undercut the interface between the substrate and the trace or adhesion issues could appear during the device assembly and end-use.

Summary and Conclusion

The brief overview given on metallization technologies for advanced packaging only scratches the surface of what currently is possible for these increasingly used interposer solutions. The adoption of panel-level substrate designs will only further the leveraging of these metallization technologies to meet the needs for cost reduction and quick design solutions in the coming wave of advanced designs utilizing heterogeneous integration to enable the future of post-Moore computing. **PCB007**

References

1. Dharmarathna, S., Bowerman, W., Watkowski, J., & Feng, K., "Embedded Trace and RDL Copper Plating Process for Panel Level Packaging Applications," iMAPS Device Packaging, 2020.

2. Gugliotti, C., Bellemare, R., Oh, A., Blake, R., & Desalvo, D., "Single-Step Metallization Process for the Filling of Through-Holes With Copper," SMTAI, September 2020.

Leslie Kim is IC substrates manager, MacDermid Alpha Electronics Solutions.

Jordan Kologe is technical marketing specialist, MacDermid Alpha Electronics Solutions.

Bill Bowerman is director of primary metallization technologies, MacDermid Alpha Electronics Solutions.

Kesheng Feng is director of research, metallization, MacDermid Alpha Electronics Solutions.

Rich Bellemare is director of electrolytic plating, MacDermid Alpha Electronics Solutions.

MilAero007 Highlights

Fresh PCB Concepts: Advantages of Application-Engineered PCBs ▶

When working with your PCB supplier, do you have a dedicated engineering resource to help with the design of your PCB before fabrication? How about a resource that has experience and knowledge about the different applications for PCBs? Jeffrey Beauchamp explains how this is one of the most important and valuable factors when producing high-reliability PCBs, as well as what—or who—this resource could be.

Standard of Excellence: Five Ways to Ensure You Have the Right Military PCB Supplier ▶

With the current shortage of qualified and certified military PCB suppliers, finding one has become more challenging than ever, and the trend toward consolidation over the past few years has only added to the shortage. Anaya Vardya shares five guidelines to consider when developing a bilateral relationship with your military PCB supplier.

Defense Speak Interpreted: The Defense Innovation Unit ▶

Many of Denny Fritz's columns are about new defense technologies and innovations, but what about an organization with "innovation" in its name? Here, he describes the history and purpose of the Defense Innovation Unit, as well as some of its programs.

IPC Statement on NDAA Provisions Aimed at Bringing Resiliency and Security to Supply Chains ▶

IPC, the global association of electronics manufacturers, issued a blog post in support of the FY 2021 National Defense Authorization Act provisions that would bolster the resiliency and security of the electronics manufacturing ecosystem, including PCB fabrication and PCB assembly, the green-and-gold hardwiring at the core of all electronics systems.

Advanced Assembly Earns AS9100D Certification ▶

Advanced Assembly announced it received the AS9100D certification. The certification was awarded after an extensive audit conducted by NQA, a division of NTS.

BAE Systems Awarded Radar Contract for Royal Air Force's Eurofighter Typhoons ▶

BAE Systems and Leonardo have been awarded a contract to develop the Active Electronically Scanned Array, the European Common Radar System Mark 2 radar, to a standard ready to be integrated on to RAF Typhoons.

Air Force Awards Contract for New ICBM System to Strengthen U.S. Triad ▶

The Department of the Air Force awarded an Engineering and Manufacturing Development contract for the Ground-Based Strategic Deterrent (GBSD) intercontinental ballistic missile (ICBM) program to Northrop Grumman on September 8.

Mr. Laminate Tells All: Is Your Laminate and Prepreg Supplier Cheating? Only One Way to Find Out ▶

According to Doug Sober, a huge void now exists in the base materials specifications for PCBs and PCB assemblies with the inactivation of MIL-S-13949 for base materials and the loss of the military's oversight function. IPC-4101 replaced the specification for MIL-S-13949, but there was no mechanism established for an oversight function.

Stacked Microvia / Weak Interface Reliability Study

Article Edited by Happy Holden
I-CONNECT007

At the IPC High-Reliability Forum, Marc Carter gave a presentation on a study that covered stacked microvia/weak interface reliability. I have assembled the highlights of Marc's presentation, including the transcript, which has been slightly edited for clarity.

Marc Carter is the president and owner of Aeromarc LLC, as well as an I-Connect007 columnist. He has worked in the electronics interconnection industry since 1984 in a variety of roles in fabrication and assembly materials, processes, environmental compliance, and supply chain management activities around the world. Marc has had the honor and privilege of working with and learning from many of the true giants of this industry in multiple functions over many years. His experience includes a major mil-aero OEM, field and development work at material suppliers to the printed circuit industry, and an educational stint as the sole proprietor of a manufacturer's agency representing multiple high-tech mil-aero material suppliers.

Background

I am going to outline a project that a number of us in the industry have undertaken, recognizing the lack of publicly shared information that has been commented on several times. Intended as a tool in guiding our future designs and procurement, this stacked microvia and weak interface reliability study is a three-year, three-phase iterative industry and academia collaborative research project.

The methodology we undertook does not try to look at everything. We did not try to "boil the ocean," and we wanted to approach it in manageable stages, each providing some immediately useful knowledge, revising subsequent stages based on what is learned. Here are some of the team participants that we are working with at this point:

- Fabrication: Calumet Electronics and Electrotek Corporation
- Simulation: ANSYS (Sherlock)
- Statistics: Michigan Technological University (MTU), electrical and computer engineering
- Test: Foresite Inc. and Robisan Laboratory
- Project facilitation: Aeromarc LLC

The industry has been using microvias for decades, and most of us shared a basic misconception about microvias and high-reliability applications. The microvia was believed to be the most robust type of interconnect. In many ways, it still is. This is a low-probability problem, but its latency and inability to be detected by traditional testing methods is unfortunate. Seeking certain density designs, we incorporated two, three, four, or more stacked microvias, possibly without sufficient forethought as to what that might do to uncover new failure mechanisms. Because of our preconceptions, we miss diagnosed problems quite often and early on. In some cases, companies drifted along for some years, thinking they uniquely had the problem—until they started comparing notes [1].

Marc Carter

We are in a containment position. We have received guidance from the IPC, and we have internal companies with their own guidance. You've seen the Motorola red, yellow, green structure [2]. That involves a kind of containment by limiting the complexity and being very careful to qualify sources because not everybody is equally good at this. Using intensive screening and perhaps over-conservatively defined lot rejection, this problem is corralled but limits advancement.

Many OEMs felt confident about what they were getting and fielding. With limited capability, especially as you get to the more complex structures, that limited capacity in the industry in North America. Some of those failures and rejections have reportedly led to late deliveries, etc. In today's world, the biggest impact is scheduling.

We have made a lot of progress in screening technology. Screening helps prevent escapes to the field. We are much further along in containment than we are in understanding the interaction with the multiple contributing mechanisms [3]. There are some papers listed. This project is intended to add to the publicly available knowledge of those mechanisms.

Project History

It was a little before mid-2019 that we started having conversations. From some of the candidate organizations—mostly centered around bemoaning the absence of definitive conferences of industry accessible data—we know that there is very good testing that has been done by some of the larger OEMs and large printed circuit networks. However, due to the nature of the commercial world we live in, a lot of that is proprietary IP and has been difficult sharing. That is perhaps starting to open a little bit. But when we started this project, it was a real problem, and the VTSL data sorting microvia group had hoped to do a lot of mining of existing data and was thwarted by that inability to get it past the IP police of various organizations.

We began the process of saying, "What are we going to do about this?" We began discussions among a select group of manufacturers, test organizations, simulation labs, and universities. The market segments were served, and similar processes were especially important.

One of the things that took the longest, if you are going to have two or more fabricators building a test vehicle, is getting an exact consensus on the details of layup and construction, which became an exceptionally long, hard, arduous process. In September of last year, the fabrication companies began the consensus material selection; we were in a fairly quick and early agreement. We wanted a material and stackup that was widely used and available, but perhaps not the most used, as the ultimate material. And that was also covered by those who would supply the material to support this test in return for access to the information.

In October of last year and running through at least January, the two fabricators collaborated in an exceptionally open manner. Those of us in the industry are used to helping each other out, but this was remarkable and resulted in a consensus on a detailed layup and layout for the test article. We struggled with that because, as those of you that are familiar with the industry realize or have recognized in the past, if you put the exact same stackup layout design in front of two different fabricators, there are differences in their press operation, relief pattern, panel layout, and DFM projection software. That will get you two different results. We finally had to give ground on one dielectric layer in each to get to an identical predicted structure. In February, the test labs that we are working with on this began consensus discussions will continue detailed sample handling and testing.

And in late April of this year, the project proposal was submitted to the U.S. Army's Cornerstone Group at Rock Island. I must stress that at this point, when this was submitted, many thousands of dollars and hours of time were invested because we were concerned about this problem. We have gone about as far as we can go off the cuff. We need to get some funding, and since this is aimed primarily at military applications and use, that's why we're going to Cornerstone with this.

Objectives

Project objectives were to provide publicly accessible information on some contributors to the weak interface failure mechanism. If you try to do an ideal design that covered every possible element on a fish-bone diagram, we would all be much older, grayer, and many millions of dollars poorer than we are today. We have taken the approach of getting this in bite-sized chunks. From a manageability standpoint, getting viable data was quickly deemed preferable to getting the ultimate answer to all problems and questions in 10 years. We have taken the mini-phase approach.

We are going to help determine current limits on reliable design production methods and materials for use in high-density interconnect microvia electronics and critical high-reliability applications. We are not building cellphones or addressing that. This is a narrow market segment.

We are very eager to help enable improved correlation between predictive modeling, simulation reliability, and actual results. This is one of the reasons that our friends from ANSYS are so willing to help with this; they very much want to improve their ability to handle all different structural types of high-density stacked/staggered microvia reviews and be much more confident that those are going to provide reasonably good predictability.

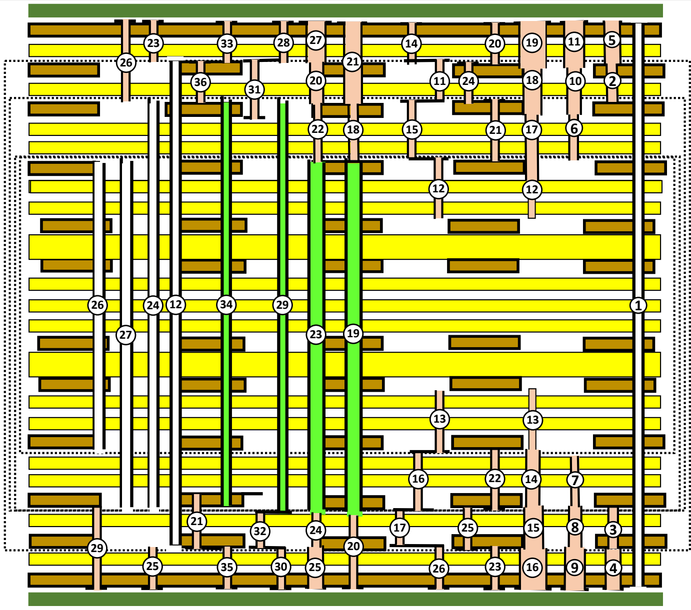
We are very eager to help enable improved correlation between predictive modeling, simulation reliability, and actual results.

Each phase of this project is designed to inform and direct subsequent phases in terms of specific structures, materials, manufacturing testing techniques, etc., and to successively improve the predictive modeling. The first results will be compared with the predictive modeling, the predictive modeling will be readjusted, and then the second phase will make the same iterative loop.

The test article is seen in Figure 1, including covers stacked and staggered from one to four. It is a little more aggressive than the iMac ESA Structure. It is probably less aggressive than Lockheed's structure. We purposely chose to limit it to a single material in this first phase. It will provide a readout, though, on a few commonly commonly employed structural choices during the design phase. It gives staggered microvias in varying offset staggered, and there are a couple of microvia sizes there.

Methodology and Variables

- "Shop A" vs. "Shop B"
- Structure (stack height, stacked vs. staggered, stacked over buried, degree of offset, etc.)
- 17 different D structure coupons were required (when metallization included)



Layer	Min	Max	Thickness (Inch)	Family	Description	Type DK / DF
SM1				TAIYO HFX		0.00 / 0.0000
L1			0.00042	Copper Foil	.375	POWER GROUND-COPPER FOIL
			0.00273	370HR	2113-59%	4.02 / 0.0210
L2			0.00162	Copper Core	.375 + 0.0007	SIGNAL – COPPER
			0.00273	370HR	2113-59%	4.02 / 0.0210
L3			0.00162	Copper Core	.375 + 0.0007	SIGNAL – COPPER
			0.00330	370HR	106-76%	3.74 / 0.0210
				370HR	106-76%	
L4			0.00162	Copper Core	.375 + 0.0007	SIGNAL – COPPER
			0.00412	370HR	106-76%	3.74 / 0.0210
				370HR	106-76%	
L5			0.00060	Copper Core	.5	SIGNAL
			0.00500	370HR	0.0080 (1-7628)	4.28 / 0.0210
L6			0.00060	Copper Core	.5	SIGNAL
			0.00504	370HR	1080-65%	3.90 / 0.0210
				370HR	1080-65%	
				370HR	1080-65%	
L7			0.00060	Copper Core	.5	SIGNAL
			0.00500	370HR	0.0080 (1-7628)	4.28 / 0.0210
L8			0.00060	Copper Core	.5	SIGNAL
			0.00412	370HR	106-76%	3.74 / 0.0210
				370HR	106-76%	
L9			0.00162	Copper Core	.375 + 0.0007	SIGNAL - COPPER
			0.00330	370HR	106-76%	
				370HR	106-76%	
L10			0.00162	Copper Core	.375 + 0.0007	SIGNAL – COPPER
			0.00273	370HR	2113-59%	4.02 / 0.0210
L11			0.00162	Copper Core	.375 + 0.0007	SIGNAL – COPPER
			0.00273	370HR	2113-59%	4.02 / 0.0210
L12			0.00042	Copper Core	.375	POWER_GROUND-COPPER FOIL
SM2				TAIYO HFX		0.00 / 0.0000

Figure 1: Test vehicle article showing stackup, materials, constructions, and thicknesses.

- Reflow simulation temperature (eutectic, 230 °C, vs. lead-free, 260 °C; 10 reps)
- "Test Lab A" vs. "Test Lab B"
- Microvia formation method (mechanically drilled vs. laser-ablated, such as UV/CO_2/UV)
- Metallization (direct metallization vs. electroless copper)
- Note: Laminate material is not a variable in Phase 1

Some of the variables will be examined. Those of you who have been around the industry for a long time and have tried to do comparative studies of a particular problem or issue recognize that with the best of intentions and the most stringent controls on processes, process consistency and trying to match processes between two operations, is quite often the biggest and most statistically significant variable about who built the boards.

The two participating fabricators were selected in part because of the common processes they had and our ability to coordinate their efforts with back and forth shuttles. We have gracious technical support from chemical suppliers that supply the same direct metallization and electroless processes at both. We are making every effort we can to reduce the effect of uncontrolled variables but will try to capture that information and those side effects of shop-to-shop differences.

The structures we selected resulted in 17 different IPC-D structured coupons. Comparing direct metallization to electroless, that doubles. I will touch on reflow simulation temperatures later. There has been some discussion, and our test labs were very helpful in working through this. We are concentrating exclusively on the weak interface; we are not worrying about the various through-holes that are in the structure by necessity. Even more traditional microvia failures (cracks or voids in microvia sidewall, for example) are outside the scope of this study.

We intend to force the failure of the weak interface of the microvias by concentrating on the reflow simulation with the fabricator shops or test labs. Each test lab will get 102 samples of D-coupons from each of the two fabricator shops.

One of the variables will be microvia formation. And that is one of the differences between these two shops. Their microvia formation method: one is mechanically drilled, and

the other uses a UV/CO_2/UV laser formation technique. For metallization, both have the same electroless copper bath and the same direct metallization process offered by the same manufacturer.

Half of the coupons or panels at each shop will be done with direct metallization, and half will be done with electroless copper. And I must note that comparing different laminate material was not considered in phase one. We'd love to have the luxury of looking at different materials, but that's going to have to wait for phase two.

We expected to see some failures. I am counting on failures. The primary measurements for our statistics are going to be the survival number of cycles and the statistical likelihood of failure.

We're pretty confident we'll be able to do some good statistics on the relative significance of each individual variable. There has been a lot of work with each contributor to this problem. I'm going to be counting heavily on our friends at MTU, working on statistical analysis to see how much statistical reliability we can get from what really is—even though it is several hundreds of D coupons—still a small statistical sample. We need to see if we can determine the statistical significance of interactions.

One of the goals here is the final report out at a public venue, and the results will be the guide. Phase two and phase three structures are material and methodology.

Status

Build structures and data packages are ready to release to production, and materials have been donated by the material supplier. In return for access to the data, the raw material and technical support offered by both the material and the chemical suppliers have been very gratifying. The simulation will commence simultaneously with the start of the build. At this point, we have taken this project as far as we can out of pocket. We're waiting for funding.

Simulation for the sake of simulation is sort of a sterile exercise. Once we can commence the build of the test articles, then the simulation will begin. And we have talked about this before, but the equivalent of thousands of dollars has already been invested in this thing.

What is the cost to completion? Phase one would be rated at about $140,000 to just build test vehicles. Can you read that we estimate very conservatively? Time to completion is defined as this point of a phase one report out at a public venue is nine months after the funding is secured.

You may have noticed there has been some disruption of government finances in the past five months. There is some uncertainty. We have discussions ongoing about getting government entities to partner on funding through the Cornerstone Group. And for those of you who have tried to deal with government funding in the past, I can only recommend working through the Cornerstone Group as opposed to other funding venues that you tried to work with in the Defense Department. It is a far cleaner and more straightforward process, and the Cornerstone Group has been immensely helpful.

The future is obvious at this point for this group. We must secure the funding to complete phase one. We need to start getting some real data. Then, we can share that with others. One thing that was not immediately obvious in this from the start is that there was an area reserved on each of the panels that contains those test articles that each of the shops will retain for their own testing. They can perform their own internal and proprietary testing. That is fine. Everybody got something out of this discussion when we started this project. **PCB007**

References

1. IPC, "IPC Issues Electronics Industry Warning on Printed Board Microvia Reliability for High-Performance Products," March 6, 2019.
2. Bill Birch, "Reliability Testing for Microvias in Printed Wire Boards."
3. Yan Ning, "Reliability of Copper-Filled Stacked Microvias in High-Density Interconnect Circuit Boards," Doctoral Dissertation, UMD-CALCE, 2017.

A Process Engineer's Guide to Surface Prep and Dry-Film Photoresist Adhesion

Trouble in Your Tank

by Michael Carano, RBP CHEMICAL TECHNOLOGY

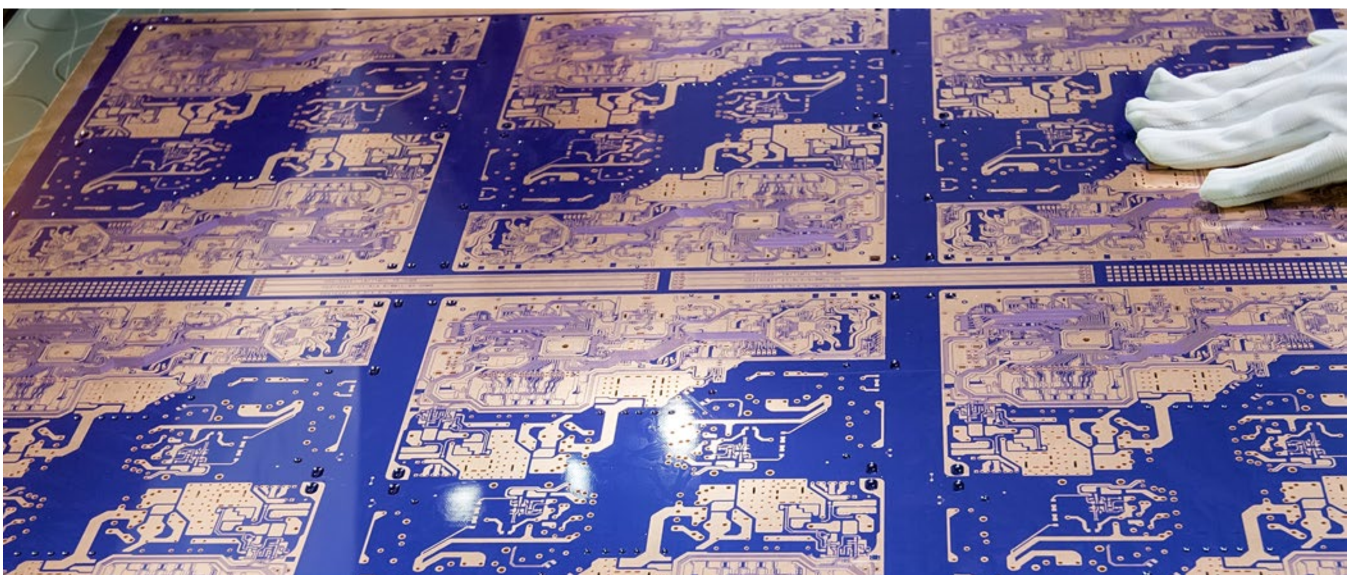
Introduction

One cannot underestimate the importance of surface preparation of the copper surface and its relationship to dry film adhesion. Further, the quality and dimensions of the circuit as it was designed depend heavily on the surface preparation of the copper foil. Certainly, we have witnessed a step-change in technology that has necessitated a total rethinking of how copper surfaces are cleaned and prepared to enhance photoresist adhesion.

Several of these changes are driven by cost pressures leading to substrate construction. The need to handle thin core materials, as well as lower copper foil thicknesses, is driving the move to alternative surface preparation techniques. And while many of these techniques are well-established, the drive to 5G, higher frequency transmission, and automotive changes—including crash avoidance and autonomous driving—higher-density designs with sub-three-mil lines and spaces are becoming the order of the day.

Thus, the first order of business is to prepare the surface for resist adhesion while reducing the amount of copper removal. In addition, designers prefer lower profile copper to effect improved signal integrity. In this context, low profile refers to the smoother, more uniform topography of the copper foil side facing the prepreg.

All this leads to increased emphasis on the adhesion of the photoresist to the copper substrate. Further, thinner core materials are prone to distortion and cold-working with mechanical surface preparation methods. Cold-working a metal can lead to the creation of internal stress, which then is the cause of copper foil cracking. For this reason, chemical cleaning methods are favored over mechani-



cal methods, as long as copper removal rates are reduced and excessive surface roughness is avoided.

Getting to Optimum Resist Adhesion

Let's review the task at hand. The objectives are simple. First, a clean, virgin copper surface is the first step to ensuring optimum adhesion. In addition, some surface restructuring is needed to provide anchoring points for the resist.

The ideal surface should include:

- Oxide-free
- Moisture-free (moisture causes resist to flow into holes, leading to lock-in)
- No pumice residues
- No fingerprints
- Complete chromate removal
- High surface area but somewhat uniform
- Water break test (holds film in water for 20–25 seconds)

Figure 1 shows an example of fingerprints, and Figure 2 demonstrates severe oxidation. The oxidation can be blamed on allowing moisture to remain on the boards without proper drying, or a heated dry was too hot. Oxidation leads to resist lock-in, making developing, resist stripping, and final etching problematic. Fingerprints are simply caused by poor handling procedures.

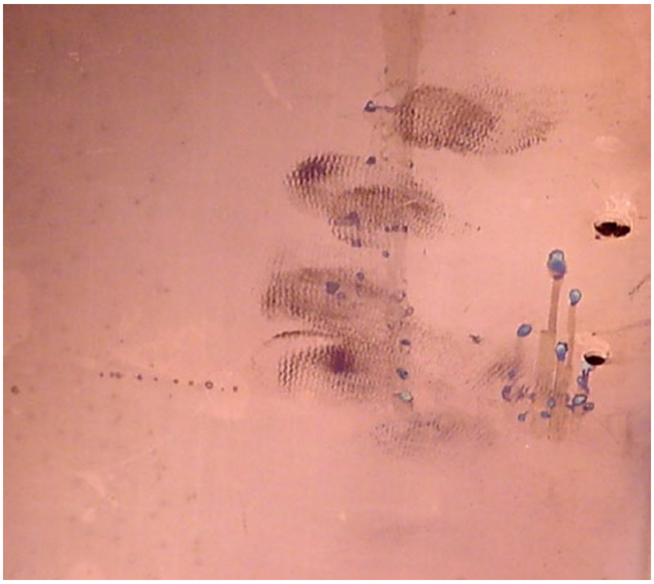


Figure 1: Example of fingerprints on copper.

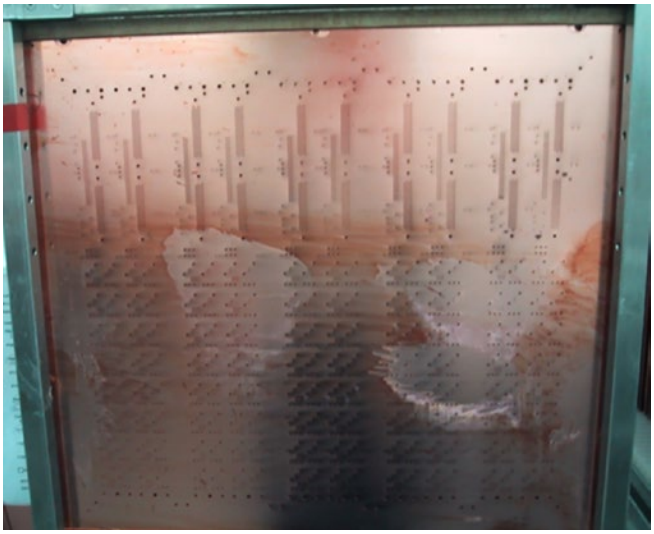


Figure 2: Oxidation. (Source: RBP Chemical Technology)

Keep in mind that rinsing after chemical processing steps is as important as the chemical processes themselves. Using counter-flow rinses and maintaining the cleanliness of the rinse water will minimize ionic contaminants from negatively impacting resist adhesion.

As stated earlier, oxidation will lead to resist lock-in. Fingerprints will prevent uniform adhesion of the film and will negatively impact surface preparation and final etching (Figure 3). The improper cleaning of panels, resulting in residues (i.e., fingerprints) remaining on the panel surface after precleaning before resist application, leads to the issue seen in Figure 3. Improper handling is also a potential root cause.

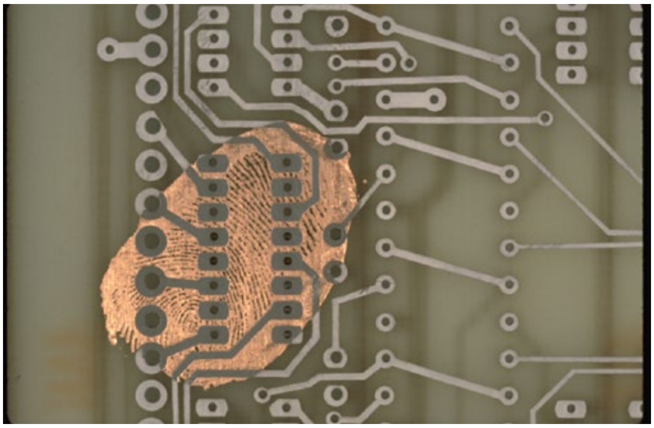


Figure 3: Example of oily fingerprint preventing complete etching of the copper. (Source: RBP Chemical Technology)

One should understand that copper foil producers apply an anti-tarnish coating (generally a chromate-based conversion coating). This helps maintain that cosmetic copper color. However, as the first step in surface preparation for inner layer processing, the chromate must be removed from the surface. Chromate thicknesses are somewhat non-uniform in practice. Regardless, before micro-etching the copper surface, it is highly recommended that the chromate be completely removed. This is accomplished with a mixture of strong mineral acids. It is recommended that a formulated acidic cleaner with some solvation properties (surfactants, solvents) be used to remove organic residues.

Proper surface cleaning before micro-etching or pumice treatment will minimize issues where the soils prevent uniform micro-roughening of the copper surface. My key point is chemical micro-etching, and pumice type treatments work best when the surface copper is free of organic soils and inorganic materials such as chromate coatings. The copper surface then is better able to obtain an acceptable surface roughness that will enhance resist adhesion.

Failure to completely remove soils prior to pumice or chemical micro-etching will only prevent the uniformity of the surface roughening process. Think of this as a surface where there are spots where there is very little, if any, roughening and where there could be areas of extreme roughness. This is not an optimum situation.

In addition, failure to remove chromates and other soils effectively will lead to what we call differential etching. Essentially, this means that during the surface roughening step (after chromate and soil removal), by employing a micro-etch formulation, the roughening will be less than optimal due to incomplete chromate and other soil removal. This negatively impacts the adhesion of resists. Understandably, in those areas where organic soils and chromates remain, the micro-etchant will have compromised ability to provide a uniformly structured surface.

Next Time

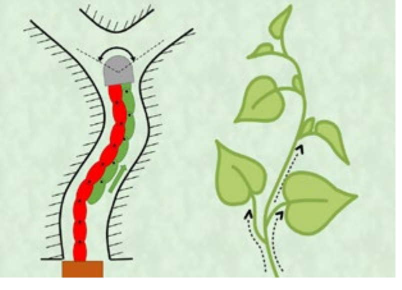
In a future column, I will explore the relationship between resist lamination parameters, developing, and etching. **PCB007**

Michael Carano is VP of technology and business development for RBP Chemical Technology. To read past columns or contact Carano, click here.

Flexible Yet Sturdy Robot Is Designed to 'Grow' Like a Plant

MIT engineers have developed a robot designed to extend a chain-like appendage flexible enough to twist and turn in any necessary configuration, yet rigid enough to support heavy loads or apply torque to assemble parts in tight spaces. When the task is complete, the robot can retract the appendage and extend it again, at a different length and shape, to suit the next task.

The appendage design is inspired by the way plants grow, which involves the transport of nutrients, in a fluidized form, up to the plant's tip. There, they are converted into solid material to produce, bit by bit, a supportive stem.



Likewise, the robot consists of a "growing point," or gearbox, that pulls a loose chain of interlocking blocks into the box. Gears in the box then lock the chain units together and feed the chain out, unit by unit, as a rigid appendage.

The researchers presented the plant-inspired "growing robot" last year at the IEEE International Conference on Intelligent Robots and Systems (IROS) in Macau. They envision that grippers, cameras, and other sensors could be mounted onto the robot's gearbox, enabling it to meander through an aircraft's propulsion system and tighten a loose screw or to reach into a shelf and grab a product without disturbing the organization of surrounding inventory, among other tasks.

(Source: MIT)

IPC Standards Development: Business Challenges and an Inside View

Article by Graham Naisbitt
GEN3 SYSTEMS

The rapid pace of technology development, miniaturisation, and high-density packaging is presenting new opportunities, but with them come challenges involving traceability and quality control—both of which heavily rely upon control standards.

One of the best forums for evolving such documents is IPC, which is headquartered in the U.S. and has historically been heavily influenced by the demands of the U.S. aerospace and defence sector since the removal of "MIL" standards during the Reagan administration back in the '80s. However, a major criticism is the pace by which standards are developed and for which five-year timescales are a problem. This time lag with the actual technology used in high-volume products is problematic. Moreover, the military and high-reliability industries are late adopters, further delaying the start of work on standards for current products. Another, and perhaps more significant, problem is that the development work has been done by volunteers, albeit on behalf of their employers.

With increasing frequency, standardising the standards, such as ISO 9201, imposes certain rules that must be met to ensure "fair play" amongst the supply chain. There will be those familiar with hearing about "false positives/negatives" and "never trust the salesman," so mitigating these is no easy task. However, there is the chance for each 5-30 Task Group to review industry requirements and set out the work program for the ensuing period.

With that in mind, much of what follows is based on comments we learn about from our industry around the world, many of whom are not yet IPC members. Yes, this is a membership recruitment drive, unashamedly, as well as a search for volunteers willing to help create the standards of tomorrow.

IPC Task Group 5-32b SIR and ECM: Structured Development Programme

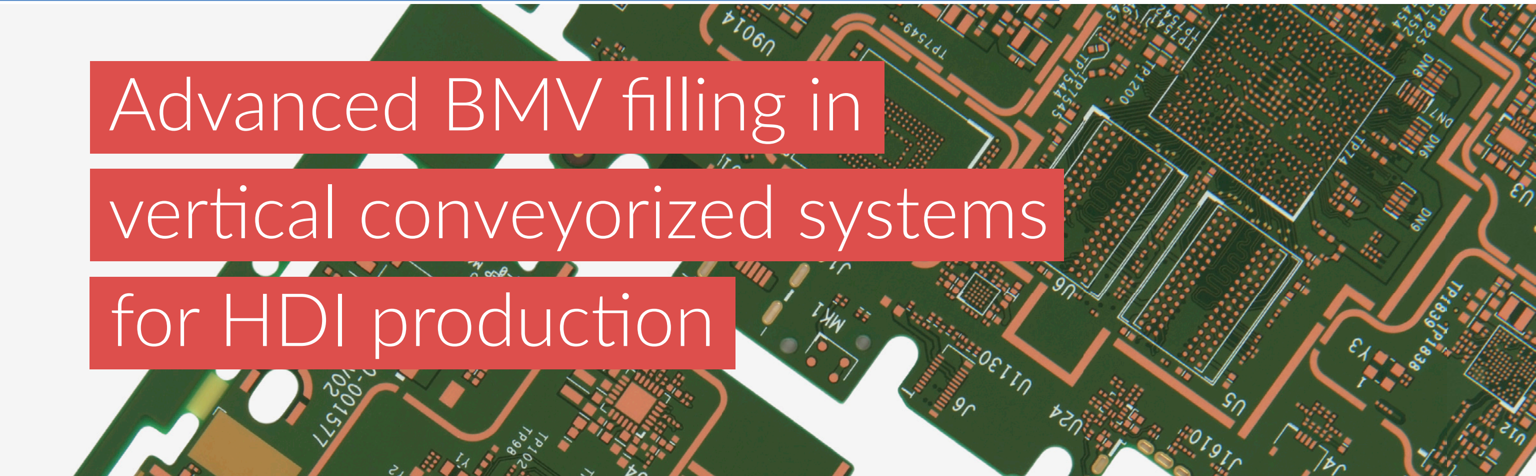
Background

The current IPC SIR 2.6.3.7 test is targeted at typical applications, which is where the minimum PCB feature is separated by more than 200 µm and the voltage is within the approximate range of 10–100 V. The test dura-

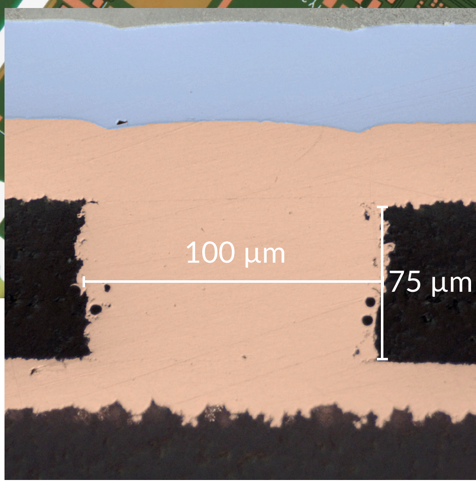
InPro® MVF2

Advanced HDI BMV filling

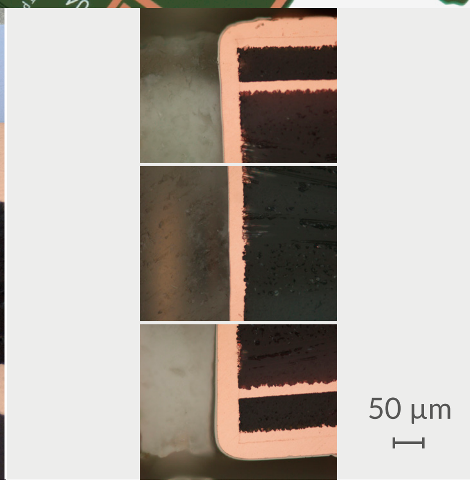
ATOTECH



Advanced BMV filling in vertical conveyorized systems for HDI production



BMV filling with dimple < 5 µm and surface copper 12 µm



Over 70% throwing power in through holes with AR 6.4:1

2

A/dm² applicable current density

12

µm plated copper necessary for BMV filling (100×75 µm)

Our next generation filling process is designed for vertical conveyorised systems with insoluble anodes. It offers much improved filling performance and a wider working window compared to older generation products. By filling at lower surface thickness InPro® MVF2 enables cost saving potential and allows for finer resolution. The new process is applicable for next generation HDI BMV filling and also for half-filling in Flex application.

Atotech Group
+49 30 349850
info@atotech.com

tion states not less than 72 hours by committee agreement. This was to revert to 168 hours, but evidence is now available that flux residues may lie dormant for beyond 500 hours in service, and hence there is a need for a three-week or four-week test.

Today, there are two different developing technology regimes: (1) high voltage (~1,000 V) electronics for electric vehicles and (2) low voltages and fine-pitch devices (~2 V and <100-µm feature size) in the medical and space industries. The existing test 2.6.3.7 is not appropriate for these technologies. For example, in the high-voltage testing standard ISO PAS 19295:2016(E), electric components or circuits are required to operate with a maximum working voltage between 30 V AC (rms) and 1,000 V AC (rms) or between 60 V DC and 1,500 V DC.

An impetus for a new test has been created by the removal of the ROSE test from Rev G of J-STD-001. There is a desire to qualify cleaning efficacy underneath bottom terminated components (BTC), using a modified SIR test, along with a new test vehicle, that can take advantage of low-cost test vehicles and use SIR patterns underneath the BTC to evaluate cleaning efficacy.

Following on from a current HDPUG project on corrosion, a method will be produced to look at pitting and crevice corrosion through solder mask. Here a modification of the SIR technique is proposed to evaluate solder mask integrity and use a new test vehicle.

Aim

The aim here is to develop new SIR standards to cover the low and very high voltages, and validate the developed approach with a Gauge R&R study, all under the auspices of IPC. The work will build on the approach in 2.6.3.7 but will tailor the approach appropriately for the two technology areas. 2.6.3.7 will also be updated from the current 2007 version, and incorporation of the new IPC B53 test pattern, which incorporates a 200-µm SIR pitch pattern. The new standard will also look at test duration, which will include a minimum of one option to test for at least 500 hours and possibly beyond 1,000 hours.

The cleaning efficacy SIR evaluation, and the corrosion of solder masks, will follow a similar path, with the development of test vehicles, dummy components, and a test protocol. The IPC SIR committee 5-32b will lead the development of the documents and organise a round robin trial with Gauge R&R validation.

Funding

The standards will be written as now within 5-32b by voluntary work. Production of the samples might be funded by IPC, and then the intercomparison work by the collaborators will take place at their expense.

Methodology

For these, we need a consensus on the track and gap for the patterns. Our current point is 25 V/mm, with the 200-µm (B53) and 500-µm (B24) patterns. For low-voltage applications, it is envisaged that the test voltage of 2V and ~50-µm track spacing, and this will lead to 40 V/mm. With high-voltage testing, an anticipated field strength of 500 V/mm is expected, hence with a 1,000 V test, the feature spacing will be 1 mm.

It has been demonstrated that electrochemical processes will not always scale with feature size, or SIR pattern pitch, and the applied voltage. Thus, careful consideration must be given to the applied test, and the conditions of the test must be applicable to the use case. If not, the produced data can be valueless. Therefore, new test coupons will be required, and the input from the wider industry is essential to define the requirements.

New material systems are known to have a long incubation period before the onset of corrosion; periods of up to 500 hours have been noted. Testing at >1,000 V may generate failure modes that occur over relatively long distances and hence may take even longer times, and test durations of over 1,000 hours may be required. Proposals for the cleaning efficacy SIR evaluation and the corrosion of solder masks will be brought forward.

Validation

When the committee has agreed on the test methodology, the method and chosen test ve-

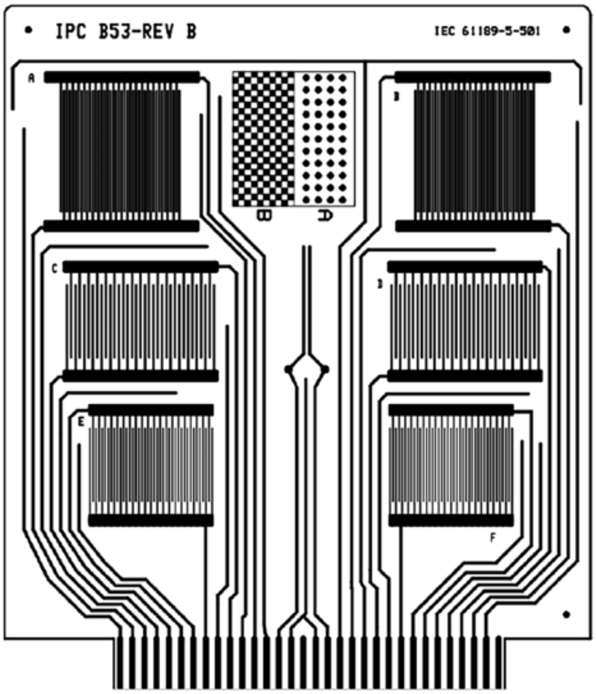


Figure 1: IPC B53 Rev B.

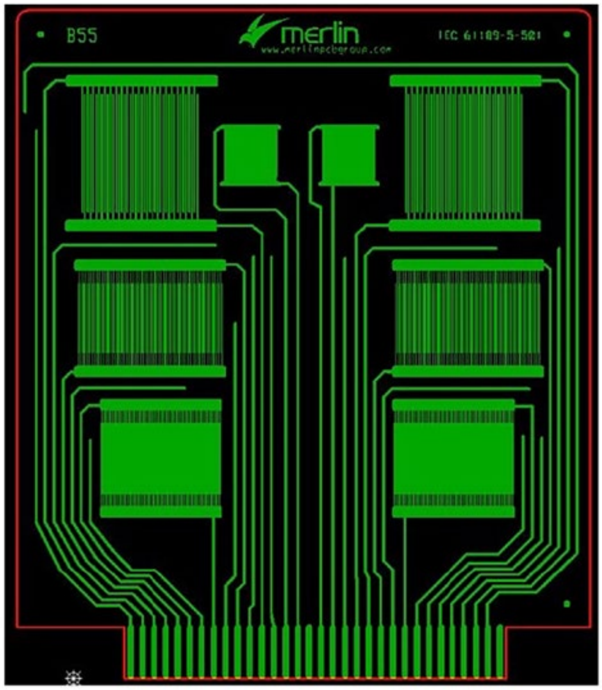


Figure 2: Proposed IPC B55.

hicles need to be validated. Previously an intercomparison was organised jointly by IPC and the IEC, and the results were reported and published as IEC TR 61189-5-506. This report compared the response using SIR patterns with 500-µm, 318-µm, and 200-µm conductor separation. The test coupon used for this was IPC B53 Rev A. These results are now an important part of the updating of 2.6.3.7. The development work described here plans a similar exercise with the to-be-developed standards and test vehicles.

Work has already started, and there is a Rev B to IPC B53—the development of which was intended as a potential replacement for IPC B24, B25, and B25A coupons. A further refinement of the B53 to the B55 has also been designed, which contains an extra pair of patterns with 50-µm spacing. Both of these new boards are shown in Figures 1 and 2.

The plan is to start this work soon and produce the necessary draft standards and test vehicles.

We feel that the broader industry needs to be aware of this work and help in the development of the next revision of the SIR/ECM standard that includes:

- IPC-TM-650 Method 2.6.3.7
- IPC 9201 Surface Insulation Resistance Handbook
- IPC 9202 Material and Process Characterization/Qualification Test Protocol for Assessing Electrochemical Performance
- IPC 9203 Users Guide to IPC-9202 and the IPC-B-52 Standard Test Vehicle

A new test method for process characterisation and a toolbox of other test methods can assist in evaluating and resolving test failures. **PCB007**

Graham Naisbitt is the chairman and CEO of Gen3 Systems, as well as the chair of IPC 5-32b SIR/ECM, vice-chair of the IPC 5-30 Cleaning and Coating Committee, and vice-chair of 5-32e CAF. He is also the author of *The Printed Circuit Assembler's Guide to...Process Validation*. Visit I-007eBooks.com to download this book and other free, educational titles.


PRINT ON DEMAND
ORDER NOW
Automation and Advanced Procedures in PCB Fabrication
Happy Holden
DOWNLOAD NOW
I-007e Books
I-007eBooks.com/automation

Editor Picks from PCB007

1 Punching Out! Are We Selling a Business or Watching 'Die Hard'? ▸


Tom Kastner

According to Wikipedia, the movie series "Die Hard" is about "a police detective who continually finds himself in the middle of violent crises and intrigues where he is the only hope against disaster." Tom Kastner explains how if you use the "strong or powerful" definition of "violent," that pretty much describes many M&A deals.

2 Real Time with...SMTAI 2020: ASC Makes Lemonade Out of Lemons ▸

Steve Williams and Anaya Vardya, president and CEO of American Standard Circuits (ASC), discuss the upcoming virtual SMTAI show and how the company is "making lemonade out of lemons." Anaya explains how the COVID-19 lockdown has caused ASC to become more creative in its marketing efforts, including holding webinars and publishing two eBooks with I-Connect007.

3 The Government Circuit: Green Regulations, the Economy, COVID-19, and 'Decoupling' in Focus for IPC This Fall ▸


Chris Mitchell

Summer may be winding down, but autumn is shaping up to be a busy advocacy season for IPC. In this month's column, Chris Mitchell provides an overview of the latest worldwide regulations you should be attuned to, the global economic landscape, and opportunities to make your voice heard with policymakers.

4 Just Ask John Mitchell: Are IPC's Positions Dictated by Politics? ▸


John Mitchell

First, we asked you to send in your questions for Happy Holden, Joe Fjelstad, and Eric Camden in our "Just Ask" series. Now, it's IPC President and CEO John Mitchell's turn! Over the years, he has served as an engineer, manager, and executive at a variety of companies and organizations.

5 Catching up With Nate Doemling, New CEO of IMS


Nate Doemling

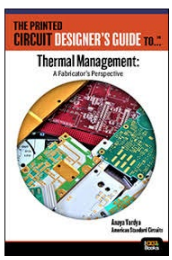
Dan Beaulieu recently interviewed Nate Doemling with Intelligent Manufacturing Solutions (IMS) in New England about his new role at the company. After serving on the IMS board of directors for several months, Doemling joined the company as CEO in January 2020.

6 It's Only Common Sense: Sales Leaders—Are You Ready for the Future?


Dan Beaulieu

Besides all the hardships we have faced this year, there will come many changes in not only the way we lead our life but also the way we do business. Here, Dan Beaulieu shares seven things sales leaders must do going forward.

8 An Excerpt From the Book *'Thermal Management: A Fabricator's Perspective'*



Thermal management in the printed circuit board world is big business! A recent Markets and Markets report projects the thermal management market to reach $16 billion by the year 2024, with an average CAGR of 8% over that period. We have chosen to focus this book on providing designers a thermal management desk reference on the most current thermal management techniques and methods from a PCB fabrication perspective.

7 Board Shark PCB Enters the U.S. Southwest Market with ARK Manufacturing


Dabe Murrin

Board Shark PCB, a PCB solution provider, announced a new partnership with ARK Manufacturing Solutions LLC. Dave Murrin, president and principal owner of ARK Manufacturing, will help Board Shark PCB expand its customer base in New Mexico, Arizona, and Southern Nevada.

9 Hitachi High-Tech Launches EA1400 RoHS Analyzer for Hazardous Substance Control

Hitachi High-Tech Analytical Science launches the EA1400 RoHS analyzer for hazardous substance control. Designed to play a key role in manufacturing facilities, this latest analyzer for hazardous substances has been developed to meet the latest directives.

10 Ventec Strengthens Growing U.S. and Mexican Market with New Sales Representative

Ventec International Group Co. Ltd. has announced the appointment of Spectrum Marketing Associates based in Arizona, U.S., to provide sales and support to customers in the U.S.-West Coast region and Mexico.

For the Latest PCB News and Information, Visit: PCB007.com

Career Opportunities

CIRCUIT FOIL

US Sales Manager

THE ROLE:

- To promote, sell and secure orders from existing and prospective customers in North America (USA, mainly, and Canada)
- To provide administrative help to our CFT Inc office in Glenside, PA
- To demonstrate our products to existing and potential customers and to assist them in selecting the copper treatments best suited for their needs
- To provide technical assistance to customers in case of claims, technical assistance, new product development
- To promote our products to OEMs
- To attend fairs (IPC, DesignCon,...), technical conferences (IPC 4562A,...) and customer presentations

THE PROFILE:

- Master's degree in engineering, with experience in technical sales
- At least 5 years of relevant experience in similar position
- PCB sales experience an advantage
- Very good knowledge of all product/services and international market regulations
- Knowledge of financial indicators
- Ability to work under pressure in order to meet deadlines
- Good organizational, planning, analytic, negotiation, presentation and people-management skills

We offer a permanent contract based on full-time presence as well as good salary conditions in an international environment. Curriculum vitae in English and French with application letter should be addressed to:

HR Department • Circuit Foil Luxembourg

jobs@circuitfoil.com

apply now

FTG

Chemical Process Engineer
Fredericksburg, VA

Scope:

Responsible for implementation and maintenance of chemical processes used to manufacture printed circuit boards.

Responsibilities:

- Research availability of chemical processes
- Write plan for process implementation
- Implement process and perform failure mode analysis to establish correct operating conditions
- Write all necessary procedures and instructions for process operation, maintenance and safety
- Monitor process operation on a daily basis to ensure consistency
- Perform failure and root cause analysis when product/process problems occur
- Perform chemical analyses on processes when required

Knowledge and Skills:

- Ability to read, write and communicate in English necessary to perform the job
- Knowledge and application of statistical techniques for process control
- Knowledge and application of failure mode effect analysis techniques as applied to process improvement and process development
- Ability to lift 25 pounds
- Will be exposed to hazardous waste while performing daily job duties
- Will undergo chemical handling training prior to start and will actively participate in ongoing hazardous waste and chemical handling training

Education and Experience:

- Bachelor of Science degree in chemical engineering or equivalent
- Must have general knowledge of methods used to train people in the operation and theory of the processes they operate

Salary negotiable and dependent on experience.
Full benefits package.

lisabradley@ftgcorp.com

apply now

Career Opportunities

Career Opportunities

Manncorp

SMT Operator
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for a **surface-mount technology (SMT) operator** to join their growing team in Hatboro, PA!

The **SMT operator** will be part of a collaborative team and operate the latest Manncorp equipment in our brand-new demonstration center.

Duties and Responsibilities:
- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities
- Some mechanical assembly of lighting fixtures
- Assist Manncorp sales with customer demos

Requirements and Qualifications:
- Prior experience with SMT equipment or equivalent technical degree preferred; will consider recent graduates or those new to the industry
- Windows computer knowledge required
- Strong mechanical and electrical troubleshooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
- Ability to work with minimal supervision
- Ability to lift up to 50 lbs. repetitively

We Offer:
- Competitive pay
- Medical and dental insurance
- Retirement fund matching
- Continued training as the industry develops

apply now

ventec INTERNATIONAL GROUP 騰輝電子

Customer Service Rep.
Near Chicago, USA

We have a great opportunity at Ventec's Elk Grove Village facility to join our customer services team as a customer service representative (CSR) to act as a customer liaison, manage incoming orders, order entry into ERP system, provide product/services information, and resolve any emerging problems that our customer accounts might face with accuracy and efficiency. As a CSR, you will provide a two-way channel of technical communication between Ventec's global manufacturing facilities and North American customers to ensure excellent service standards, efficient customer inquiry response, and consistent highest customer satisfaction.

Skills and abilities required for the role:
- Proven B2B customer support experience or experience as a client service representative
- Strong skill set in Excel, Word, and Outlook for effective communication
- Strong phone contact handling skills and active listening
- Customer orientation and ability to adapt/respond to different types of characters
- Excellent communication and presentation skills
- Ability to multi-task, prioritize, and manage time effectively
- High-school degree

What's on Offer:
- Excellent salary & benefits commensurate with experience

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits.

Please forward your resume to jpattie@ventec-usa.com and mention **"Customer Service Representative—Chicago"** in the subject line.

apply now

Career Opportunities

MivaTek Global

MivaTek Global: We Are Growing!

MivaTek Global is adding sales, technical support and application engineers.

Join a team that brings new imaging technologies to circuit fabrication and microelectronics. Applicants should have direct experience in direct imaging applications, complex machine repair and/or customer support for the printed circuit board or microelectronic markets.

Positions typically require regional and/or air travel. Full time and/or contractor positions are available.

Contact HR@MivaTek.Global for additional information.

apply now

BÜRKLE NORTH AMERICA, INC.

Service Engineer

Schmoll Laser Drilling and Direct Imaging

Burkle North America seeks a full-time service engineer in the Northeastern U.S. This position will provide expert-level service on multiple laser drilling and direct imaging product lines. Install, commission, and maintain Schmoll products at multiple customer sites across the Northeast. The candidate will perform modifications and retrofits as needed. Maintain complete and detailed knowledge of Schmoll products and applications and handle a wide variety of problems, issues, and inquiries to provide the highest level of customer satisfaction. Assist customers with the potential optimization of their machine functions and work with clients on application improvements.

Qualifications

Required: Bachelor's degree from a technical college/university in an associated field. Three years directly related experience, or equivalent combination of education and experience. Must possess a valid driver's license and have a clean driving record.

Preferred: Experience in control systems and electronic troubleshooting, as well as in general electrical and mechanical service tasks. Experience and knowledge in the PCB manufacturing process, with a focus on laser drilling and/or direct imaging.

Send resume to hr@burkleamerica.com.

apply now

Career Opportunities

LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®

Sales Account Manager

Sales Account Management at Lenthor Engineering is a direct sales position responsible for creating and growing a base of customers that purchase flexible and rigid flexible printed circuits. The account manager is in charge of finding customers, qualifying the customer to Lenthor Engineering and promoting Lenthor Engineering's capabilities to the customer. Leads are sometimes referred to the account manager from marketing resources including trade shows, advertising, industry referrals and website hits. Experience with military printed circuit boards (PCBs) is a definite plus.

Responsibilities

- Marketing research to identify target customers
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
  - Market and product
  - Circuit types used
  - Competitive influences
  - Philosophies and finance
  - Quoting and closing orders
  - Providing ongoing service to the customer
  - Develop long-term customer strategies to increase business

Qualifications

- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is a leader in flex and rigid-flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

apply now

LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®

Senior Process Engineer

Job Description

Responsible for developing and optimizing Lenthor's manufacturing processes from start up to implementation, reducing cost, improving sustainability and continuous improvement.

Position Duties

- Senior process engineer's role is to monitor process performance through tracking and enhance through continuous improvement initiatives. Process engineer implements continuous improvement programs to drive up yields.
- Participate in the evaluation of processes, new equipment, facility improvements and procedures.
- Improve process capability, yields, costs and production volume while maintaining safety and improving quality standards.
- Work with customers in developing cost-effective production processes.
- Engage suppliers in quality improvements and process control issues as required.
- Generate process control plan for manufacturing processes, and identify opportunities for capability or process improvement.
- Participate in FMEA activities as required.
- Create detailed plans for IQ, OQ, PQ and maintain validated status as required.
- Participate in existing change control mechanisms such as ECOs and PCRs.
- Perform defect reduction analysis and activities.

Qualifications

- BS degree in engineering
- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is the leader in Flex and Rigid-Flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

apply now

Career Opportunities

Manncorp™

SMT Field Technician
Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:
- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:
- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:
- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

apply now

U.S.C. U.S. CIRCUIT

Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:
- Candidates must have previous PCB sales experience.

Compensation:
- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

apply now

Career Opportunities

BLACKFOX
Premier Training & Certification

IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

apply now

YOUR JOB AD HERE

For information, please contact:
BARB HOCKADAY
barb@iconnect007.com
+1 916.365.1727 (PACIFIC)

I-Connect007
GOOD FOR THE INDUSTRY

Professionals Seeking Employment

D.B. Management Group L.L.C. is currently working with many professionals who are seeking new positions. If any of these qualified professionals sounds like someone you would like to learn more about, contact **Dan Beaulieu** at **207-649-0879** or **danbbeaulieu@aol.com.** If you are a qualified professional looking for a new opportunity, contact Dan as well. Fees are 10% of candidates' first year's annual compensation. There is no fee for candidates.

Click here to learn more ▶

President, Company Leader, Business Builder
This professional has done it all. Built new businesses and turned around hurting businesses and made them successful. A proven record of success. This candidate is a game-changer for any company. He is seeking a full-time leadership position in a PCB or PCBA company.

General Manager PCB and PCBA
Senior manager with experience in operations and sales. He has overseen a number of successful operations in Canada. Very strong candidate and has experience in all aspects of PCB operations. He is looking for a new full-time position in Canada.

Regional Sales Manager/Business Development
Strong relationship management skills. Sales experience focused on defense-aerospace, medical, high-tech PCB sales. Specializes in technical sales. Also has experience in quality, engineering, and manufacturing of PCBs. He is looking for a fulltime position in the Southeastern U.S.

Field Application Engineer (FAE)
Has worked as a respected FAE in the U.S. for global companies. Specializes in working alongside sales teams. Large experience base within the interconnect industry. He is looking for a full-time position.

Business Development Manager
Understands all aspects of interconnect technical sales from PCB design and fabrication to assembly and all technologies from HDI microvias to flex and rigid-flex. Has also sold high-tech laminates and equipment. Proven record of sales success. He is looking for a full-time position.

CEO/President
Specializes in running multimillion-dollar companies offering engineering, design, and manufacturing services. Proven leader. Supply chain manager. Expert at developing and implementing company strategy. Looking to lead a company into the future. He is looking for a full-time position.

PCB General Manager
Forty years of experience serving in all capacities, from GM to engineering manager to quality manager. Worked with both domestic and global companies. Available for turn-around or special engineering projects. He is looking for long-term project work.

Process Engineering Specialist
Strong history of new product introduction (NPI) manufacturing engineering experience: PCB/PCBA. Held numerous senior engineering management positions. Leads the industry in DFM/DFA and DFX (test) disciplines. He is looking for either a full-time position or project work.

VP Sales Global Printed Circuits
Worked with a very large, global company for a number of years. Built and managed international sales teams. Created sales strategies and communicated them to the team. One of the best sales leaders in our industry. He is looking for a full-time position.

Plant Manager
This professional has years of experience running PCBA companies. Led his companies with creative and innovative leaderships skills. Is a collaborative, hands-on leader. He is looking for a full-time position.

National Sales Manager
Seasoned professional has spent the past 20 years building and growing American sales teams for both global and domestic companies. Specializes in building and managing rep networks. He is looking for a full-time position.

Global Engineering Manager/Quality Manager
Has experience working with large, global PCB companies managing both engineering and quality staff. Very experienced in chemical controls. She is interested in working on a project-by-project basis.

CAM Operators and Front-end Engineers
These candidates want to work remotely from their home offices and are willing to do full-time or part-time projects.

MANAGING EDITOR: **NOLAN JOHNSON**
(503) 597-8037; nolan@iconnect007.com

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

SALES: **ANGELA ALEXANDER**
(408) 489-8389; angela@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

CONTRIBUTING EDITOR: **PATRICIA GOLDMAN**
(724) 299-8633; patty@iconnect007.com

CONTRIBUTING TECHNICAL EDITOR: **DAN FEINBERG**
baer@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

ASSOCIATE EDITOR: **KIERSTEN ROHDE**
kiersten@iconnect007.com

ASSOCIATE EDITOR: **MICHELLE TE**
michelle@iconnect007.com

CONTRIBUTING TECHNICAL EDITOR: **HAPPY HOLDEN**
(616) 741-9213; happy@iconnect007.com

PRODUCTION MANAGER: **SHELLY STEIN**
shelly@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA, TOBEY MARSICOVETERE**

CREATIVE TECHNOLOGIST: **BRYSON MATTIES**

COVER: **SHELLY STEIN**

COVER IMAGE: **FRESHIDEA**

PCB007 MAGAZINE

PCB007 MAGAZINE®
is published by BR Publishing, Inc.,
942 Windemere Dr. NW, Salem, OR 97304

October 2020, Volume 10, Number 10
PCB007 MAGAZINE is published monthly,
by BR Publishing, Inc.

ADVERTISER INDEX