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Fine Pitch

While this issue may be about finer pitches in manufacturing and packaging, to successfully manufacture circuit boards in this time of shrinking components and board features, the secret is to ensure success with the solder joints. Manufacturers will need the tools, options, and human expertise to succeed at this level.

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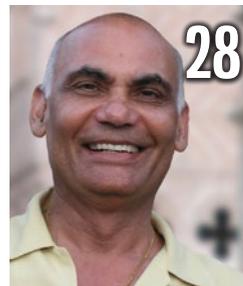
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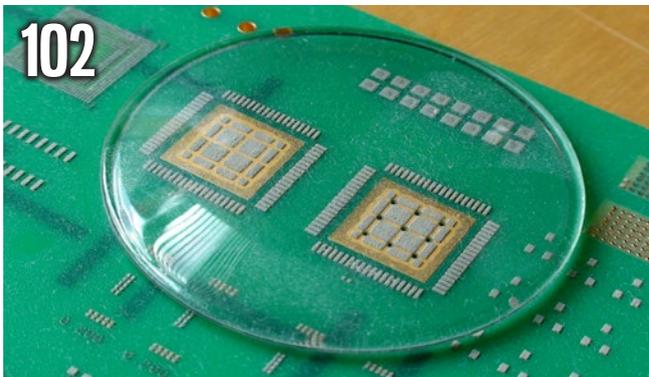
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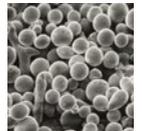


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Fine Pitch

Nolan's Notes

by Nolan Johnson, I-CONNECT007

As much as I'd like to report on baseball, based on our cover, that's not what we're addressing this month. For those of us who do follow the American major leagues, however, baseball season begins with spring training. Sure, the regular season is what counts, but it all begins in Florida or Arizona every February. The first players to report to spring training camp are the pitchers and catchers. This year, the day to report is February 12. Position players, of course, report on February 17, give-or-take. Why does the pitching staff show up early? Because pitching is a precise business.

It's no surprise, then, that this issue targets finer pitches in manufacturing and packag-

ing in our industry. We dove into the dynamics driving smaller components and finer dimensions in board fabrication. This led us to some interesting interrelationships. The dynamics—smaller component packages, courtesy of ever-shrinking semiconductor processes, which lead to smaller pitches between pads and more pads per package—allow boards to be packed more densely with very small devices.

In baseball, there are three basic pitches: fastballs (five separate grips), breaking balls (four grips), and changeups (three grips). Throw in the infamous “knuckleball,” and that pretty much covers all the legal, practical pitches in professional baseball. The pitcher's ability to



succeed in their job—giving the opposing team the opportunity to put the ball into play while simultaneously denying the opponents that very chance—depends on the use of all the options at their disposal.

We've made this point multiple times in this publication: automotive and medical electronics applications are demanding very high-volume production at two orders of magnitude greater reliability than is the current industry benchmark. Fabricators will need the tools, options, and human expertise to succeed at this level. So, where's the real pain point, where things are stressed enough to break?

The different grips the pitcher uses on the ball make the ball perform as they intend. If one deconstructs the grip, one realizes that the grip is all about fingers and knuckles. Any major league pitcher will tell you that it doesn't matter how good the rest of their mechanics are; it's their grip with their finger joints that makes the ball come to life on its way to the plate.

Success, as a pitcher, has much to do with controlling the joints, and that's what we found, too. To manufacture circuit boards in this time of shrinking components and board features, the secret is to ensure success with the solder joints. Of course, it's not lost on any of us that some landing pads are intentionally shaped like a baseball home plate. The parallels are never-ending.

Throwing the first pitch, so to speak, are Dana Korf and Chuck Bauer. The I-Connect007 team, along with Bauer and Korf, talked in-depth on the topic of finer pitches and the consequences on the industry, in "Semiconductors in Charge: The Changing Face of Board Manufacturing." Next, Brent Fischthal shares the inspection perspective in "What's Driving AOI Innovations and Collaboration?" Ray Prasad talks with the I-Connect007 team about market drivers in "The Big Picture on Small Components," Joe Fjellstad highlights "Solder in PCBA: Can't Live Without It... Or Can We?" and Jeff Schake addresses solder paste printing from the stencil's perspective.

Eric Camden bats lead-off for the columnists in this issue with "Big Trouble Comes in Tiny Packages." Then, we talk to Stephan Schmidt and Mirela Orlowski of LPKF about the challenges they face cutting those very stencils for IIT and companies like them.

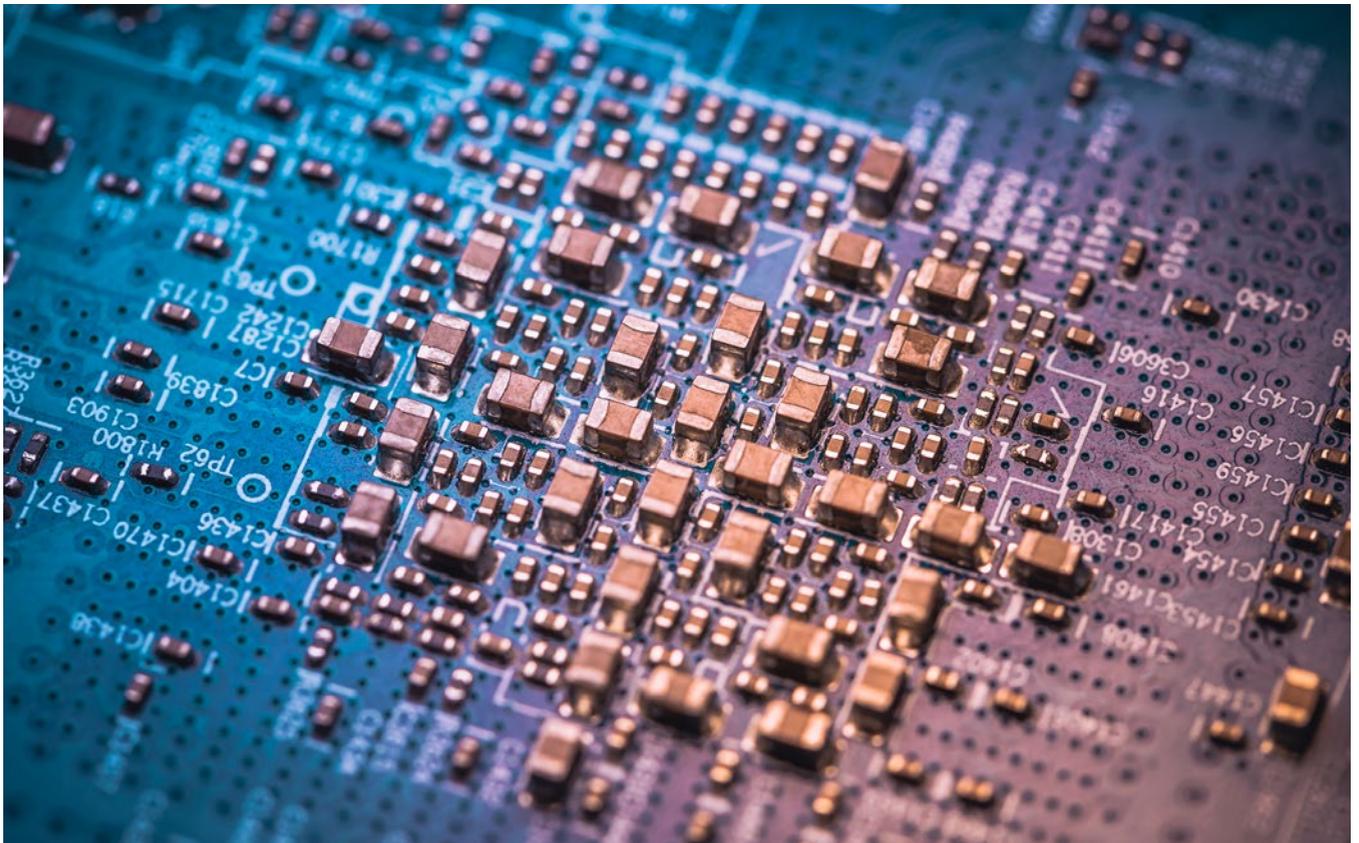
Michael Ford's column considers the digital side of things in "Size Matters: The Digital Twin." Then we turn to Taiyo's Yuya Suzuki to talk solder mask. In our conversation, "Evolving Solder Capabilities for Shrinking Components," Suzuki discusses Taiyo's efforts to endure ever increasing precision with solder mask, including—but not limited to—creating a planar surface for the stencil. Having discussed solder mask, we complete the cycle with a conversation with Indium Corporation's Chris Nash to talk solder paste itself. Ray Prasad returns this month with his column "Dealing With Package Parasitics."

Just about where the seventh inning stretch should be, we visit with Epoch's Foad Ghalili in "Market Insights From Epoch International's President." Then, we swing back to technical topics with Vern Solberg's piece "Embedding Semiconductors." Alfred Macha's column encourages "Sharpening Your Organization's Competencies," which is good advice, as the products we build get more precise. We also feature a piece by Pete Starkey on Bob Willis's webinar in "Solder Paste Evaluation and Simple Tricks of the Trade."

What is clear is that whether it's fine pitching on the diamond or fine pitch on the manufacturing floor, it takes all team members doing their part to succeed. As you follow along with your favorite team this spring, we invite you to consider all the information we've gathered on fine pitch components and fabrication processes. **SMT007**



Nolan Johnson is managing editor of *SMT007 Magazine*. Nolan brings 30 years of career experience focused almost entirely on electronics design and manufacturing. To contact Johnson, [click here](#).



Semiconductors in Charge: The **Changing Face** of PCB Manufacturing

Feature Interview by the I-Connect007
Editorial Team

The I-Connect007 editorial team recently spoke with Chuck Bauer and Dana Korf in a technical discussion that spanned a number of topics around shrinking components, such as redistribution layers (RDLs), active embeds, and why even the most revolutionary technologies must show ROI to be successful.

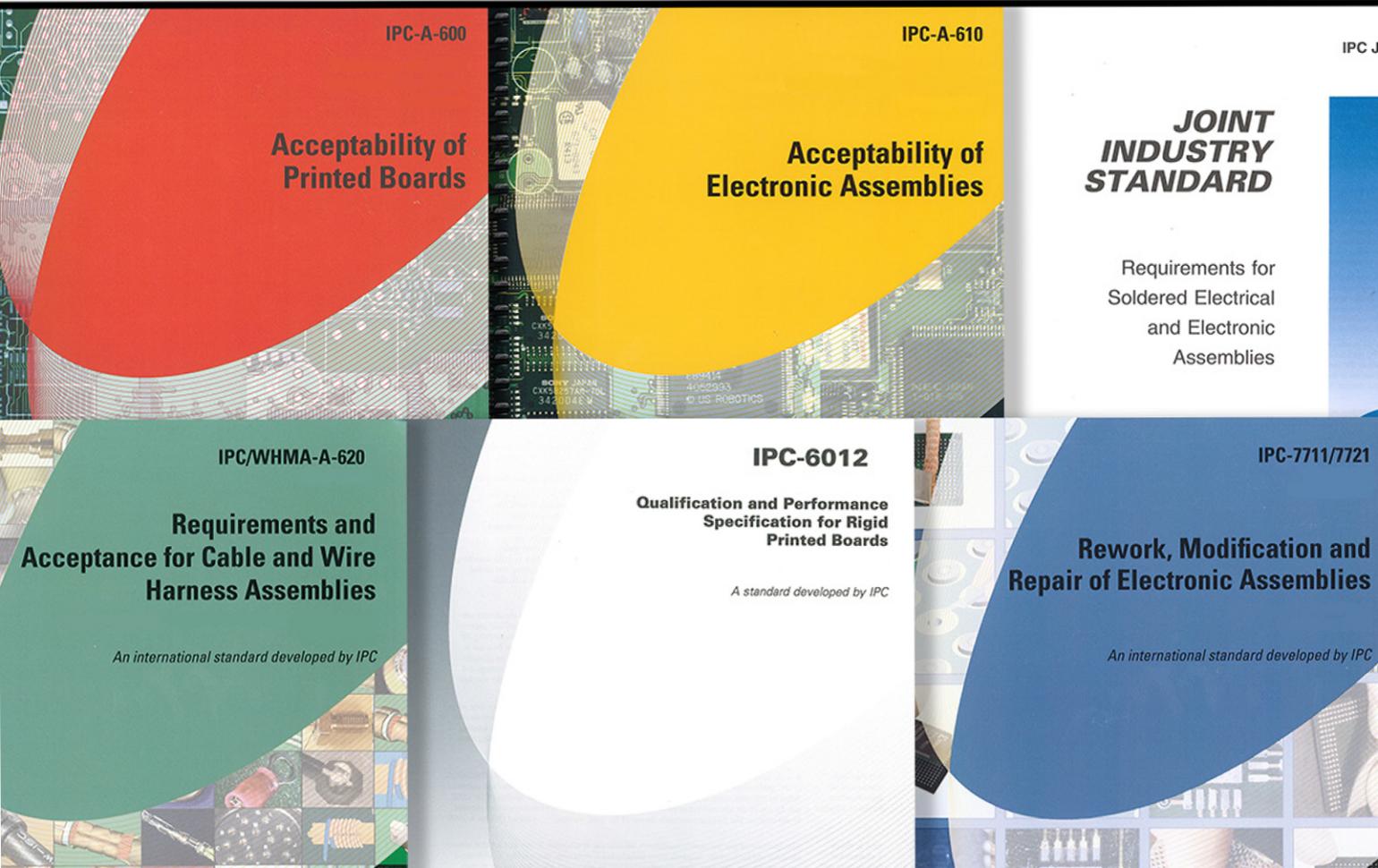
Nolan Johnson: Thanks for joining us. There is a miniaturization and design constraint shift going on as a result of increased densities and shrinking board sizes that also seems to be pushing on the component supply chain. It's not entirely clear to me whether components are driving board design shrinks or whether

shrinking board size is driving component miniaturization. Let's start with you, Chuck.

Chuck Bauer: It is kind of difficult; I haven't thought about it a lot from that perspective. In general, we all know that the primary custom component of the product is the PCB. Most of the other components are pretty much standardized. But even though the PCB may not be a major piece of the bottom line cost, it is generally the only fully custom component in the product other than some of the external design functions.

Packaging capability is driving toward miniaturization, primarily for two reasons. There's a moderate impact on the cost by miniaturizing the package, but there's a more significant impact on the cost by miniaturizing the board.

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The components drive the miniaturization from a technology standpoint, and the boards drive miniaturization from a cost standpoint.

Happy Holden: Yes, but what's the drive toward wafer-level packaging? Is it to get away from having to buy a separate component that gets assembled flip-chip-wise or something like that? From what we've been following from the ECTC conference, the wafer-level packaging sessions keep growing and growing.

Bauer: The trends in wafer-level packaging are driven almost entirely by cost. The technology for doing it is like anything else; if you can minimize the cost, you're going to have an opportunity to either capture market share by reducing pricing or increasing margins. Cost is always the driver.

Holden: There seems to be a major push into the electronic panel level, wafer column plating, and other finishes for a level of assembly automation that includes embedded actives in the semiconductor package.



Chuck Bauer

Holden: They deal with integrating active chips that get embedded in the package, and die may also go on the surface, but now the actives are embedded. They supply plating and other kinds of automation for this level of integration that's growing, especially in Asia, as an alternative to 3D packaging or 2.5D packaging. Wafer-level packaging has been going for a long while but still continues to grow. If it's

wafer-level packaging, then that's the device that gets soldered onto the PCB at assembly. It doesn't go through another packaging step. It comes from the wafer and is now a component that's going to be assembled on the finished board. Is that only for the smaller number of leads? How big does wafer-level packaging go in terms of what it attempts to connect?

Bauer: To my knowledge, nobody's using wafer-level packaging to do microprocessors or large memories either. If you go to very high I/O, you still don't find it there.

Johnson: Why do you suppose that is?

Dana Korf: It's yield. When you get so many devices put together in a package like that, for many years, that has been known as the "known good die" problem. You put a bunch of die together, or you glob them up. One's bad, so what do you do? You throw the whole thing away. You have to know those devices are good as well as the interconnect or you throw away a lot of money for a single interconnect problem. This tends to be the problem.

Bauer: I'm going to throw out a couple of somewhat controversial ideas. We've talked about trying to focus on miniaturization, particularly 5G and high-performance technology, as well as those that will be critical for communications, autonomous driving, IoT, etc. What we're very likely to find is something that the folks at Panasonic discovered back in the early

Wafer-level Packaging

Bauer: If you look at it from the device perspective, the memory and RF companies in particular have always had embedded passives on their chips. One of the biggest issues for the RF companies, especially, has been if you come up with a low-cost, silicon-integrated passive, the chip size for a GaAs chip goes down by an order of magnitude. Thus, the capacity for GaAs devices immediately goes up by an order of magnitude, and the pricing goes in the toilet because there's suddenly a huge overcapacity. The gallium arsenide companies continually fight against integrated passives for this reason.

to mid-1990s. When you get small enough, the cost of using a ceramic substrate instead of a PCB becomes very competitive. Many people are jumping on the IoT and 5G bandwagon for these tiny devices or key chains, and I use “key chain” as an expression of size, not of the technology or application.

When you’re talking about end products that are the size of a key chain or a flash drive, this question is going to come:

Do we need PCBs anymore for those kinds of devices? I don’t know the answer because it seems to me that with wafer-level packaging, the wafer-level package could be the product when we get to that point, in many cases. The wafer-level package doesn’t have to have a single device in it; it can have 2–5 devices in it in an area that’s no more than a centimeter or so on a side. At that level, the issues that you resolve in terms of reliability and the complexity of the interconnects that are required are greatly simplified, and ceramic becomes very competitive with PCBs at that level.

Matties: Is wafer-level packaging also much better for thermal situations?

Bauer: If the dielectric constant is better for things like the very high frequencies that we’re going to need for 5G, then the thermal management becomes less of an issue. When you’re processing a maximum of an 8x8 substrate to make these things with ceramic, all of a sudden, the geometries are competitive with what a PCB shop can do on an 18x24 inch panel. When you automate the technology, the costs make it very competitive. My point is that it’s not all doom and gloom for PCBs, but a lot of those products are going to be looking at that kind of trade-off. They may very well find that for many of those tiny products ceramics make more sense.

On the other hand, there might be a way to use RDLs in a multi-chip, wafer-level package. If you do that, that’s how you’re going to compete with something like a ceramic sub-



Dana Korf

strate because you eliminate an assembly issue. The challenge there, again, is going to be about yield. If you’re going to use a multi-chip, wafer-level packaging approach, then you have to make sure that you get very high yields; otherwise, you’re not going to be competitive. At the other end of the spectrum, where you’re not going to that level of miniaturization at the product level, you still miniaturize the configuration of the product, but you have a product that’s much larger.

Even with a couple of inches on a side, the PCB suddenly becomes far more capable. The ability to use RDLs on top of a PCB, for example, makes more sense and allows you to get to that point. The barrier to all of that is going to come down to power supply. It’s not going to be signal and connecting the circuits because those kinds of devices are not going to be super complex. The complexity will be buried in the chip, so the issue is going to be how to get the cost down along with the size and maintain the simplicity. PCBs have an advantage there, so there’s going to be a size trade-off when you look at those cost comparisons. Again, cost is going to drive it all.

RDL and Shrinking Die Sizes

Holden: A term that seems to have come back is RDL. I heard that term being used 20 years ago, but now the RDL has shown up again associated with wafer-level packaging.

Korf: I have seen that in Asia in cellphones and IoT devices; they want to get rid of that package and drop the device down to the board where, theoretically, it’s more reliable and somewhat cheaper. However, RDL is not very well installed over in Asia because it’s extremely expensive to set up a line to do that. The concept is to get rid of the device package and drop the die down onto the mainboard, like in cellphones.

Johnson: Could you give us a tutorial explaining what the RDL is and its purpose for those who might not be familiar with it?

Korf: If you look at a traditional HDI packaging or PCB technology, you get down to 2-mil or 1.6-mil lines, and your via pads are still fairly large because you have to drop vias down into the board. If I wanted to start doing 10-mil vias into a 4-mil pad with a 1-mil wide line or less for 20-micron, 30-micron, or 40-micron layers and above, those can be done with HDI. You have to put a layer down on the outer surface so that you can now lay down that 20-micron wide line into a 100-micron pad and put your die directly onto the board. You can't afford, and you can't use that technology to make the entire structure—meaning the entire board with six, eight, or 12 layers—because of the cost and the technology doing the outer layers to redistribute the pitch to a wider pitch so that you can build it into the board. I call it RDL, taking a fine via pitch and spreading it out to go down for the rest of the board.

You have to look at the physics of the material and the interconnect.

Bauer: I agree with that. The scaling of dimensions at the chip level and the package level is very different than at the board level, and the RDL is a very simple term for making the two match geometrically.

Holden: That's because the semiconductor companies continue to do die shrink.

Korf: Exactly, That is driving down the I/O pitch, which is driving down on the I/O pitch on the board.

Holden: And a smaller device turns on and off faster, which means the critical length before

the required transmission line shrinks. It's all about physics. It's also like death and taxes: You can't avoid it.

Korf: You have to look at the aspect ratio and the material properties of the dielectrics. Some good papers have been published on that topic in the last couple of years. You have to do a good 3D simulation of that RDL and what it attaches to so that the via doesn't break off like it used to do with BGA packages to boards. You have to look at the physics of the material and the interconnect.

Johnson: Dana, that sounds like a design-time consideration.

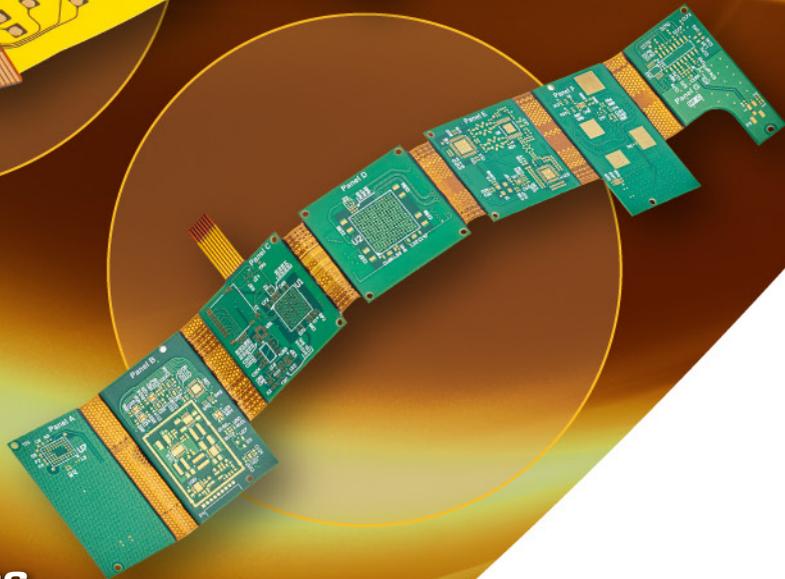
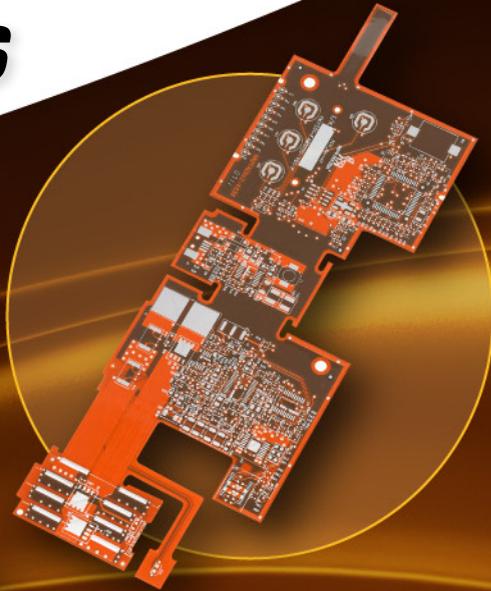
Korf: Yes, because the material is very thin, and you don't want a thick via structure. If you go back to the '80s and that period for initial surface mount, we had ceramic TCE mismatch to the FR-4 that was breaking solder joints. It has resurrected where the vias will separate from each other due to CTE differences from the various materials being used to have that very fine-pitch part mounted to this PCB structure.

Johnson: We have these challenges in addition to packaging, of course. The semiconductor industry continues to shrink the die as much as it possibly can, and we understand why that is. It allows them to put more chips on the one wafer and increase their profit margins. However, that creates this particular kind of stress at the board level. Then, the OEMs—especially, in automotive and medical, for example—can get more functionality in smaller real estate. But where we seem to have the biggest challenge at the moment is connecting those very small chips together across what we can do on a circuit board. What's going to give first?

3D Printing

Dan Feinberg: Chuck, I'd like to hear your opinion on some of the recent advances in

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3D-printed circuitry—not necessarily making a circuit board, but 3D printing of interconnect circuitry, especially with the advances in printing resistors and capacitors for interconnects. Do you think that might have an effect?

Bauer: I've been playing around with 3D printing for about six years now in general, but not specifically in electronics. It's going to have an impact, but in a while—maybe the next five or 10 years. I doubt it will happen faster because things don't get adopted that fast. If you've ever worked with polymer thick film, for example, you know that we can print resistors, inductors, capacitors, no question. But it's like buried capacitance in a PCB: How many people are doing that anymore?

It's very hard to control and design, and unless it saves a lot of money and is a game-changer, it's not going to make a difference. If you're using 3D printing to do prototyping or customized products for a specific application, that makes a lot of sense, even today. But when you go to volume, there are niches where it works. In PCB assembly, the biggest application of 3D printing in the electronics worldwide is making masks for connectors during conformal coating.

Feinberg: One of the reasons I asked is because there seems to have been a tremendous advancement by the people at Nano Dimension, and the number of machines that they're selling has gone up exponentially over the last six months. Also, the majority of what they sold seems to have been to the military.

Bauer: And the reason for that is that the military has the most customized needs in the world.

Feinberg: Right, and they also are less cost-sensitive.

Bauer: Correct. It is amazing. As I said, the biggest electronics application has been masks for connectors because if you order masks for connectors, you have to order them six or eight weeks ahead of time and must order a min-

imum quantity. You may not have that big of an order, but if your production planning group says, "We're going to build 100 of these boards tomorrow," at midnight, you have the 3D printers start printing masks, and you have the 50 printed masks that you need to do 150 boards because you can use them over about five times, and now you can have them by the next morning. You saved eight weeks and all that inventory. Cost is going to drive that.

With 3D-printed electronics, it's going to still be relegated to very simple circuits because 3D-printed resistors, in particular, are very sensitive to moisture. The capacitors and inductors are also very sensitive to moisture, and the precision with which you can print is still not up to the level of what you can get with the traditional approaches in most cases. There's always the one-off. Somebody can always give you an example of having a perfect 3D-printed circuit, but building it in volume is a different subject.

Glass Substrates

Holden: Chuck, when you talk about ceramic, would the glass panel also be in that same category? I say that because Atotech showed a machine for 610x610-millimeter pattern plating of two-micron geometries on glass.

Bauer: Absolutely. They have been working on that for several years with Dr. Rao Tummala at Georgia Tech. They're part of that consortium. Rao has retired now, but the program and the center are still there, and Atotech is a big part of that.

Holden: At Gentex, they helped us do a 1x1-meter panel of electronic glass that we had metallized with ITO. We had phenomenal yield, and I hate to say how many packages came out of those thousands and thousands of meter-by-meter panels.

Bauer: That's going to be a fascinating area over time because if you talk to the semicon-

ductor companies, one of the things that you learn is that that sort of volume creates its own unique set of problems and challenges.

Holden: There's a new generation of lasers that will cut glass in milliseconds without any sharp edge. I'm not sure if it's an X-ray laser, but you can shave up that one-meter-square piece of glass into 10,000 individual pieces that are all perfect. Afterward, you can sputter additional layers on it, not the initial ITO, but a carbon nanotube. Because of the size, the unit cost is much better than using silicon PCBs made out of wafers as a packaging substrate. Glass can have better mechanical and electrical properties than silicon but be much larger as a panel.

Routers

Bauer: Cisco would love to have a memory device that was 512 bits wide and four bits deep, but nobody will make it for them. The world market for that memory device because that device would be perfect for switcher routers. It would help them make them much faster and more efficient. It would make them more reliable because there wouldn't be so many different board assembly operations. However, if one supplier was making them, they would not have to make more than 3,000 or 4,000 wafers a month to supply the world market.

For them to come down the learning curve and get their yields up requires a minimum of 5,000 wafers, and they don't even look at a market unless it requires 20,000 wafers a month and be able to sell it at a reasonable price. To get a memory maker to design a 4x512 memory, you can't pay the company enough money to do it. It's cheaper to take the 16x32 memories, line them up on a board, use them as 4x512, and configure them. It's cheaper because you can use the reject die from the high-density memory companies. Doing glass on the meter-square sheet is going to create that same kind of challenge. If they don't have enough volume to come down the learning

curve and get the yield up high, it's not a product that's going to fit in that format, even if the material would be ideal.

What's Going to Give?

Johnson: What's going to give first? It sounds to me like the answer to what's going to give first is the substrate.

Holden: The substrate has always been the unique piece of it. You take the standard chips, and how the customer sees them, and it's often oriented and packaged along with some of the other stuff we add to the circuit. That's an infinite variability there working with standard chips and components.

Matties: If we put this in terms of an assembler today who is putting together their five-year roadmap for their business, what should be their considerations?

Korf: We already see 0.4-, 0.3-, and 0.2-millimeter pitch devices go on boards. With 0.16-millimeter pitch, what's driving RDLs are MSAP, SAP, and a bunch of processes trying to get that pitch down. It's also driving electrical test and solder mask capabilities, and it's hard to lay a web down that small in solder mask and get a high-speed, high-volume contact that's good when the pitch gets that small.

Active Embedded

Matties: I was recently visiting AT&S in Austria where they have been doing the active embedded for a while. It requires new testing and handling challenges and new disciplines. If a company is putting together a roadmap, is that an emerging opportunity?

Korf: It's an area that always gets talked about, and I came back from several years in China this year. People would say, "We're ready to do it. Who wants to buy it?" Well, nobody. Only a few companies are doing it. It's only

a few devices. Most people put down a cavity instead so that they can access it from the outside. It's almost a catch-22. No one wants it, so no one's going to fund someone to do it. It needs a couple more people. You're correct in that AT&S is a good leader in this. A couple of Japanese companies are also driving this, but it's a relatively low-volume process. However, their applications will typically be in fairly high volumes on a part-number basis.

Matties: They talked about supply chain challenges for this technology.

Korf: Big issues come up. I did an investigation once where we tried to put 132 devices in a module embedded, and the yield was zero.

The question fabricators had when we were approached with this was, "Who pays for the board when the component is bad?" The shops, customers, and EMS suppliers aren't going to pay for it, and then it stops.

Matties: The decision to go with the active embedded is a design or an OEM decision. But the advantage of active embedded is enormous, according to AT&S, because you get a lot more functionality out of a lot less space.

Korf: There's no question. The liability discussion is what's holding it all up. Who's going to pay for it?

Matties: This has been great. Thank you very much. SMT007

Changing Dynamic in Stencils

In the last 20 years, the electronics industry has been making adjustments to accommodate shrinking component sizes, and the shrinking trend continues to grow.

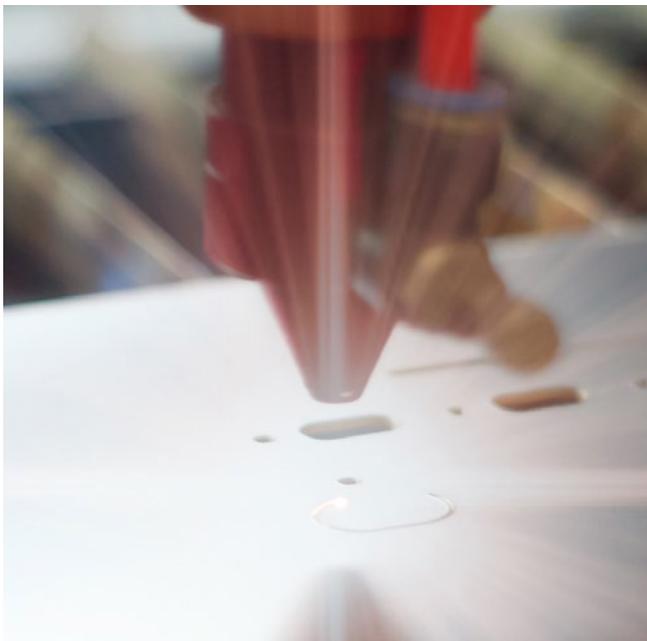
High-precision fiber laser cutting systems allow stencil manufacturers to cut an aperture as small as 0.00025", but that doesn't mean that solder paste will get through that opening. Metals with smaller grain structures, nano-

coatings, careful solder paste selection, and proper aperture design work together to achieve optimal paste release.

However, the challenge doesn't stop at simply getting the paste to release from the stencil. The appropriate solder volume required for each device must also be achieved. This can be difficult with densely populated boards that have a high mix of devices (i.e., connectors on the same board with micro-BGAs), especially utilizing a single stencil thickness. The aperture design can be manipulated to a point, but the area ratios must be met to maintain paste transferability; often, maintaining a 0.006" stencil thickness for those big connectors cannot be done with small chips and other micro-devices on the board.

While there have been significant advancements in paste deposition machines, or jet printing, stencils are still the most effective tool for high throughput. Multi-level stencils (step stencils) have answered the call for these high mix boards, allowing for optimal paste volume for multiple device types with a single stencil. The connector now gets the 0.006" deposition it needs, and the micro-BGA has a nested pocket, allowing for 0.004" paste deposition.

(Source: Stephanie Hardin, Integrated Ideas and Technologies Inc.)





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What's Driving AOI Innovation and Collaboration?

Feature by Brent Fischthal
KOH YOUNG AMERICA INC.

Industry 4.0 Discussion

Big data is the foundation for Industry 4.0, so advanced inspection systems must evolve from simply judging “pass/fail” tools into highly intuitive, dynamic decision-making systems that emphasize the need for reliable, traceable data. Artificial intelligence (AI) engines can empower tools to help customers analyze and optimize the production process by managing process data from connected SPI and AOI systems.

When we look at the optical inspection market growth trajectory, we can see how process challenges helped create innovations. For example, solder paste inspection (SPI) has undergone a shift from 2D to 3D because the 2D inspection technologies manufacturers traditionally used to collect solder deposit images could not solve shadowing problems. Thus, companies developed 3D SPI to capture the printed solder paste height to accurately measure the total volume of paste printed. Several years later, we see the same need for surface-mounted component inspection with AOI systems.

As today's board complexity is increasing with more components and joints, higher density, and shrinking package technologies, such as the 0201 metric (008004 imperial) microchips (Figure 1), basic AOI technologies using blob analysis or high megapixel cameras may no longer be practical. Most decisions made are based on a “good/bad” comparison of reference images, which can easily be affected by variables like component surface finish, board condition, component proximity, and more.

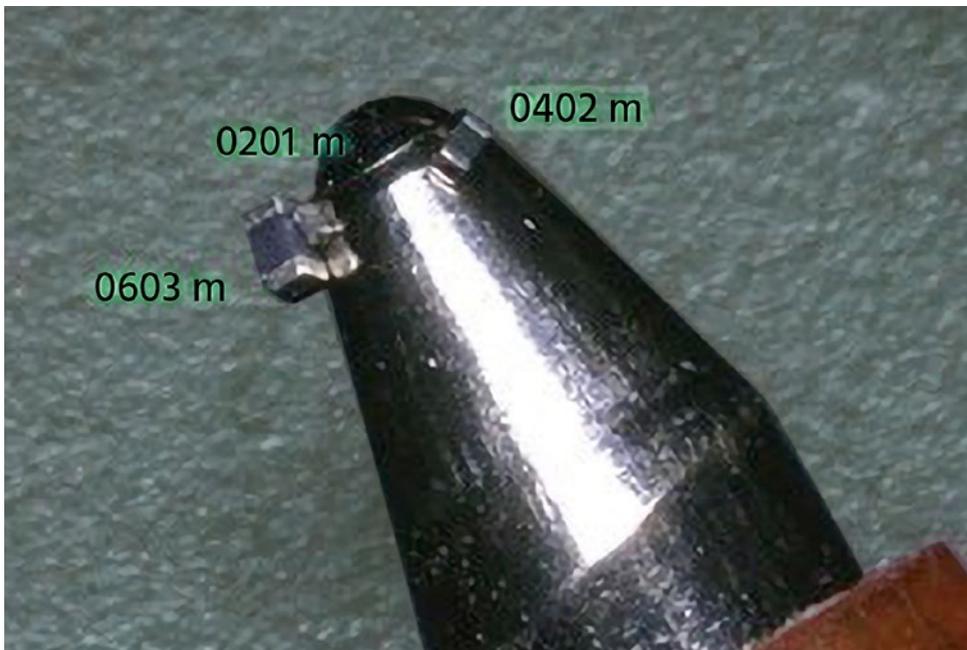


Figure 1: Using a ballpoint pen for reference, the image compares an 0201 metric (008004 imperial) component with an 0402 metric (01005 imperial) and an 0603 metric (0201 imperial) component. (Source: ASM Assembly Systems GmbH)

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Although 2D AOI is still a technology in the market, more manufacturers are adopting 3D AOI to increase board quality. The benefits are clear. Using clearly defined thresholds backed by accurate data will eliminate the need to constantly debug inspection programs. Moreover, measurement data generated from some 3D AOIs provides meaningful insights about the process and helps eliminate the root causes of a defect. Combining a 3D SPI with 3D AOIs enables manufacturers to accurately control and monitor the board assembly process.

But with so much data, engineers are hard-pressed to collect, process, and implement all the data using traditional techniques and software. AI and deep learning lay the foundation for machines to learn from the vast amounts of process data collected by adjusting the output based on the data inputs and performing tasks to help engineers perform tasks more intelligently. The many examples we hear about, such as computers playing chess or autonomous (self-driving) vehicles, use deep learning to achieve tasks by processing large amounts of data and recognizing patterns in that data.

This is ideal for volume PCB production and helps create a data set for a smart factory. From statistical process control to instant program refinements, AI-powered platforms can intelligently apply real-time data to improve production processes. Going beyond smart factory solutions, manufacturers can use the same technology to optimize the process and adjust process parameters by exercising complex machine-learning algorithms.

Realizing a smart factory means taking a practical approach to processes and systems while examining areas to improve productivity. Combining machine learning with 3D measurement data generated during inspection helps manufacturers define inefficiencies and boost line efficiency. Machine learning uses programmed algorithms that receive and analyze input data to predict output values within an acceptable range. As new data is fed to these algorithms, they learn and optimize their operations to improve performance, developing intelligence over time.

For example, some tools allow manufacturers to simultaneously deploy programs and inspection conditions across multiple lines, which enhances productivity and, more importantly, data integrity with consistent performance. Operators can further improve line maintenance with other tools for real-time monitoring to instantly display relevant process parameters at remote locations for immediate analysis and action. What's more, combining multipoint views from SPI, pre-reflow AOI, and post-reflow AOI with real data management and monitoring allows operators to determine actionable insights to optimize the processes. However, the adaptation of AI-powered process tools takes optimization to a higher level.

Converting all the data requires a simulation tool to review identified defects with accumulated historical data from printed circuit board assembly (PCBA) lines while avoiding unnecessary downtime. Software tools can reliably allow manufacturers to predict the effects of fine-tuning without stopping the line. Moving forward, an AI-powered platform can autonomously render complex process optimization decisions typically reserved for dedicated process engineers. Embracing connectivity can create a smart factory. For instance, software modules can exercise complex algorithms to develop closed-loop process recommendations. The machine-to-machine (M2M) connectivity drives the smart factory vision one step further by enabling automatic SMT line maintenance. Finally, combining inspection with printers and mounters can enable the network tools to connect and simplify communication across the entire PCBA line.

Defining the correct process parameters often requires a high degree of expertise because of the various environmental considerations affecting the process. Using AI-powered systems and M2M connectivity, manufacturers can link inline inspection systems with the associated printer and mounters in the line to overcome the challenges. Figure 2 shows how automated machine learning can already match the results from process experts, and this will only improve.

Advanced Process Control Methodology

Reliable AOI methods have become powerful, economical complements to traditional test strategies. AOI can be used successfully as a process monitoring tool for measuring printing, placement, and reflow performance. Some advantages include:

- Detecting and correcting SMT defects during process monitoring is less expensive than after final test and inspection, where repairs are typically 5–10 times more costly
- Detect trends in process behavior, such as placement drift or incorrect mounting, earlier in the overall process. Without early inspection, more boards with the same defect could be rejected during functional test and final inspection
- Identify missing, skewed, or misplaced components with incorrect polarity earlier in the assembly process when component placement is verified before reflowing

Yet, a single inspection system has limitations, especially when there is limited or no communication with the balance of the line. In this setup, it simply cannot optimize a PCBA process. Equipment suppliers must cooperate to achieve communication for a zero-defect future. M2M connectivity can optimize the process by exchanging real-time SPI and AOI measurement data with other machines in the production line. This real-time feedback includes measurement data such as offset, volume, height, area, and warnings to other sys-

tems, while analyzing trends to optimize the process and identify trends. The connected systems can automatically define correlations between the processes.

For instance, the PCBA industry has many studies and documentation detailing how the solder reflow process can help position surface-mount components normally on the pads, even if component placement is off pad. However, the trend to shrink components to 0.3-mm bumps or 0201M microchips is opening doors to explore how process controls can improve yields in high-density placements.

Enter advanced process control (APC), a proven control and optimization technology delivering measurable and sustainable improvements in production yield. Most engineers will agree that stabilizing control loops, with underutilized or ineffective process time and strong process interactions is exceedingly difficult. APC has become a standard solution for realizing stable control processes, and, quite simply, it is the added value upgrade to a process automation system. APC collects and analyzes solder and component location data from an inspection system and then sends the recommendations across the line to printers or mounters for automatic implementation (Figure 2).

Manufacturers want to monitor and adapt the process to achieve zero defects by accessing all the data, anytime, anywhere. They must also cope with shorter life cycles, so inspection solutions should be able to collect and analyze a large amount of data to produce traceable results.



Figure 2: Theoretical SMT lines using APC active feedback between solder paste printer, SPI, component mounter, and AOI systems.

APC Printer Feedback Results

The continued demand for smaller, lighter, and smarter electronic devices has led to an increasing use of smaller components. These shrinking packages force smaller aperture designs and finer solder paste, which have made stencil printing a highly-sophisticated process with a tremendous impact on production yields. It has been reported that 70% of all PCB assembly defects are primarily due to problems directly associated with the solder printing process. Manufacturers must ensure the optimal printing parameters are consistently applied during production.

An enhanced solution, formed of interlinking software modules, can actively optimize the printing process by combining real-time printing information with SPI measurement data. More advanced software automatically performs design of experiment (DOE) intended to complete a detailed SPI result analysis using advanced diagnostic algorithms and noise filtering models and then recommends the ideal print parameters. The software triggers the SPI to send the information to the screen printer to automatically adjust the parameters. The max and min values for printing pressure, printing speed, and separation speed can be set when adjusting the printer parameters.

Other software can use multiple anomaly-detection algorithms to actively optimize the print process and further reduce false calls. Ideally, the software will evolve to autonomously generate optimized models and fine-tune the process parameters in real-time using actual results. While the software modules

would each provide standalone process benefits, the combined power of an AI-powered software suite would ensure the highest process reliability and production flexibility without dedicated resources and expertise.

APC Mounter Feedback Results

With the benefits of printers communicating with SPI machines known, what about mounters and AOI? Connecting mounters with AOI delivers obvious benefits like improved yields, especially in high-density boards. The mounters use the received data to update the placement program, ensuring the components are placed onto the solder deposits rather than onto the substrate pads. This approach to placing components on the printed solder uses the self-alignment principle to increase production yields and reduce defects. As shown in Figure 3, when solder is off pad and components are placed to the pre-defined placement location in the program, self-alignment is not effective. During reflow, components will shift off pad or bridge with other pads, causing rework or scrap.

Alternatively, corrected placements will maximize the self-alignment principle. Mounting these microchips onto the solder paste instead of the pad will increase yields and quality. Figure 4 shows a set of test results. Using this advanced communication, the 3D AOI can feed corrected mounting position values to mounters, which ensures the mounters place the components in the correct position. This improves process repeatability by automatically adjusting placements and identifying trends to make further positional corrections.

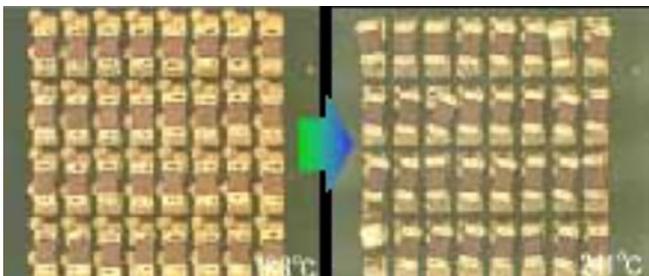


Figure 3: Traditional chip placement onto pads before and after reflow. (Source: Panasonic System Solutions Company of North America-Process Automation, or PSSNA-PA)

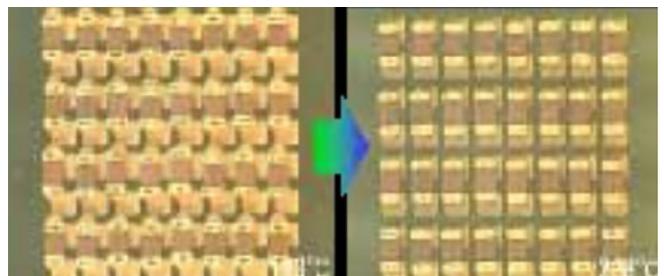
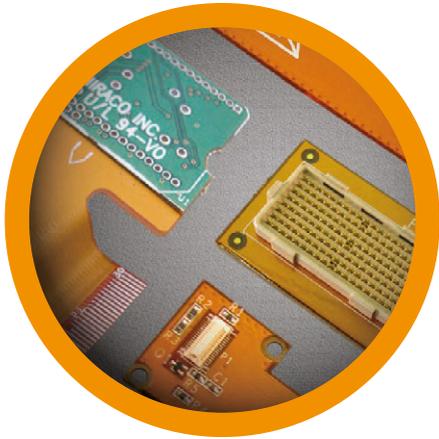


Figure 4: Controlled chip placement onto solder before and after reflow. (Source: Panasonic System Solutions Company of North America-Process Automation, or PSSNA-PA)

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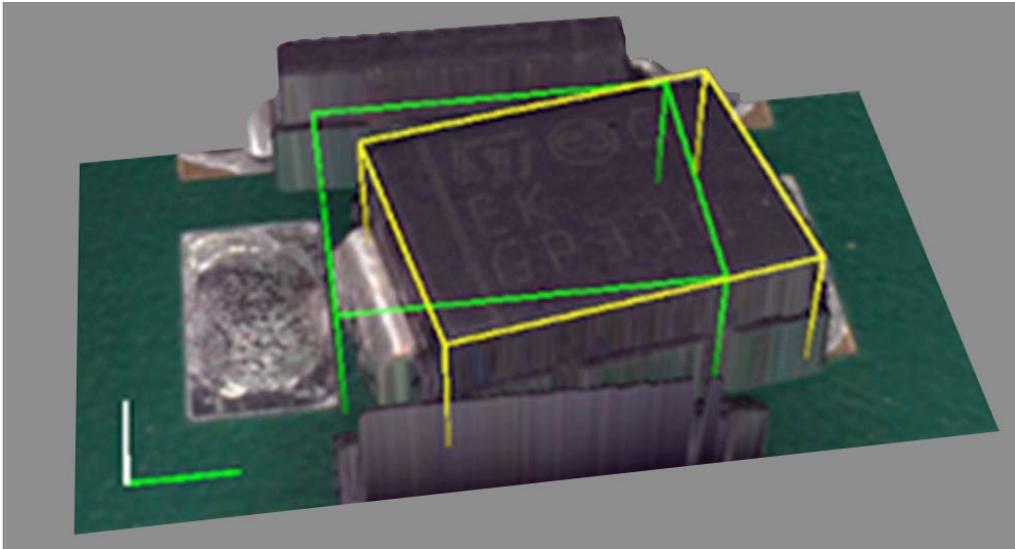


Figure 5: Example of pre-reflow 3D inspection detecting part skew, which is fed back to mounter.

Using real data from quantitative measurements, certain 3D AOI systems feed correct component position values to component mounters and ensure components are mounted in the targeted position. This type of feature improves process repeatability by automatically adjusting component placement to the paste rather than to the pad location (Figure 5). Moreover, the software will identify the shift trend and conduct further position correction by using true 3D measurement data from the AOI system.

Connecting inspection systems with mounters can help achieve complete line communication and further enhance the value of the inspection process. For example, M2M connectivity optimizes the process by exchanging real-time measurement data between the printer, SPI, mounters, and AOI systems. The systems feed offset and warning data to other systems while analyzing trends for process optimization and traceability. Combined, this process provides unsurpassed performance power.

Communication between equipment will improve process repeatability by automatically adjusting component placement to the solder deposit rather than to the pad location. This advanced process further improves microchip mounting reliability. Networked intelligent systems that allow real-time results to be correlated, calculated, and visualized will become even more essential in the smart factory.

Conclusion

Industry 4.0 and its associated benefits will help advance the industry. Equipment suppliers need to work diligently to accelerate M2M communication standards implementation to help the situation. Initiatives like the IPC Connected Factory Exchange (CFX) and IPC-Hermes-9852 underpin the efforts within the industry to develop standards and create a smart factory. These M2M communication standards, guided in part by Industry 4.0, are quickly altering the manufacturing process by improving metrics like first-pass yield and throughput by applying autonomous process adjustments. Far beyond an automatic line changeover, this two-way communication with suppliers will allow the equipment to automatically adjust production parameters to increase board quality and lower costs by eliminating rework and scrap. As part of this mission, APC with interconnected PCBA equipment will revolutionize process optimization and lay the foundation for the smart factory. **SMT007**



Brent Fischthal is the senior manager of marketing, Americas, for Koh Young America Inc.

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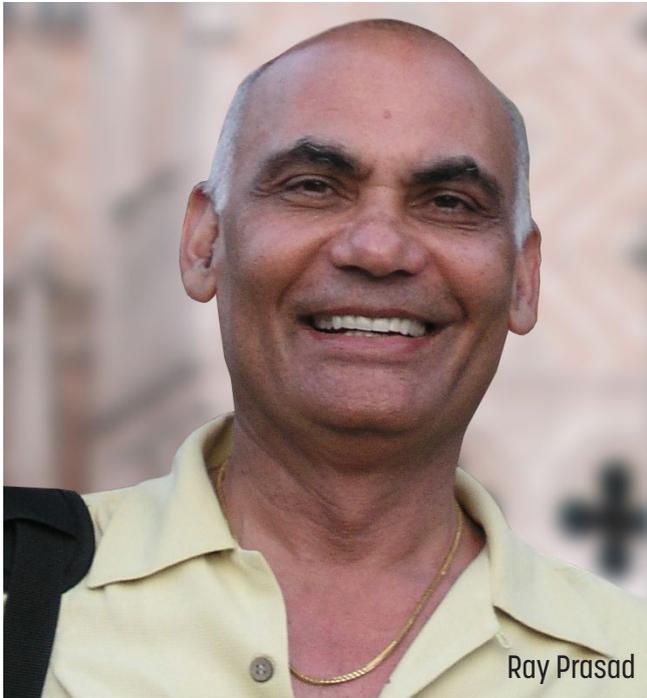


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The Big Picture on Small Components

Feature Interview by I-Connect007 Editorial Team

The I-Connect007 editorial team speaks with Ray Prasad to get his take on the drivers behind smaller component sizes and what he sees in the industry. He also talks about the need to focus on the front end, the printing and imaging area, and why that's a limiting factor currently.

Nolan Johnson: We're exploring the trend toward smaller component and feature sizes on boards. The dynamics cause stress on the capability of our manufacturing supply chain. The questions we pose are, "What's driving this trend right now? Are the components driving the features on the boards, or are the features on the boards driving components?"

Ray Prasad: If you look at the big picture, the driver is Moore's Law. In the '60s, Dr. Gordon Moore said that the performance of the silicon would double every 18 months or two years, etc. The silicon has to be put in some kind of housing—the package. The package has to get onto the circuit board, and there are a lot of these packages that will be on the circuit board.

One electron goes from one place to the other through the wire bond, through the lead, through the vias on the board, through a circuit line on the board to another wire bond of the next package, and then to the lead and back finally to the silicon. This is like commuting for an electron through rush hour traffic at a slow speed. In the process, you have the parasitic loss. The silicon designer talks in picoseconds in terms of performance, but the board designer talks about nanoseconds when they do their timing budget. The electron is slowed by the inductance, capacitance, and resistance of the wire bond, the circuit line, and so on.

To make the performance better, you have to reduce the pitches, lead sizes, wire bonds, etc. These are examples of package features that improve the electron's speed. Going from through-hole to SMT, then to fine-pitch to BGA to BTC to flip-chip also improves package performance. Similar progress—in terms of lines and spaces on the substrate level—hasn't happened as much. In the '80s, we were at 10-mil lines and spaces, and now, we are probably at five-mil lines and spaces in high-volume production, and some people can push it to four-mil lines and spaces. This is one of the examples of why the circuit board's performance is



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one of the bottlenecks in the performance of overall electronics systems.

Dan Feinberg: Size and weight are huge, which is a big factor right now, especially as we demand the capability of various devices to do more and more things, yet they need to be smaller.

Prasad: Yes, but at the end of the day, it all depends on the application. In consumer applications, of course, weight and cost will be the key drivers. Then, there are cases that the processor is a 25-watt device, in which case, the thermal performance would be the main driver. Of course, cost always plays a role in any application. The point is that the same thing doesn't drive everything in every application. If you are using a device in a satellite and going to space, they don't care as much about the cost. Even in consumer applications, like laptops, if you have a big wattage device, and don't want a fan to cool it, the thermal performance would become important. It all depends on the application.

Matties: If we bring it into the assembly process, what are the challenges that you think our industry is facing with the finer pitch?

If the pitches get below 10 mils, most people have a hard time printing paste because the pads are so close that you may have bridging.

Prasad: What are the processes on the assembly side? You print it, place it, reflow solder it, clean it, and test it and rework it if necessary. All these process steps are affected by the pitch somewhat. Printing is affected the most. If the pitches get below 10 mils, most people have

a hard time printing paste because the pads are so close that you may have bridging. For a company with good infrastructure, they have no problem paste printing up to roughly 16-mil pitch. But when you get below 16 mil pitch, printing capability is a key constraint for most companies. I don't think the real problem is in the placement and reflow.

Matties: Are you talking about stencils and jets?

Prasad: Yes. The biggest problem is there are only two kinds of defects, even though IPC-610 is a thick book with a couple of hundred pages. IPC-610 has a list of all kinds of defects, defects that are important are shorts (bridges) and opens. If you really think about it, shorts and bridges are the real defects that determine whether something passes or fails.

An interesting fact is that most companies have more opens than shorts. Ask somebody at any company to collect the data for the last six months, and say, "Break down all your defects into three categories: opens, shorts, and everything else." The number of opens in any company is about four or five times more than the shorts. What I like to advocate is you should shoot for the number of shorts to be way more, even six times more, than the opens. But why?

Shorts can never escape the test because they will flunk in-circuit, functional, visual, etc. They will be caught, and the customer will never know, but the opens or insufficient defects will escape. They will even pass in-circuit test, and that's why there is lot of confusion and disagreement between suppliers and users when there is a failure either at the customer site or in the field. Resolving the root cause can be very expensive.

However, if I apply maximum paste and have a bit more bridges, they won't escape since I can catch them before shipping. I also want to emphasize that I don't mean you should have lots of bridges. All I am saying is that there should be more bridges and fewer opens in your process; the ratio of bridges divided by opens should be closer to six. When we keep reducing the pitches, the defect rate will be higher.

Matties: With the finer pitches, do you think that there's going to be a natural or inherent movement to shorts versus opens because of the nature of proximity?

Prasad: There will be, but what people do is strange. They will still have more opens even in finer pitches because when they see bridges, they take steps to reduce the paste volume and thickness of the stencil. People don't want to see the bridges because it's obvious. To reduce bridges, they redo their stencil design (stencil thickness, stencil aperture, or both) because they don't want to see bridges that are easily visible to everyone.

To answer your question, with reduced pitch, there will be more bridges, of course, but people would modify their stencil and printing process and end up with insufficient solder. This leads to more opens instead of more bridges, as you might expect.

Matties: Even though it's closer, the tendency is to apply less or thinner.

Prasad: And that's why the defect level with finer pitch is 10,000+ parts per million when you are using less paste (there are other reasons, such as lead fragility).

Matties: How does the solder paste manufacturer fit into this?

Prasad: For paste printing, there are many guidelines. One of them is that the ratio of stencil aperture to solder powder should be 4:3 or more. In other words, more than four solder balls should pass through the stencil aperture so that there is no clogging. There is also a guideline for the stencil aperture width. The aperture width is roughly half the pitch. Generally, when the pitches are lower, you make it more than half the pitch. For 16-mil pitch, you may want stencil aperture to be 10 mils.

Smaller pitches need smaller powder sizes. However, the smaller the size of the powder, the higher the exposed surface area of solder powder. More surface area means more oxidation, and if there is more oxidation, you have

more solder balling. For smaller powder sizes, you need an inert environment like nitrogen. Make those powders in an inert environment and ensure they don't oxidize because the smaller size is more susceptible to oxidation. The paste manufacturers have a huge role, especially paste for fine pitch.

Matties: The construction geometries of the stencil will play a role in this too.

Prasad: Yes, you need thinner stencils for finer pitches. There's a limit to how thin it can be, depending on the metal. When some people want to make two- or three-mil stencils, it becomes very hard, and they try to do it with a Kapton tape. Also, with the electroformed stencil, which is plated stencil, that's where it makes sense for fine pitch. Electroformed stencils are not rolled steel, so they are not going to be as strong, and the cost is five times greater than normal stencils, which cost \$200–300; electroformed stencils will cost \$800–900.

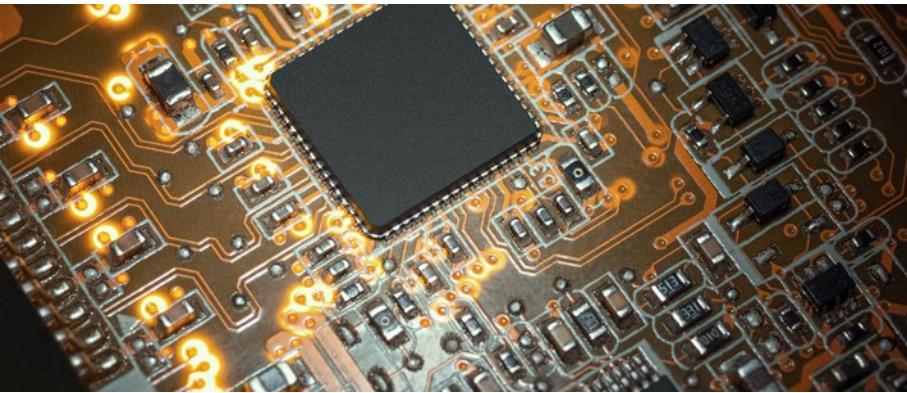
You need the electroformed stencils with their very smooth surface so that nothing gets stuck to the sidewalls, and all of what you're depositing needs to go fully on the board when you're lifting the stencil. If the surface is not very smooth, some of that paste will come back with the stencil when it's being lifted, and then you have insufficient solder.

Matties: When you're talking about lack of solder paste, are these going through an inspection process in SPI?

Prasad: They are, but there's a big range when it comes to paste coverage—from 65% to 125–225% of the pad area that's covered—and whatever the height is, so they need to do that.

Matties: My point is if it's going to SPI, you're going to see if there's not enough solder or paste rather before it winds up as a field failure.

Prasad: That's what you need to do, and you have to set those standards on the higher end (closer to 100% pad coverage) for acceptance



so that you have the maximum volume. SPI would help.

Matties: Is that a standard practice now in most shops?

Prasad: Not for everybody. It depends. If you buy a \$50,000 printer, it's not going to have SPI capability. I also want to mention that the most important capability you need in a printer is the ability to suck solder out of the stencil aperture. When the pitches get smaller, you want to ensure that nothing gets stuck in there. As the pitches get smaller, it becomes harder and harder to meet that requirement. The capability to suck solder out of small aperture is available mostly in more expensive printers (100,000+), and not everybody has such printers.

Matties: For the fine pitch, you said placement isn't an issue or should be a non-issue.

Prasad: For most people, the placement is not an issue because most machines are a lot better than they used to be; even if you are off, you are allowed to be off by 50% for Class 1 and 2, and for Class 3, you are allowed to be off by 25%. You don't have to be perfect, and self-centering takes place. When the solder melts, it will pull back in, even if it's a little bit off.

Matties: Are you talking about a standard subtractive process?

Prasad: Yes. I don't think additive processes are common at this time.

Matties: Where do you see the fine pitch being utilized, and how ubiquitous will this be in the world of electronics?

Prasad: Nobody wants to buy a big phone. Wherever you need small size and weight, that's where the fine pitch has to be. We are also achieving more shrinkage by the adoption of area array

packages, such as BGAs. For example, if you convert a 0.5-mm pitch QFP to a BGA, the pitch will become 1 mm, and the size will become smaller because you are using the entire bottom side of the package. In addition, when you use 1-mm pitch package instead of 0.5-mm, your printing doesn't become a problem.

If you use ultra-fine pitch packages, such as 10 mils, you will have not only a printing problem, but a major handling problem as well because the leads would be so fragile. That's the other part of the reason the problem happens—not the printing—because when the leads are that fragile, they will cause mechanical problems before you get to placement.

For ultra-fine pitch, the placement becomes more important. The way to talk about that is not in terms of pitch, but pitch and what kind of package. If it's a very fragile package where the leads are only on the periphery (QFP), then handling and placement will become critical. But if the same package is in a BGA or BTC, you can drop it on the floor, and nothing happens because they're very robust. It depends on the package.

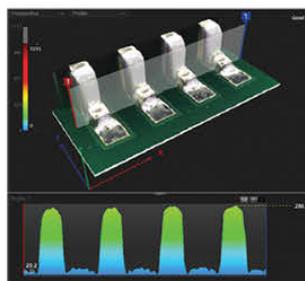
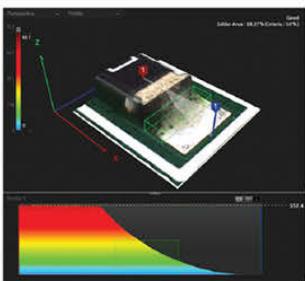
Feinberg: Some devices, but not many, have no circuit boards. In other words, the entire device is on the chip and the connection between the chip and the user is done wirelessly, as well as the controls; there are no circuit boards in it. I got to see some this week at CES.

Prasad: Look at the stocks and the PE ratios between hardware and software companies. With hardware, if you're hitting a limit, some of it can be addressed with software or AI.

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Feinberg: Absolutely. We have no way yet to exceed the speed of light with electron flow.

Johnson: I wanted to double back to the threshold for when you move from subtractive to additive. Is that threshold well-defined, and is it moving?

Prasad: I am not an expert in that area. From observing the additive process, I see that many people are using that, whether the reason is in terms of the technology or cost. Imagine if we are able to do the circuit board in one or two mils; the number of layers that we now need, initially being eight or six, it could be two.

Then, the cost would go down, but the cost goes up because of the one- or two-mil line, which can probably be done with the subtractive process. Why is that not being done? I don't know the answer.

Johnson: We had a number of conversations through 2019 with people in the supply chain, and some of the advice with regard to components was, "Go as small as you can," because the drive to make the smaller components is happening thanks to automotive and cell-phones. The secret to a longer-life product, according to these bill-of-materials experts, is to use the smallest components you can. If design teams start following these guidelines, does that get them closer to needing to use some other process?

Prasad: I don't think the size of the component matters that much. In terms of the size limit, that is already happening with 0201s and 0105s, and my advice has been quite the opposite, generally. You should use the largest component possible to do what you want to do, meaning the pitch. Go with the largest pitch. The only time the size matters is if we're talking about 0402 or 0201—the resistors and capacitors.

Johnson: The largest possible pitch makes sense.

Prasad: The largest possible pitch is what you want to go with. You can have your cake and

eat it too if it's a thin package, and you are going to use that as a BGA-type package versus QFP.

Matties: What is your knowledge around active embedded?

Prasad: There's quite a bit of effort. There is some movement, but I don't know that that much is happening in that area for active embedded. Think of the passive resistors and capacitors and what it would take to get them incorporated. We have been talking about embedded passives since the '80s, but how many embedded passives do you see today? If that was happening, we wouldn't be using the 0201 or 0105 because, in any particular board, you have hundreds of these passives being placed, depending on the size of the board. That's a lot simpler than trying to embed the active ones.

Matties: Why do they not use the passives as embedded?

Prasad: It's all about money.

Matties: It costs more to have it embedded?

Prasad: Yes. And remember, each board is unique; you could make one, five, 10, 20, 100, 1,000, or 10,000. When you make components, you make millions and billions. You can never have the efficiency and yield of these processes that make millions and billions versus even if you make 10,000. Ten-thousand boards a day is high speed for most people, and that's nothing for a component supplier. If you compare that to the volume of the components and passive components, they're in the billions. It's hard to get that efficiency in a low-volume environment and make them cost-effective.

Matties: It's always enlightening to talk with you, Ray. We appreciate your time. Thank you.

Prasad: You are welcome. SMT007

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Big Trouble Comes in Tiny Packages

Quest for Reliability
Feature Column by Eric Camden, FORESITE INC.

When it comes to making consumers happy and electronic assemblers miserable, nothing achieves both quite like miniaturization. With our ever-increasing demands to house a full-size movie theatre with surround sound and limitless digital storage in the palm of our hands, the only way for CMs to respond is with miniaturization (and cursing—lots of cursing). In this installment, I'll revisit the history of shrinking packaging and lessons learned.

The move to make products smaller isn't anything new, but, at this point, it is a matter of scale. Making a computer's physical footprint fit inside a room smaller than the size of a football field was a big leap, but a lot of the technology required to do that didn't exist until that happened. There was a healthy amount of new component technology being introduced into the industry at the time that made that process much easier in comparison to what the industry is working with today. When the size of a product has already been reduced to the smallest thing you've ever seen, making that even

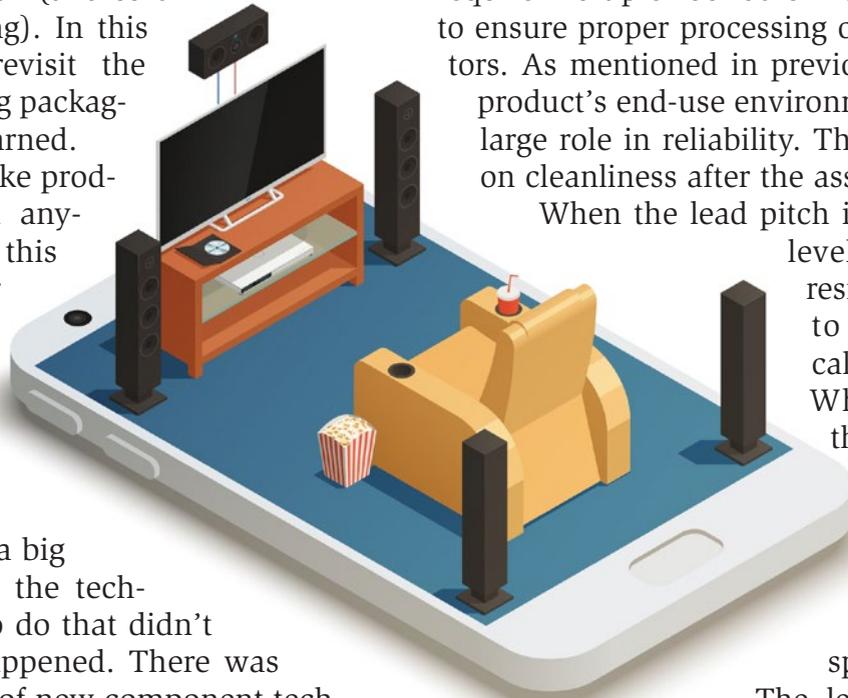
smaller will require shrinking of every component that is already being used.

Any time you reduce the spacing between leads or contacts with bias differential, you increase the risk of electrical leakage and electrochemical migration. Using parts with tighter spacing, or lower standoff will most likely require multiple rounds of verification testing to ensure proper processing of the flux activators. As mentioned in previous columns, the product's end-use environment plays a very large role in reliability. This puts the focus on cleanliness after the assembly process.

When the lead pitch is reduced, lower levels of conductive residue are required to create electrical leakage paths. When discussing the end-use environment, the main parameter we look at is available atmospheric moisture.

The leakage fire triangle requires conductive residues, atmospheric moisture, and electrical bias. Of those three ingredients, the one that is easiest to control is the residues.

The reduction in component pitch puts a premium on cleanliness to reduce the risk of den-



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drite growth-related field returns. When processing with no-clean flux, the focus is on the thermal profile for ensuring that all flux activators are properly complexed with the activators outgassed as designed by the flux manufacturers. Conversely, when an aqueous wash process is used after assembly, it is important to be sure the process is fully removing all of the residues. If you are washing a water-soluble flux, any remaining residue will be conductive without question, and if washing no-clean flux, any remaining residue may or may not be conductive.

The reduction in component pitch puts a premium on cleanliness to reduce the risk of dendrite growth-related field returns.

Washing a no-clean flux is especially challenging when parts with tight pitch spacing are used because the outer shell of the flux can effectively create a dam between the leads and prohibit the wash solution from penetrating under the part as necessary to remove all the residues. Far too often, we see customers that had been using a water-soluble flux migrate over to a no-clean flux and use the same recipe that was previously effective without understanding the differences in the materials. The problem with that is the extra energy required to break through the outer resin shell that is created through the thermal excursion that is meant to help prohibit moisture from reaching any active residues.

If the process is only breaking down that outer shell, it will often leave behind the residues that were meant to be protected and can be just as conductive as water-soluble flux. This is why testing at the specific fine pitch component locations with ion chromatography is so important whether you are cleaning

or not. IC testing will yield data that tells you the type and amount of ionic content present. That tells you if you are at an increased risk of electrical leakage in the field. This all speaks to your product's reliability, which, of course, speaks to your company's bottom line and reputation.

Cleanliness is one of the most important aspects to consider when using these types of components but certainly not the only aspect. Another thing to consider is the paste printing process. When you print solder paste for these parts, there is an increased risk of bridging after reflow soldering. This can increase hand rework after reflow, and every time you subject your product to a human, you increase the risk of damage. When a machine is making a mistake, it will normally make that mistake repeatedly, and those types of issues are fairly easy to discover and fix.

When you send your assemblies to one of many operators in the rework area, the risk of one-off damage increases because it is much harder to control each operator's process. There may even be a need to evaluate the paste flux currently being used to determine if that is still a viable material for your process. All major flux manufacturers offer a range of options that specially address fine-pitch components, so if you need to make a change, there should be no shortage of materials available.

The bottom line, from my point of view regarding reliability on miniaturization, is the same as with any assembly process; you have to do the required chemical and environmental testing to determine if your assembly parameters are properly processing the chosen material set in a way that does not increase the risk of electrical leakage in the field. Now, we just need to work on a popcorn popper that fits in my other pocket. **SMT007**



Eric Camden is a lead investigator at Foresite Inc. To read past columns or contact Camden, [click here](#).

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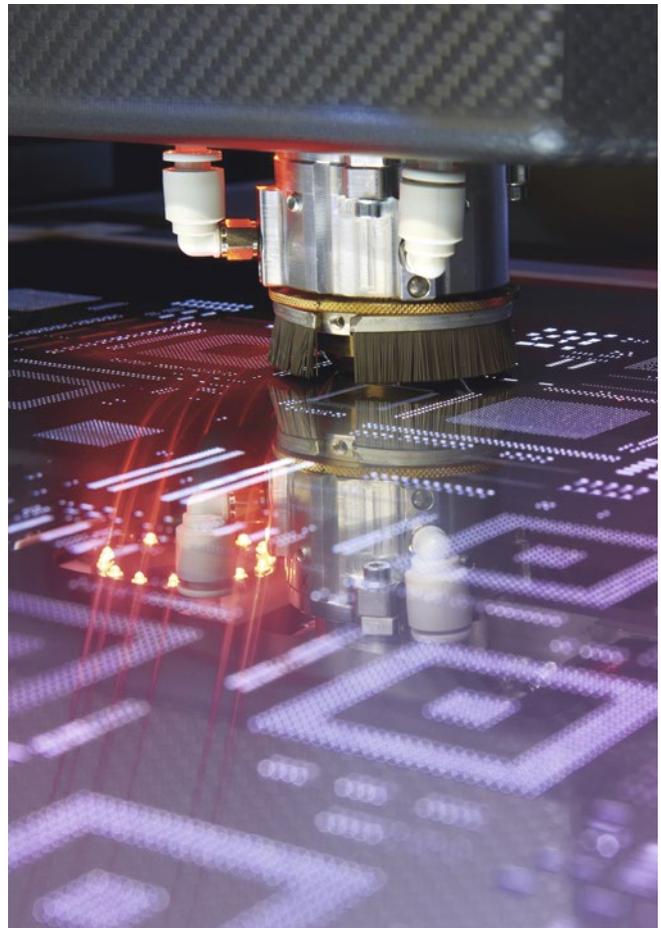
LPKF on Stencils and Depaneling

Feature Interview by the
I-Connect007 Editorial Team

Stephan Schmidt and Mirela Orlowski of LPKF Laser & Electronics North America discuss laser technology in cutting stencils and depaneling circuit boards as a factor in shrinking component sizes and why few people in the industry realize how much of an impact the stencil can have on the manufacturing line.

Nolan Johnson: There's a lot happening right now with smaller components, smaller step sizes between pads, smaller features on the boards, tight tolerances, as well as interfacing between the component and the board with the solder paste. What's your perspective on the challenges as an equipment manufacturer?

Stephan Schmidt: We have an impact on two sides of the assembly world. One side is the equipment for the depaneling of PCBs because this product is at the forefront of high miniaturization. It's used for challenging components and circuit boards that can't be done with the traditional technologies, such as routers and pizza cutters or manual depaneling situations. If you have small components that need high tolerances, that is not possible anymore with traditional mechanical separation methods.



We also have some impact on the stencil manufacturing side, where we manufacture laser systems to cut SMT solder paste stencils. The importance of the quality of those stencils is higher now than it ever was in the past. With the tolerances in PCBs being what they are, it can only be reasonably affected by the buyer of the circuit board, and it is important that the quality of the stencil not add any negative impact.

Especially with SMT components getting smaller and smaller, we need to get the solder paste in the right spot to avoid any shorts or bridges. Having an accurate stencil goes a long way. Some manufacturers that we've worked with in the past have looked into this carefully and understood how important the role a relatively inexpensive item, such as a regular solder paste stencil, has in their manufacturing yield.

Once they looked into this and understood how important those things were, they decided that only stencils with a certain quality can be used, and it made a big difference in the



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Stephan Schmidt

manufacturing process. They recognize that buying a stencil that's made on a high-quality machine versus one that is 20 years old and out of calibration makes a huge difference for them. It doesn't come down to saving \$10 on the cost of the stencil; it's about saving thousands of dollars in the manufacturing process by buying a quality tool that is reliable for manufacturing.

Johnson: Since you have laser technology involved, have you had to increase accuracy within your equipment, or have you been able to deliver the necessary cutting accuracy already? Where is the pain point right now?

Schmidt: Remember, we are not selling stencils; we are manufacturing the equipment that goes to produce the stencils. Many stencil shops have been, for the longest time, under enormous pressure for price. There was a big race to the bottom for the lowest stencil price of it because many stencil buyers didn't have enough of an awareness of how important the stencil is in their manufacturing process since it only costs \$200–500, depending on where you buy it.

Many stencil manufacturers don't necessarily have the research horsepower by themselves to convince the buyers how important the quality had to be for them. However, we have published a number of white papers to educate stencil buyers about the factors that impact the stencil quality.

Johnson: Do you see other manufacturers—not the stencil specialists—start to bring stencils in-house because of this?

Schmidt: Yes, we have some situations like this. I am surprised there aren't a lot more yet. I can

only explain this by a lack of enough awareness at the EMS companies to address that properly. If I were in charge of this, for something as important as a stencil, I would want to have full control over an important printing tool in my process. Manufacturing this in-house with a controlled quality environment is an inexpensive step to make that happen. Also, some companies have recognized that and brought this technology in-house. Others continue to purchase this on the open market.

Barry Matties: Why wouldn't they bring it in-house? What's the logic there?

Schmidt: In many cases, it's driven by price. It's an industry where some EMS companies say, "I buy the products in the market, and they seem to work for me." There's not a lot of research going on about why they should work or not work, so they continue on like this, but it's surprising. In an industry like this, you would think somebody would want to get end-to-end control over the quality of the tools they use for their manufacturing process to control quality tightly.

Matties: Today, utilizing the equipment should be pretty straightforward, as well.

Schmidt: Absolutely. It's easy to use. With modern equipment, you put a piece of sheet metal in a frame, select your artwork, press a button, and that's it. You have all the information that can be easily done from anywhere.

Johnson: They're already passing along the cost of the stencil to their customer when they're getting it outsourced. You can do the same thing with an in-house tool.

Schmidt: Exactly. Most EMS companies believe they don't use enough stencils to make it worth their while. They probably compare the total cost to buying from a stencil shop that makes stencils every day; therefore, they can offer stencils at a relatively low cost. At the same time, they might be giving up their full quality control, but by outsourcing it, there might be a gap in the quality control process.

Matties: Is this more of a regional strategy in North America versus Asia?

Schmidt: This is a worldwide situation. In some segments, we see EMS companies bring the stencil technology in-house, but the majority of them continue to purchase stencils on the open market. Again, with the higher level of miniaturization, it's more important than ever to have full control over every detail of the tolerances that can be controlled in such a process.

Matties: And time as well.

Schmidt: Yes, When the SMT line is down because the stencil is not there or because something needs to be recut for one reason or the other, that is at a significant cost, which can be avoided altogether by having access to those tools.

Matties: As you sell the tool, do you make recommendations for potential stencil utilization to the fabricators, or do buyers look to the stencil provider?

Schmidt: In many cases, we sell the tools mostly to stencil providers and stencil shops. Usually, the EMS companies are interested, and when they bring this in-house, they want to learn about the technology as well. They lean on us to learn about what parts can be controlled, and that they have the proper working environment with those machines.

Happy Holden: And what's the turnaround time for laser cut stencil by these providers?

Schmidt: Stencil providers are often a local business, and a lot of stencils are being cut at the last minute. They get the information from the EMS companies and drive these stencils out the same day to customers/users. Why would such an important part not be planned any more ahead of time? Why should this be a last-minute job? This leaves a lot of possibilities for quality being subpar.

Matties: I'm still surprised that this is not in-house.

Schmidt: It seems like it's an afterthought. Sometimes, people think, "Everything else is on the line. We need the stencil, too, so let's get that ordered because we can get it the same day and not worry about it as much."

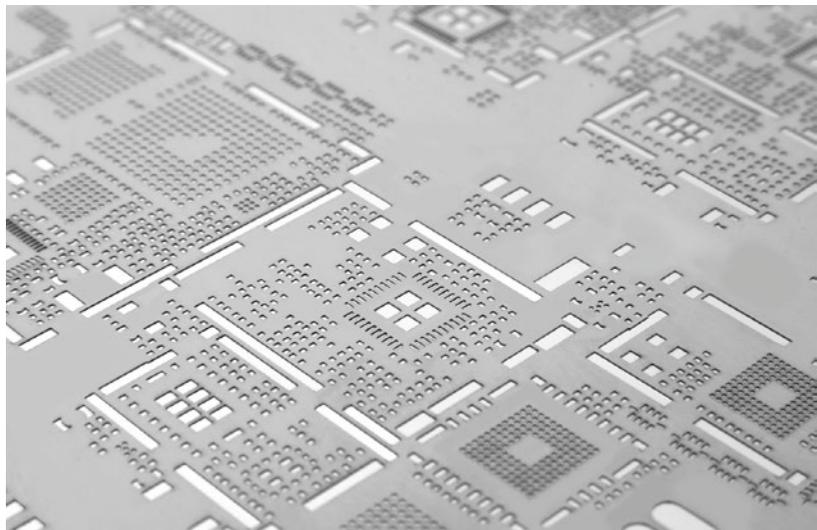
Matties: How expensive is your equipment?

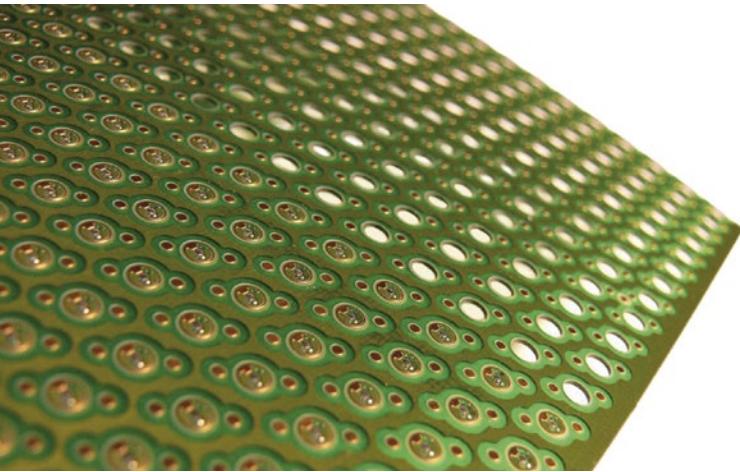
Schmidt: The equipment is designed for producing stencils very fast, so the stencil laser system typically costs between \$130,000 to a little over \$200,000.

Matties: They may wind up making more stencils every month if they had their own equipment.

Schmidt: Exactly. There are a lot of details in the electronics manufacturing process on how to design the stencils and maintain quality control. However, it's amazing how some OEMs or EMS companies do not pay all that much attention to those details. Some focus on it, and those are the successful companies. They understand the quality impact that a stencil has and demand certain quality standards being required in their supply chain.

Matties: In terms of cutting the stencil, are there different approaches to the geometry of the cut, or is it a single cut that's always the same?





Schmidt: In terms of the geometry, it is important that the system that cuts the stencil maintains the accuracy with tight tolerances. As I mentioned earlier, a lot of the circuit boards have come with larger tolerances in the first place. If you imagine you have a stencil system that creates additional tolerances and if those tolerances go in the opposite directions, all of a sudden, you're printing next to your pad and not on your pad anymore, especially with very small components. If the stencil is at the end of the line, it can't add any tolerances, and there are much higher tolerance requirements to the stencil than there ever are on the circuit boards itself because those come with certain tolerances in the first place.

Matties: As we see finer and finer pitch, it seems like maybe the stencil will soon become more of an issue, and we'll see more EMS companies wanting to bring it in-house.

Schmidt: We expect to see that through increased awareness of how important the stencil is, and that it can be produced in a well-controlled environment. Large EMS companies have that type of capability, and they're aware of the importance of the manufacturing procedures so that they don't leave anything up to chance. Having a stencil cutting system in that environment would guarantee the same quality every time.

Matties: And the cost of a stencil from a provider must be pretty affordable as well. Unless

there is a pain point there, there's little motivation to move off of it.

Schmidt: Right.

Matties: You mentioned some EMS companies cutting one stencil a week or something like that. How did you make your case?

Mirela Orlowski: If you need only one stencil a week, you do not need a stencil laser in-house. In that case, you would work with a stencil service supplier. But if you need larger quantities of stencils, it can make sense to bring the entire process in-house to save cost and to control the manufacturing process end-to-end.

Matties: Where is the crossover point on your ROI matrix?

Schmidt: It depends on the exact cost for the buyer, but typically in the area of three to five stencils a day, they can easily make this cost model work. If they look at all the different costs that are around manufacturing a stencil, they would see immediate improvement.

There are two parts. One is the ROI to purchase their own equipment for the EMS or OEM, but the secondary issue, which is more worrisome and requires more industry education, and that is the general awareness of how important quality stencils are in the first place. Even if somebody only buys a handful of stencils a week, they may not need to have their own equipment for this, but they should have a vested and well-managed interest in how the stencil is manufactured, including to what standards.

Johnson: Even if you don't want to go in-house, make sure that you know a lot about what your stencil provider is doing.

Schmidt: Correct. When you call Uber, you want a qualified driver, not somebody who got their driver's license last week and didn't make the insurance payment for their car. As a consumer, we should be educated about the service that we have been provided, and it's important



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for any stencil buyer to be educated about this whole thing. It's surprising how much of the focus is on price rather than quality control.

Johnson: What should an EMS provider ask their stencil vendor?

Schmidt: An EMS provider should ask the provider what quality tolerance they provide in the first place and what type of equipment they use because many stencil providers have a variety of different systems in operation. If I were a buyer, I would want to make sure my stencils are always made on a certain piece of equipment with a specific quality standard since different systems come with varying quality levels.

The secondary issue is how the data is being managed. Is the data being manipulated after it's being transferred to the provider for "optimization" that the EMS company may or may not have any influence on? Or is the data is fully under control of the EMS company and not being changed by the stencil supplier? These are things that the EMS companies should have a vested interest in.

Holden: Do you have a machine that could both depanel boards and cut stencils?

Schmidt: No, those are two different processes. Stencils are a tool for the beginning of the line, and then we have a depaneling machine that's at the end of the assembly line. They use different methods. Although they both use lasers, that's the only general thing that they have in common. That's where the similarities end.

Holden: It would be nice if there was one machine that did both because the stencils are kind of at the beginning of the process, and if the machines at the end do depaneling, then it would be pretty high payback in terms of the active use of the machine.

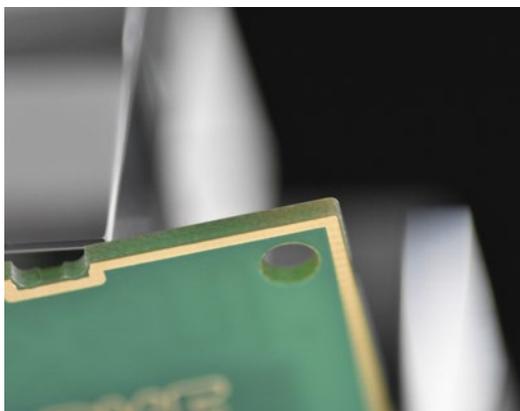
Schmidt: Absolutely. However, the challenge that we have with this is a laser that's a specific tool. The lasers that are used for cutting stencils and metals fast with high qualities use a different process. That process is called the melt and blow process. This is the technology that's being used for cutting sheet metals versus the cutting and depaneling of circuit boards, where we use an ablation process. It's like a chainsaw and a paring knife; they can both cut things, but they have different designs for each specific purpose to be efficient in that field.

Johnson: There's a lot of motion right now in materials. What challenges does that present to you?

Schmidt: On the materials side, there are a bunch of new materials, but lasers are well-suited to manage them. Both the materials and dimensions are becoming extremely challenging. If you deal with pre-routed materials, for example, cutting out breakout tabs is becoming difficult when you have small devices or devices with a lot of sensors. More and more devices have sensors these days. You cannot

use brute force to pry something out of a panel anymore; you have to use something that's a lot more gentle and doesn't leave a lot of side effects. Tolerances are extremely important as well because not adhering to a tolerance leads to not getting your small parts into small housings.

Today's PCBs have to be made to extreme standards that we couldn't even imagine 10 years ago. There's a lot happening on the materials side, especially with RF and wireless communication. Again, lasers can deal with that well. We are addressing this through different lasers because not every laser can do everything, and they have different strengths and weaknesses. We can process different materials with different laser wavelengths and pulse length very carefully.



Matties: Has LPKF looked at an ROI for a typical North American EMS facility to have in-house laser cutting? If so, what are your findings, generally speaking?

Schmidt: We do that a lot. Let me draw a little bit wider circle around this whole thing. There's a couple of things that are interesting, and we deal with a little similar situation as we have with stencils. For the direct ROI, comparing a method that separates the circuit board of the panel is one piece of the cost, which is everyone's focus. You have a pair of pliers or a laser cutter, and the laser may not appear cost-effective there.

However, when you look at yield, it goes a long way, and when you consider environmental management, then it goes even further. For example, when you use router systems or saws, the amount of the work and money that has to be spent for the mitigation of the airborne dust in the plant is quite significant, not only for the protection of the workers but also for the protection of the sensitive components—especially optical sensors or other sensors on boards that are easily affected by airborne dust.

The other element is vibration. Using a violent method to pry a highly sensitive circuit board out of a panel creates significant yield issues by vibrating the board, especially if you have a lot of sensors on a board, which can easily be affected by it. These things should be considered for ROI, as well. Speed is another one that we addressed with ROI. Modern depaneling laser systems are on par with mechanical routers when it comes to speed. That is a big step forward from the past 10 years when lasers were only used in boutique applications for thin circuit boards that couldn't be manufactured any other way.

Nowadays, it's becoming a lot more attractive for mainstream applications because the throughput is on par with mechanical depaneling methods. At the same time, you can get a much higher yield. And you can forego all the dust mitigation issues in the plant, which are often substantial.

Matties: And cutting tools.

Holden: One expert mentioned the growth of cavities. Are your lasers used to do micro-machining of circuit boards?

Orlowski: We encounter more and more of those applications now. The beauty of a laser as a tool in general, especially lasers and wavelengths used for the depaneling,

is that they work well for high-mix environments, both on the material and application side. Not only are you able to use the same tool to easily process different types of materials by changing the parameters on the machine, but you can also use the same tool easily for a different application. You can use the same tool to cut, drill, create pockets, etc. This is one of the positive aspects of a laser, especially in the North American market, which is high mix in terms of application and materials. This is one of the big advantages of a laser as opposed to a mechanical method.

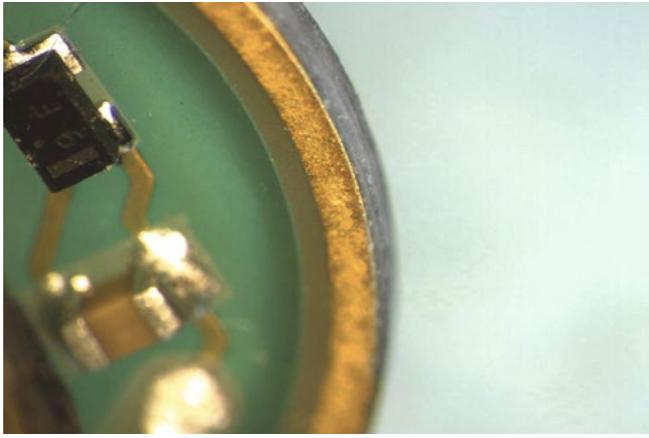
Johnson: How does your equipment fit into the infrastructure for CFX Hermes digital factory?

Schmidt: Our equipment directly integrates with manufacturing execution systems, especially on the paneling side. We can read data codes or barcodes with the laser machines, and even write barcodes on boards. We can also depanel certain boards inside a panel. For example, if specific boards are being already identified as not functioning before they even come to the depaneling process, then those can be automatically skipped to save production time. Our process is fully integrated with a modern manufacturing execution system environment.

Johnson: That's an application I wouldn't have considered. You can leave the failed boards right there in the panel and not even bother with them.



Mirela Orlowski



Schmidt: Correct. It's all about efficiency. When it comes to medical manufacturing, it's also important that we have a complete collection of the cutting data so that boards can be traced back to what machine the board is being cut on, what laser power is being used, etc.

Orlowski: If you're cutting maybe 300–400 parts per panel, it saves quite a bit of on throughput if you are able to avoid cutting bad parts altogether. If you have a high volume of parts in a panel, the ability to skip bad boards is valuable.

Johnson: That also makes it easy to show your customers where the real issues are. Wrapping up, what are the other common issues that need attention with customers?

Schmidt: The tolerance is an important part, as well as the fiducial recognition or overall positioning systems, especially in the depaneling world. Again, a lot of boards come in pre-routed, which means you have an artwork that has gone through photo process and chemical etching. Then, you have the routing channel, which is made on mechanical routers. Two completely different platforms and the depaneling machine have to negotiate the tolerances of these two different platforms to create an optimal result. You want to create a board that is cut in the correct outside dimension, but also make sure there are no tips left over at the breakout tabs so that the small parts fit in challenging housing or packaging. It is important that a depaneling system has superior optical

positioning systems that can look at both the artwork on the circuit board itself as well as all the mechanical pre-routed parts on it.

Orlowski: Another thing that I would like to reiterate is that the market still needs some education about laser tools for depaneling in general. We still run into quite a few companies that believe that the depaneling tools are only used for thin flex parts. That was the case as Stephan said maybe 10 years ago, and they have evolved quite a bit over time. Right now, depaneling lasers are most popular for your standard 62-mil FR-4 board, which is still the majority of electronic manufacturing. It's an important message to make that the lasers have come a long way, and they're capable of depaneling or drilling a wide range of materials and thicknesses.

Schmidt: Since laser depaneling is a relatively young industry, it's not like routing or injection molding that people know pretty much everything that there is to know. Laser depaneling is new technology and has been damaged by multiple companies' attempts in the past to use cheap, high-power CO₂ lasers to burn the boards and separate them this way. That created a negative impression of laser depaneling—that it's dirty, expensive, and not for anybody. Because people who looked into this in the early days of the CO₂ lasers, the results were horrific, so it's no wonder that some people would dismiss laser depaneling altogether.

This has changed fundamentally, especially over the past few years. The technology has progressed so substantially with completely different laser technologies that are extremely clean, and highly precise, especially for small parts. It's cost-effective for thicker boards and cutting longer lines. We have plenty of applications for the entire board is being cut by a laser, so there's no more pre-routing necessary at all. That saves space on the panel itself. The laser is much smaller than a mechanical router bit—8-mil diameter, for instance. You save a lot of real estate by putting everything on the same panel and letting the laser do the job. More awareness is needed that lasers have come a

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long way since early lasers tried to blast through circuit boards.

Matties: You have seen a shift in the past couple of years. What do you see in the future for lasers?

Schmidt: They're going to be faster, cleaner, gentler, and even more accurate. The same trajectory that we're on right now will continue for some time. Laser technology continues to be developed, and there are completely new lasers available right now in the lab. Ten years from now, we're probably going to have them in manufacturing systems at reasonable prices. We see short-pulse lasers starting to become available at reasonable cost levels that nobody could touch in a manufacturing environment five years ago. Today, they are reasonably inexpensive and produce at different quality levels that we couldn't reach with other lasers in the past. There's a lot more to come on the laser side.

Matties: You're saying productivity is on par with mechanical, but the advantage of the environment and other variables make the laser a better choice and more accurate.

Schmidt: Correct. We're going to get much tighter tolerances and a much more gentle process in terms of mechanical impacts, such as vibration, and much cleaner in terms of contamination. Contamination is a huge factor that is not considered by many manufacturers. They live with the yield that they have, often not realizing that this can all be mitigated by going to a laser instead of cleaning the air. How about not creating dust contamination in the first place?

Matties: And if the speed is on par or better, then what's the delay?

Orlowski: The trend is changing a bit because manufacturers realize that the speed of the lasers is often on par with the routers now. By switching to lasers, they can eliminate their

entire post-process cleaning when it comes to the debris on top of the board. Coming back to the ROI, you should not compare your router price with your laser price. Instead, you should compare your router cost plus your tooling and cost for post-process cleaning with the cost of laser. There's quite a bit of difference there.

Holden: We've been publishing articles about a new high-density construction called the vertical conducting system, or VECS. Instead of creating a hole, it creates a trench and uses the sidewall and treads to connect to inner layers.

They use a mechanical router, but it would seem that with the right kind of laser, you would be much more efficient and precise than a mechanic router.

Schmidt: Yes. A laser would be able to process this more selectively and with higher resolution.

Matties: Lasers have impacted the industry on a large scale, and will continue to do so in many ways.

Schmidt: It's a big field, and lasers can do many amazing things; they all are a little specialized. Lasers are not good at everything; instead, they have specific purposes. It's not the one-size-fits-all solution; that's long gone, and I don't think it's ever going to come back.

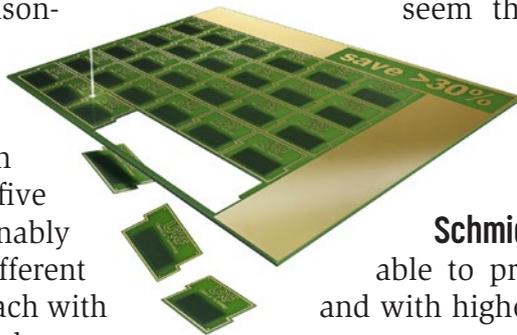
Orlowski: Because they're able to produce much better results. That's the key.

Schmidt: Exactly.

Matties: Very interesting. We appreciate your time and expertise.

Schmidt: Thanks again for talking to us about this. We are happy to help.

Orlowski: Thank you. SMT007





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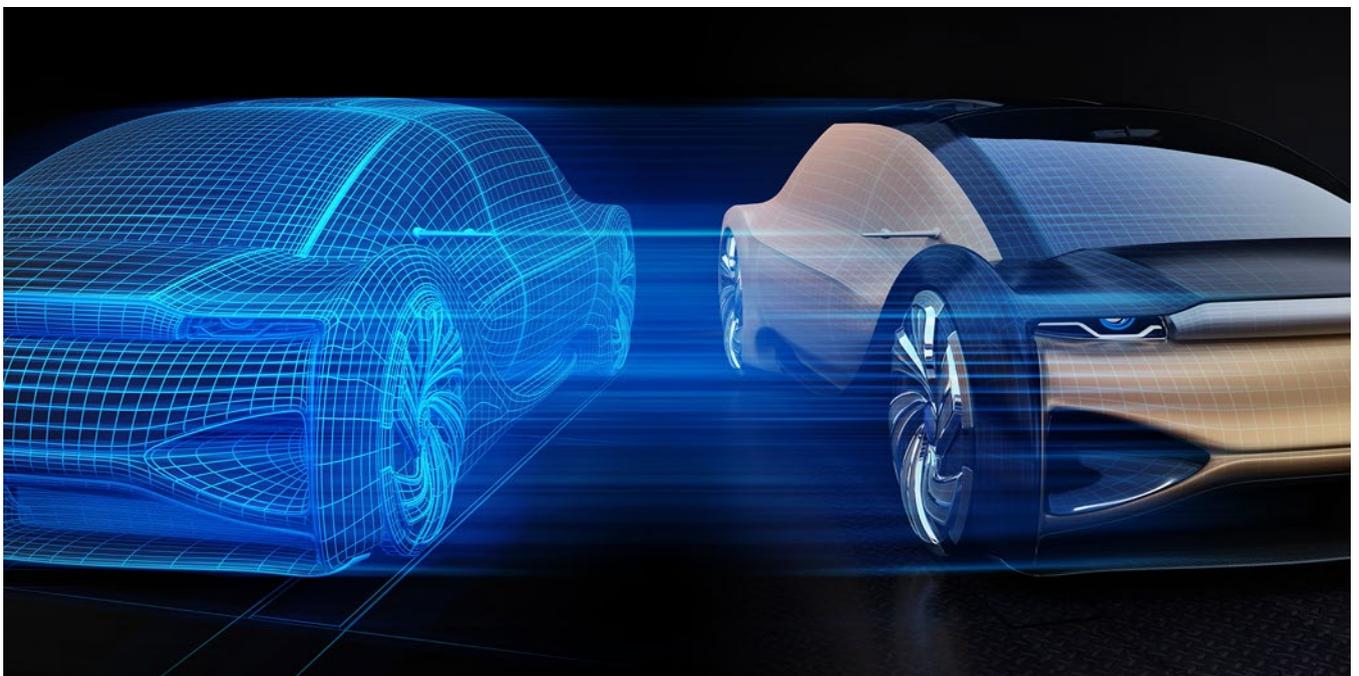
Size Matters: The Digital Twin

Smart Factory Insights
Feature Column by Michael Ford, AEGIS SOFTWARE

In the electronics manufacturing space, at least, less is more. There are a whole plethora of reasons that have been driving down the size of electronic assemblies for many years—a trend which shows no sign of diminishing. The price we all have to pay as electronics manufacturers is not trivial, as existing paradigms of assembly, inspection, test, and quality control are challenged to the extreme. The digital twin is supposedly the new paradigm, yet—as with many things these days—the term has already been abused by various marketing teams to promote many disparate products and bespoke technologies, causing confusion, which stifles progress. Let’s consider what the true digital twin is really all about—including the components, uses, and benefits—and see that it is not just an excuse to show some cool 3D graphics.

Size Matters

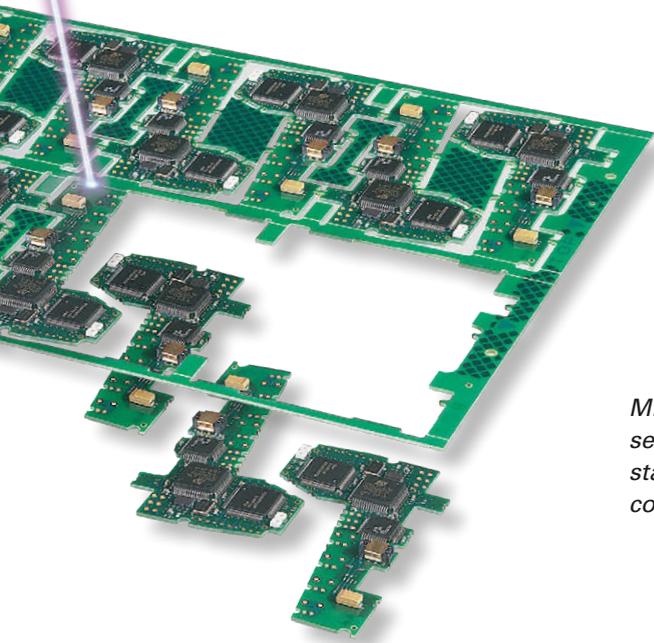
Miniaturization, in one form or another, has led the way competitively between OEMs of key consumer devices—a phenomenon that has now stretched across the whole industry. The trend started back in the 1980s when portable consumer devices first appeared, and rivalries between the giant consumer device manufacturers became public. One great example was the launch in Tokyo by Sharp, who launched their smallest ever mini-disc player to huge media accolades. Attending the event was Sony’s president at the time, Norio Ohga, who—when asked about his reaction to Sharp having the smallest player in the world—took out of his shirt pocket what appeared to be a prototype of a player half the size, and said, “I don’t think so.”



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Though with less fanfare, perhaps, the reducing size of electronics has been a continuous pursuit. It is not just a matter of being stylish and easy to carry. Sophisticated electronic controllers are now being integrated and embedded into the majority of everything that we own or use, including phones, energy meters, automotive intelligence, and military and space technology. There are many other factors apart from size itself that are important, including the weight; the space required for storage and transportation related to packaging; the amount of material consumption, especially for key materials for which there is a finite supply; the energy consumption of the device, including the safety of power supplies—especially batteries; and the physical strength of the device in terms of protection for example of an automotive module involved in a collision.

Size matters are clearly not a new challenge, but we do appear to have reached the point of diminishing return where the refinement of existing processes for the manufacturing and assembly of electronics-based devices—as well as integration of electronic assemblies into more mechanical products—when dealing with the practical aspects of size. Rather than further incremental change, the industry needs to take a step forward.

Rather than further incremental change, the industry needs to take a step forward.

It Starts With Design

In the design world, the issue of reducing the size of designs is really not an issue of their domain. In any design work being performed, the designer can simply zoom in, and everything looks the same as before. The physical world does not allow such luxury, as there are some very specific constraints, which the designer later experiences as they run their design for manufacturing (DFM) tests. Many assumptions

and decisions are typically made in the virtual world of design that either need extensive re-evaluation or could be missed, the ramifications of which come to light only during the physical realization of the product. The problems then translate into production issues, where test points cannot be physically accessed, for example, such that assembly confirmation cannot be done completely, representing a risk of defects appearing in the market.

There are so many well-known examples of challenges within manufacturing as the size of products decreases, and hence the density of components increases, including stencil creation, component placement, soldering, as well as test and inspection. Most issues in manufacturing are size-related. Though automation has been developed to follow the trend of miniaturization, unfortunately, with humans, the trend has, if anything, been the reverse. More and more traditional assembly tasks have become impossible to execute through manual assembly, such that they become the target of specialist robotic assembly or require the need for specialist tools and equipment. The effect of all of these challenges is simply an increase in the cost and lead-time for assembly, which is not good news in a highly competitive industry.

Beyond manufacturing, the reliability of products in the market is also affected, as smaller product sizes make it more difficult to dissipate heat effectively, for instance. The smaller sizes of components also means less tolerance to unusual conditions, such as overvoltage. Life expectancy may be limited in many cases.

The Role of the Digital Twin

The development of digital tools for design, together with the subsequent flow of data to manufacturing and the many tools that are then required to execute manufacturing, have been quite removed from the world in which they work, with no concept of evaluating the physical result of what they are doing. This connection is vital. Without it, it is on a par with a media company creating television programs without understanding what audiences like.

The definition of the digital twin goes beyond the simple gathering of data related to product

design, manufacturing, and operation. It is the reconciliation of physical and virtual worlds such that the manipulation and use of data are done in the precise context of the physical constraints. This includes not only the product itself, but also all materials, tools, machines, and processes used throughout the life cycle of the product, as well as environmental aspects such as temperatures, pressure, energy supplies, and physical stresses and strains to which the product may be subjected.

The Use of the Digital Twin

The true digital twin, therefore, is inclusive of a vast array and architecture of technologies, all of which are represented through data, available to any application that wishes to be a part of the new paradigm of digital manufacturing. At the highest level, we can see the point at which a corporate business manager will simply select a digital product model on his screen, and then drag and drop it into a digital assembly model of a line or factory. This will automatically determine and show the capability, delivery, timing, and cost of manufacturing with many layers of software (likely from many different vendors)—including IIoT-driven MES and machine vendors—working seamlessly together to model the physical and digital world.

Designers no longer need to depend on static design-rules, but can seamlessly understand the effects of producibility and product reliability as they perform the original design. In manufacturing, rather than the dependence on the physical analysis of the product to determine production configuration parameters, they can be set based on the digital model without a doubt that constraints of the actual equipment, materials, and tools selected have been taken into account. This is just as well, as any form of manual intervention in the equipment programming or engineering processes can no longer be reliably made based on the physical domain alone as product sizes decrease, and component densities increase.

The Realization of the Digital Twin

The practical ways forward towards the real digital twin have already started. The IPC-2581

Digital Product Model (DPMX), for example, is a mature and successful way to model the complete electrical design of a PCB in a single simple file. The JEDEC JEP-30 standard is a new way to model components in three dimensions, including temperature profiles, specifications, and tolerances. The IPC Connected Factory Exchange (CFX) standard promotes open IIoT-driven communication amongst machines and systems, orchestrated by the IIoT-based MES platform—which is essential as the connectivity required for the digital twin to be inclusive of all components—without the need any longer for hundreds of millions of dollars to be spent throughout the industry on bespoke connections.

The true digital twin will encompass all of these existing technologies and expand its purview to include such things as mechanical design, robot simulation, and reliability performance. These elements are not solutions or proprietary, nor do they belong to any one vendor, but they define the environment in which solutions from many different vendors can work together.

What Can I Do?

For the vast majority of people in the industry, it is important to understand the true scope of what is happening and judge solutions as they are marketed based on the knowledge of what has to happen to make the transition from separated physical management and digital management into becoming the true digital twin that combines both. For those adventurous enough to want to contribute to the creation of a digital twin standard or simply understand more about what the true digital twin is about, IPC has just started such an initiative, which will quickly develop into the necessary guidance for what must happen in the industry to make the step-change required in our miniaturizing world. **SMT007**



Michael Ford is the senior director of emerging industry strategy for Aegis Software. To read past columns or contact Ford, [click here](#).

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NVIDIA's AI Edge Innovation Center, a first for this year's Mobile World Congress in Barcelona, will put attendees at the intersection of AI, 5G, and edge computing.

New Reliefband Wearable Devices Unveiled at CES 2020 ▶

Reliefband Technologies LLC, an innovator in wearable technology that prevents and treats nausea and vomiting symptoms, announced new Reliefband® Travel and Reliefband® Sport wearable therapeutic devices.

Rogers Communications and University of Waterloo Partner for 5G Tech ▶

Rogers Communications and the University of Waterloo joined in a three-year, multi-million dollar partnership agreement to advance 5G research in the Toronto-Waterloo tech corridor. Together, they will create the first 5G smart campus in central Canada.

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Fourteenth Air Force Redesignated as Space Operations Command ▶

By order of Secretary of the Air Force Barbara M. Barrett, effective December 20, the 14th Air Force was officially redesignated as Space Operations Command.

NIU Launches the Future of Urban Electric Motorcycles—5G Connected, Autonomous and Self-Balancing ▶

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Evolving Solder Capabilities for Shrinking Components



Feature Interview by the I-Connect007 Editorial Team

Taiyo's Yuya Suzuki, marketing manager for IC packaging materials, talks with Nolan Johnson and Dan Feinberg about the challenges with soldering due to shrinking components and how Taiyo's R&D work around smaller filler sizes and increased planarity has been preparing them for the future of solder mask.

Nolan Johnson: Shrinking components and smaller feature sizes are creating a need for increased precision in all aspects of the component attachment processes. For Taiyo and its products, what research and development work are you doing to meet these tighter tolerances that are increasingly showing up in stencils and solder paste application?

Yuya Suzuki: Screen printing is the major process for coating or caulking the photoresist. But as the thickness control and tolerance are going to be smaller, some people—especially in the IC packaging area, where they already had a similar issue 10 years ago—lean toward

spray coating or other methods. At that point, the viscosity of the photoresist was still compatible with new coating processes. Another way Taiyo needed to tailor our solder resist ink was by changing the filler size. The thickness of the solder resist that can be coatable on top of a circuit board is defined by the filler size, so we are moving toward the smaller filler size, usually tens of micrometers. That is the first step we have taken to accommodate such requirements.

Johnson: What effect do these changes produce that can improve yield?

Suzuki: By changing the filler size, we can guarantee that we can accommodate the inner coating capability. It allows the customer to have better thickness tolerance and better reliability for assembly.

Johnson: Is the trend toward thinner coatings?

Suzuki: Yes.

Johnson: Because it's thinner and going to be more planar.



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Suzuki: Right. And for better planarity, Taiyo has developed a dry-film solder resist that isn't liquid anymore.

Dan Feinberg: Is the primary volume that your customers use still screen print?

Suzuki: That is correct.

Feinberg: They screen the product to apply the image. Do you sell photo-definable solder mask that's liquid or dry film?

Suzuki: Most of our customers still use liquid photo-definable solder mask.

Feinberg: Is the developer you use solvent or aqueous?

Suzuki: It's aqueous.

Feinberg: Very good. Chemically, there's not much difference between the liquid and dry film. It's a case of how it is applied and the way it's manufactured. As far as the thickness of the dry film, what is the average thickness that you sell?

Suzuki: The standard thickness is 10–35 microns in thickness. The direction-type materials are used only for the IC packaging area right now, where the form factor is a much thinner, and the wiring is thinner.

Feinberg: And you need a higher resolution.

Suzuki: Exactly.

Feinberg: What kind of definition can you get as far as lines and spaces with your average dry film, which is probably mid-range?

Suzuki: Our definition and resolution are defined by the opening size. With the dry film resolution solder resist, the opening sizes

are typically 50–80 microns. Resolution wise, there's not a big difference between the liquid and dry film types as long, as you're not going to look at something less than 50 microns. You don't see a big difference between the liquid and dry film in terms of the variation.



Feinberg: Do those that use your dry film use it for tenting over holes?

Suzuki: So far, nobody has used it for tenting. Similar to liquid, the dry film can flow in between the lines, but the biggest difference is the planarity of the surface after the coating, or in the case of the dry film, it's lamination. In the case of the liquid, the conformity of the coating covers the surface of the copper wiring. The surface has a good roughness, but with the lamination, there is a pressing process that planarizes the surface.

Feinberg: Do you apply the dry film solder mask with a hot roll laminator?

Suzuki: Some use hot roll laminators, but many are using vacuum laminators.

Feinberg: You apply it in sheet form and then laminate it on with a press laminator.

Suzuki: Yes.

Feinberg: You also have a lot of sales in Japan. Does your product have a decent market share in China?

Suzuki: Most of our dry solder resist is sold in Japan, Taiwan, and Korea. We've started promoting it in China right now, but the packaging market is mainly dominated by those three major areas.

Feinberg: We see manufacturing coming back from China to the U.S., but we'll see what happens.

Suzuki: At the same time, China is trying to develop new technology.

Feinberg: What do you see for the future of solder mask? What would you like to see as the next innovation or improvement?

Suzuki: There are a lot of different versions of the packaging, and the PCB area is evolving right now with HDI and high-density. It also evolved to SLP substrate PCBs. So far, we have dry-film material for the IC packaging, and that's only the form factor, but if we would like to apply the dry film material toward PCB-type applications, we need it to be thicker and keep the good resolution at the thicker form factor. Right now, we have no good capability for making the thicker film material. Thicker film with higher capability is one direction, and another is high temperature and high voltage resistance. A lot of companies are moving that direction in terms of automotive, autonomous vehicles, and industrial applications.

Feinberg: One other thing that we were always fighting to improve was the geometry of the sidewalls, especially the sidewall after exposure and development. We tried to get very straight sidewalls but with a little bit of a curve outward at the very bottom to help enhance adhesion; of course, you would need a scanning electron microscope to see it. Is that something that you're still working toward, or are the sidewalls adequate with what you're doing?

Suzuki: That requires not only ourselves but our customers on the process establishment, but that is one direction we need to move toward.

Feinberg: Chemically, it was always a challenge for my research people to get the correct geometries on the sidewalls and still maintain good exposure rates.

Suzuki: And a good exposure speed.

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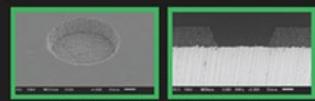
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Feinberg: What frequency of light exposure?

Suzuki: 365 nm.

Feinberg: I see some movement toward additive circuits. Additive manufacturing has been around since the '60s, but it never took off. Now, with the demand for finer lines and more components, there is one company, in particular, that's doing some amazing work on additive with 3D printing. Do you see any kind of movement toward additive circuits yet in Japan, Korea, or Taiwan?

Suzuki: In Asia, the trend toward additives is not there yet. But there is movement toward the inkjet-type photoresist, and we already have some interest from our customers about that. So far, Europe has the highest interest in terms of additive manufacturing, as well as the U.S.

Feinberg: There are some advantages, but when we were doing 20-mil lines and spaces, it didn't matter. Now, it's a tiny fraction of that, especially with all the portable devices.

There's some work being done on additive manufacturing, not only of the circuits but also of the passive components and being able to additively manufacture dielectric conductor resistors and capacitors. It's interesting. I'm wondering whether those are going to be components, or is it going to be the entire device? It's something we probably won't know some years yet.

Suzuki: Right. That's why we have a lot of SiP research and development in a variety of companies.

Johnson: As the tolerances become so tight, do you foresee a point where solder mask will need to be so precise in terms of registration that another technology will need to be deployed?

Suzuki: One answer, as a solder resist maker, is high resolution. Again, high resolution always gives you better tolerance in terms of the pattern and size. Another direction is positional accuracy, which depends on the tool and how

well they can compensate for the location of the original design versus the real panel. Cooperation between the material makers, like Taiyo, and the tool makers is very critical.

Johnson: The challenge is not with your product but with the equipment being used.

Suzuki: Exactly. Both approaches need to be taken.

Johnson: And that comes down to mechanical characteristics like stepper motor granularity and such.

Suzuki: Correct. The positional accuracy of the PCB itself has a lot of impact on that, too. Other than the solder resist, the PCB has a great impact.

Johnson: That makes sense. Thank you very much for your time.

Suzuki: Thank you for the invitation. SMT007

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Dealing With Package Parasitics

SMT Solver

by Ray Prasad, RAY PRASAD CONSULTANCY GROUP

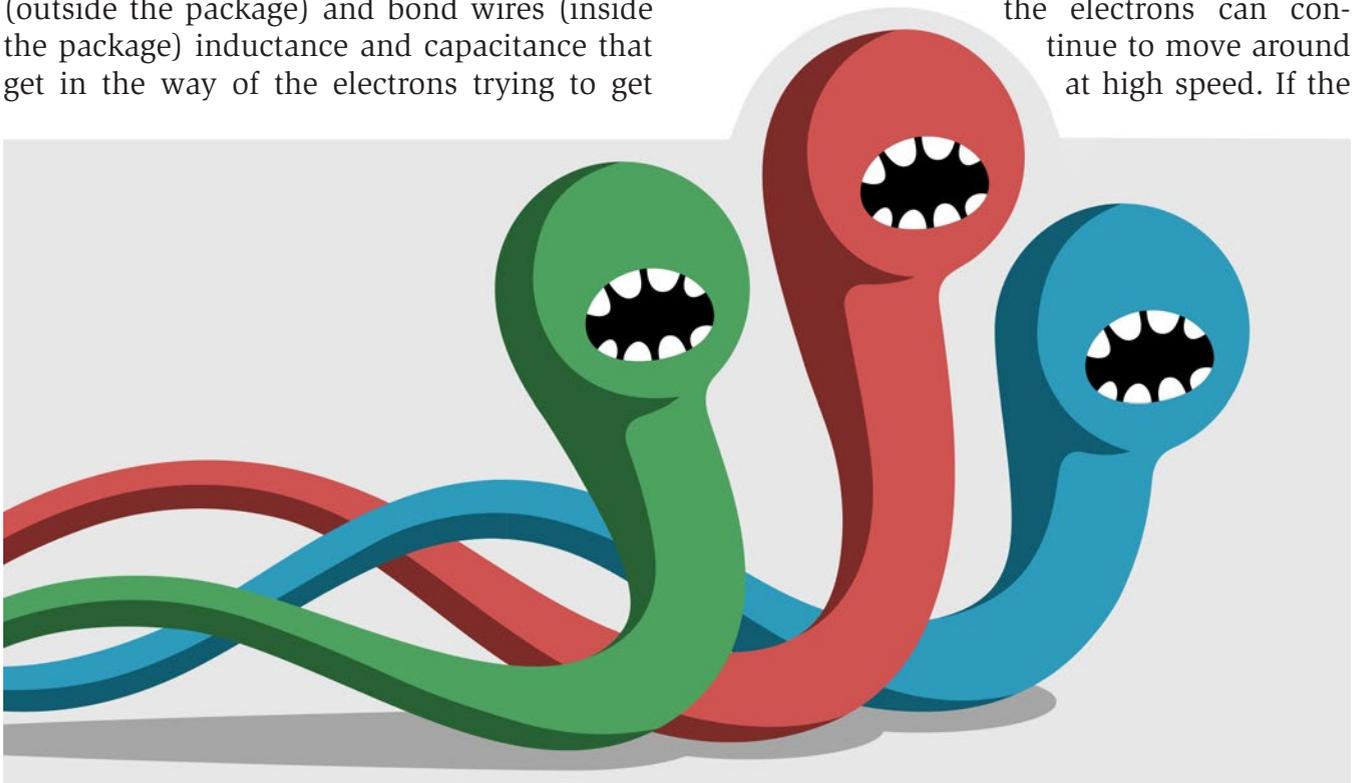
Packaging technology has constantly evolved over the decades from through-hole package to SMT with ever-decreasing pitches. There are many factors that play a role in the selection of a package, such as their cost and physical size, but the role package parasitics play in package selection has not changed over many decades. For example, while the silicon designer is preoccupied with performance issues in picoseconds, the system designer is still struggling with performance issues in nanoseconds. This 1000X reduction in performance is caused by packages that house the silicon commonly referred to as package parasitics, and they are very different in various types of packages.

Package parasitics are those undesired lead (outside the package) and bond wires (inside the package) inductance and capacitance that get in the way of the electrons trying to get

to their destinations fast. Electrons are a hurried bunch and like to travel at the speed of light. But they are being slowed by package parasitics. Why do we need to deal with packages, especially if they act like a parasite? Can't we just get rid of those packages? Why bother with parasites?

To answer this question, we need to ask the next logical question: What do these packages do besides behave like parasites? They do some very useful things. For example, the packages provide power to the silicon so that the electrons can move around. These electrons are always in a hurry, and their fast movement generates lots of heat. The packages make it possible to dissipate and remove that heat so that

the electrons can continue to move around at high speed. If the



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heat is not dissipated adequately, the higher junction temperature (temperature of silicon) will slow the electrons down. In a way, the packages make it possible to speed things up.

This is not all the good things that the packages do. They also make it possible to interconnect the signals of all the silicon on the board so that the electrons can all talk to each other. Last, but not least, they provide a safe shelter to the silicon. Being homeless is no fun for the silicon, especially if the environment around it is full of humidity and heat. A balanced way to think about a package may be that even though they slow the electrons down because of the capacitance and inductance of their leads and wire bonds, the packages also provide useful functions, such as powering, interconnecting, and shelter for the safety and comfort of its inhabitant—the silicon inside.

Despite the good things the packages do, many designers are trying to get rid of them anyway because they don't like any degradation in silicon's performance.

Despite the good things the packages do, many designers are trying to get rid of them anyway because they don't like any degradation in silicon's performance. One can get rid of the package by using bare silicon. Bare silicon is generally used as chip-on-board (COB) or flip-chip. There are some real differences in these terms. The COB term is used when the silicon is either wire bonded to the board directly or is used in the form of tape-automated bonding (TAB). However, chip and wire and TAB add wire-bond inductance. The highest performance is achieved when the bare silicon is directly flipped over and bonded to the

underlying substrate. No wire bonds or leads are involved in the flip-chip process.

One can achieve higher performance with bare chips when using them as chip and wire or flip-chip, but you create one major new problem. We should note that in addition to the package functions mentioned earlier, the packages also allow the pretesting of silicon before being soldered to the board. Out of all the multiple chips on the board, it takes only one bad silicon to render the entire assembly worthless. To correct the problem, you have to remove and replace the bad silicon, but reworking bare silicon on a substrate is not a piece of cake. On the other hand, if the silicon is housed in a package, the test sockets, and the whole burn-in and test infrastructure, are in place to enable the use of only functional silicon.

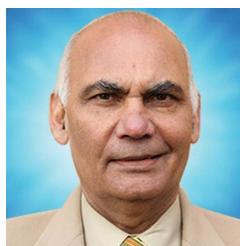
This issue of not being able to test bare silicon is referred to as a “known good die” (KGD) problem. It is not easy to test a bare die, although the industry has made good progress in this area. If that silicon is housed in a package (or used as a TAB device), the problem of using bad silicon does not arise. If you insist on using the bare silicon to achieve the performance you need, you can use flip-chip but must be willing to pay a higher cost in terms of more rejects due to a KGD problem. It is possible to achieve better performance if one is willing to pay a higher cost. There are certainly applications where it is worthwhile to pay a higher cost to achieve the needed performance, but it is generally in niche applications, such as multichip modules (MCM).

The solution for the industry may not be necessary for getting rid of the package but developing more efficient packages that can perform the traditional function of the package of protecting, powering, interconnecting, and providing a KGD without a significant penalty in performance. However, if you look at the R&D budget and effort on package versus silicon, there is no comparison. All the dollars are going into silicon development. We need that progress in silicon technology, but you cannot achieve the highest performance with a poor package. While we may not be able to get rid of package parasitics entirely, we are on

the constant hunt for minimizing package parasitics when we transition from through-hole to SMT, fine-pitch, ball-grid array (BGA), chip-scale package (CSP), bottom-terminated component (BTC), and bare or flip-chip with no package at all with the inherent pros and cons of each of these packages.

The next level of interconnect that is slowing the silicon's performance is the interconnect substrate. The traditional and widely used substrate fabrication technology cannot accommodate fine lines and microvias needed for interconnecting high pin count and lower pitch packages (or silicon). While package technology has not made the comparable progress achieved in the silicon technology over the last decade, the substrate technology is in the horse and buggy days compared to package technology. Unless the industry makes comparable progress in substrate and package technologies, the desire to achieve that performance in picoseconds will remain only a dream.

There are a variety of packages with their advantages and disadvantages. The key distinguishing feature in them is their pitch, the way the pins are arranged, and the type of housing material used (plastic or ceramic). **SMT007**



Ray Prasad is the president of Ray Prasad Consultancy Group and author of the textbook *Surface Mount Technology: Principles and Practice*. Prasad is also an inductee to the IPC Hall of Fame—the highest honor in the

electronics industry—and has decades of experience in all areas of SMT, including his leadership roles implementing SMT at Boeing and Intel; helping OEM and EMS clients across the globe set up strong, internal, self-sustaining SMT infrastructure; and teaching on-site, in-depth SMT classes. He can be reached at smtsolver@rayprasasd.com and has an upcoming SMT class April 20-22, 2020. More details at www.rayprasasd.com. To read past columns or contact Prasad, [click here](#).

I-007e Micro Webinar: Corrosion and Tin Whisker Mitigation Understood

Have you ever wondered about the process of corrosion and the formation of tin whiskers? The third episode of the popular webinar series, *Coatings Uncoated*, is now available to view. Author of *The Printed Circuit Assembler's Guide to Conformal Coatings for Harsh Environments* and topic expert Phil Kinner from Electrolube shares highly focused educational information on conformal coating and encapsulation. If you are in the assembly business, an EMS, or responsible for specifying conformal coating and/or encapsulation, then this free series is for you.

Watch the latest segment, *Corrosion and Tin Whisker Mitigation Understood*, which covers the elements required to invoke corrosive damage and the role of cleaning. How can conformal coating and cleaning protect the board from corrosion and mitigate against the effect of tin whiskers?

In this engaging, 12-part webinar series, Kinner will delve even deeper into the subject, examining conformal coating chemistries in further detail, including their prop-

erties, applications, issues to be mindful of and the processes you should follow to achieve a successful coating outcome. The entire “Coatings Uncoated!” webinar series can be viewed in an hour and covers a comprehensive range of hot topics and application-relevant case-study overviews, as well as back-to-basic subject matter and issues, such as condensation and contamination. Each of the 12 segments can be viewed in about five minutes.

Got five minutes? Visit iconnect007.com/webinar/cu.



The graphic features a purple and blue background. On the left, it says "I-007e Micro Webinars" and "On Demand: Free 12-part* Micro Webinar Series". The main title is "COATINGS UNCOATED!" in large white letters, followed by "with Expert Phil Kinner". On the right is a portrait of Phil Kinner, a man with glasses wearing a dark suit and light shirt. At the bottom left is a QR code, and at the bottom right is the "ELECTROLUBE THE SOLUTIONS PEOPLE" logo.



Supplier Highlights



Koh Young to Showcase AI-based Inspection Solutions at IPC APEX EXPO 2020 ▶

Koh Young, an industry leader in 3D measurement and inspection solutions, will showcase advanced AI-based inspection solutions at IPC APEX EXPO during February 4–6 at the San Diego Convention Center.

Mycronic Implements New Group Structure ▶

Mycronic AB has grown substantially during the last years, both organically and through acquisitions. To prepare for continued profitable growth, a new group structure is implemented in order to achieve the strategic priorities of improving profitability in Assembly Solutions, securing and expanding the position in pattern generators, and enhancing customer-centricity.

I-007e Micro Webinars Releases Part 2 in 'Coatings Uncoated!' Series ▶

The second part of the popular webinar series, “Coatings Uncoated,” is now available to view. Author of The Printed Circuit Assembler’s Guide to Conformal Coatings for Harsh Environments and topic expert Phil Kinner from Electrolube shares highly focused educational information on conformal coating and encapsulation.

Critical Manufacturing Appoints Technica U.S.A. as Its Newest Representative ▶

Critical Manufacturing, an ASM PT company, is pleased to announce the appointment of Technica U.S.A. as its company representative in the Western United States territory of California, Nevada, Washington, Oregon, Idaho, Utah, Arizona, New Mexico, Montana, and Wyoming.

MacDermid Alpha Electronics Solutions to Highlight the Kester Integration at IPC APEX EXPO 2020 ▶

MacDermid Alpha Electronics Solutions, leaders in innovative electronic interconnect technologies, will feature Affinity 2.0—its highly stable, low-corrosion ENIG process—and the ALPHA® HiTech™ portfolio of low-temperature adhesives, encapsulants, and underfills, at the IPC APEX Conference and Expo, February 1–6, in San Diego, California.

Indium Corporation Announces Partnership With InnoJoin ▶

Indium Corporation has formed a new sales partnership with InnoJoin GmbH to better serve its NanoFoil® customers in Europe.

MIRTEC to Exhibit Technologically Advanced 3D AOI and SPI Inspection Systems at IPC APEX EXPO 2020 ▶

MIRTEC will premiere its complete line of 3D AOI and SPI systems in Booth #1900 at IPC APEX EXPO 2020.

PDR to Show Compact X-ray Systems at IPC APEX EXPO 2020 ▶

PDR—a leading manufacturer of BGA rework systems, test, and inspection equipment since 1985—is pleased to announce plans to exhibit its X-ray equipment at IPC APEX EXPO 2020, on February 4–6.

Indium Corporation President to Deliver TestConX Keynote on Materials Science Innovations ▶

Indium Corporation’s Ross Berntson, president and COO, will deliver the keynote presentation at TestConX, to be held March 1–4, 2020, in Mesa, Arizona, USA.



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Solder in PCBA: Can't Live Without It... or Can We?

Article by Joe Fjelstad
VERDANT ELECTRONICS

Solder is a marvelous material for joining metal parts together at relatively low temperatures. The first use of solder to join metals (mostly for adornments and some simple tools) came on the heels of the discovery of tin in Britain some 4,000 years ago, according to technology historians. The base metal and later simple alloy's utility found for it an ever-expanding roll in civilization and industry for items as disparate as joining water piping, sealing automotive radiators, and making stained-glass windows. However, its crowning role for most of the last century has been for joining electrical and electronic elements of electronic products, from simple spliced wires to the most advanced chips and chip packages of the present day.

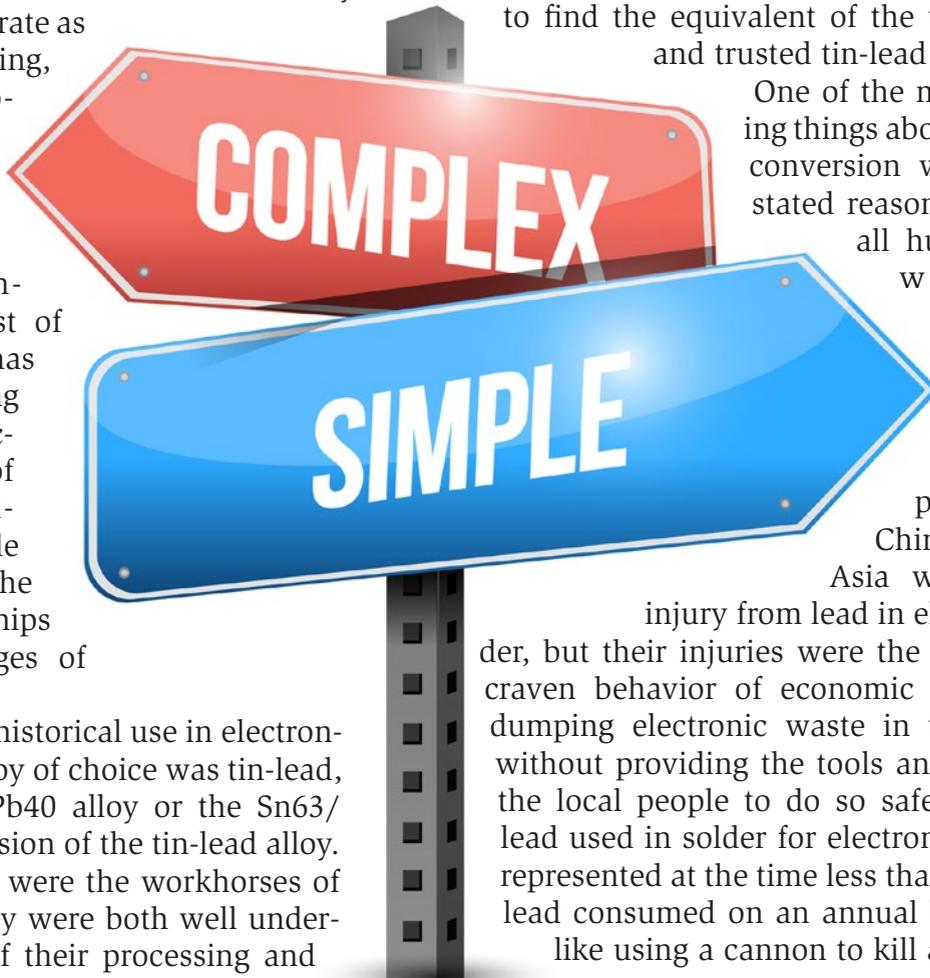
For most of its historical use in electronics, the solder alloy of choice was tin-lead, either an Sn60/Pb40 alloy or the Sn63/Pb37 eutectic version of the tin-lead alloy. These two alloys were the workhorses of the industry. They were both well understood in terms of their processing and

reliability—that is, until the advent of lead-free, a well-meaning but ill-conceived and poorly executed conversion, forced on the industry by the European Union in 2006.

While the purveyors of prospective lead-free solder solutions asserted that they had everything under control, nothing could have been further from reality. After the rollout of the first high-temperature SAC alloys, the industry quickly found out how vulnerable their production lines and products really were. More than \$100 billion has since been spent trying to find the equivalent of the tried, tested, and trusted tin-lead alloys.

One of the most frustrating things about the forced conversion was that the stated reasons for risk to all human health were massively overstated. There were admittedly people in China and South Asia who suffered

injury from lead in electronic solder, but their injuries were the result of the craven behavior of economic opportunists dumping electronic waste in those places without providing the tools and training to the local people to do so safely. In short, lead used in solder for electronics products represented at the time less than 0.5% of all lead consumed on an annual basis. It was like using a cannon to kill a fly.



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It was in this environment that the Occam Process was first conceived and proposed. Put simply, it proposed that it might be the right time to consider ways of making electronic assemblies without the use of solder. The following words of William of Occam—a 14th century monk, philosopher, and logician—were the inspiration: “It is vain to do with more what can be done with less.”

Since that time, numerous ways of making electronic assemblies without solder have been shared, but the basic idea is to assemble a component board with component terminations facing up and then build up the circuit layers (Figure 1). No solder is required. The concept was not surprisingly met with ridicule by some (but not all) folks in the solder industry, who was clearly not interested in a solution that did not require solder and reducing revenue.

A dozen years have since passed the lead-free rollout, and the perfect lead-free solder solution is no closer than it was back then. While there could not be found a current count of the number of different lead-free alloys proposed or in use, in *Database for Solder Proper-*

ties With Emphasis on New Lead-free Solders—published jointly by the National Institute of Standards and Technology (NIST) and Colorado School of Mines in 2003—approximately 50 different lead-free alloys were identified and characterized. Couple that with the myriad different fluxes, both clean and no-clean, for reflow and for pastes, and it is evident that narrowing down a single solution has been both a Herculean and a Sisyphean task for process developers with no perfect solution yet in sight. With that in mind, it is argued in the rest of this brief article that if solder can be bypassed, there are significant prospective benefits to be gained in terms of design simplification, cost, performance, and reliability. These areas are each worthy of brief individual discussion.

Design Simplification

Advanced electronic products are often designed using whatever chips are available to get the job done. Often, those chips have only one function of interest; however, everything must be connected for the chip to function, but all terminals must contact and adhere to

Basic Occam Process Steps

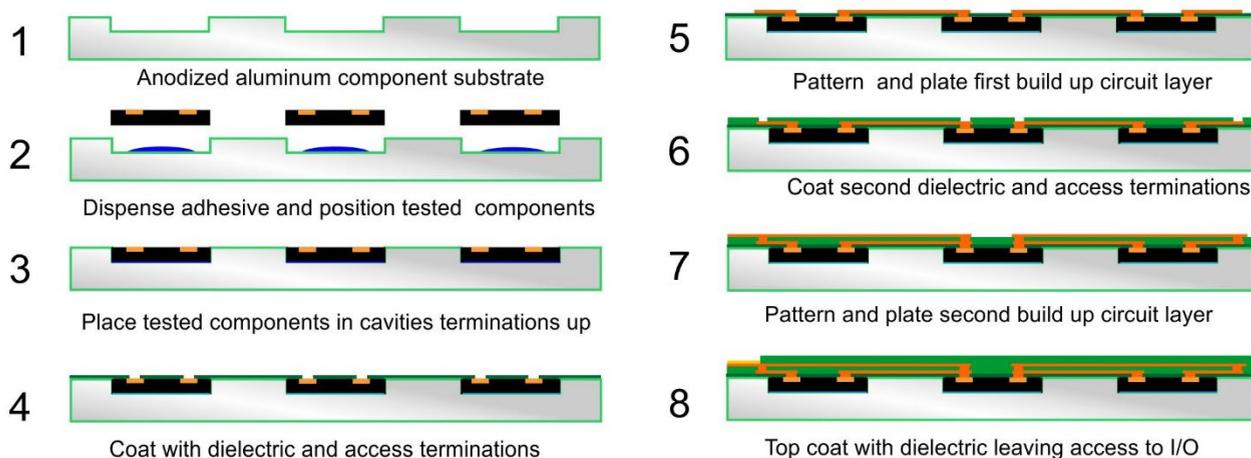


Figure 1: The basic Occam Process steps for a single-sided assembly (double-sided assembly is also possible). Because soldering is not required, the use of aluminum as a substrate is a viable option. The anodizing step for which electrophoretic coating with a polymer could be substituted and is also optional. Both provide very uniform surface coatings. Note: As a metal, aluminum is highly predictable in terms of dimensional stability, a near CTE match to copper, and an excellent thermal conductor.

the conductor metal pattern on the substrate. Moreover, undeployed terminals consume real estate and become routing obstacles. One result in the present paradigm is that the choice for the packaged function will be made by choosing from numerous different package formats, outlines, heights, lead pitches, and termination finishes. This cacophony of choice (aside from height) is often a routing nightmare as designer and design software try to find the best possible routing solution and then deal with and provide redress to the early inevitable electrical and electronic problems that can affect signal integrity.

The Occam concept proposes that all devices on the assembly have a common base lead pitch depopulated as required to hold to the objective (Figure 2). This includes everything from discrete devices to CPUs. This simple act can greatly relieve the routing challenge and result in a significant reduction in terms of design spins, the number of routing layers, and the overall size of the assembly. Figure 3 shows a comparison of results using the same number of components but with the latter design having all components of 0.5-mm pitch.

Grid-based routing was common in the early days of electronics manufacturing when nearly all components had leads provided on a 0.100" pitch. Unfortunately, surface-mount technology followed an "80% rule" for successive generations of component termi-

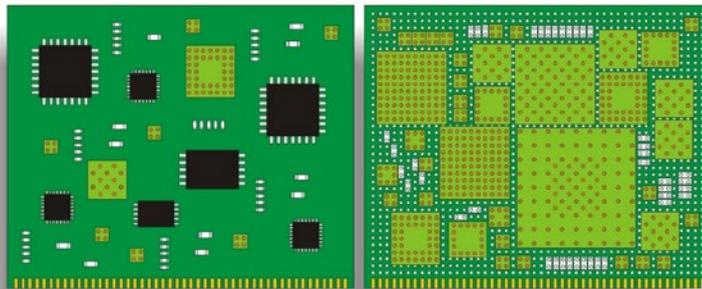
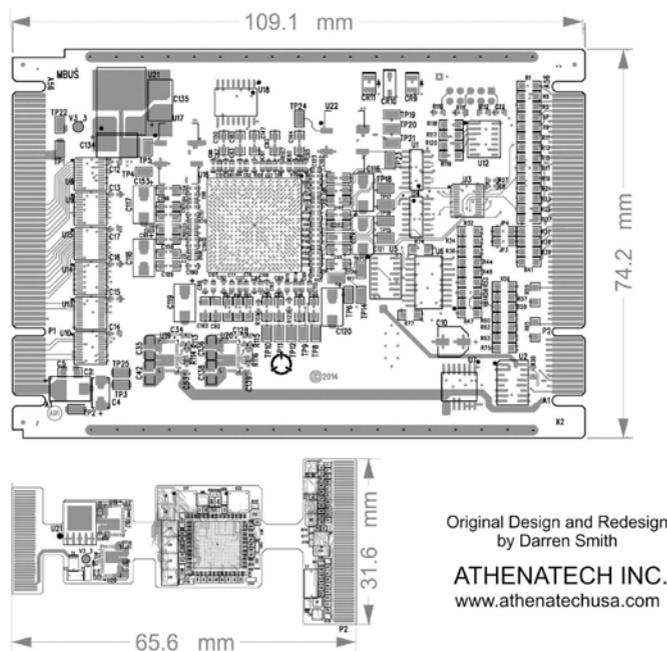


Figure 2: Multiple lead pitches and termination designs (L) make for less efficient designing and a greater waste of space and layer burn to accommodate non-uniformity. In contrast, designs where all terminations are on a pre-determined (e.g., 0.5 mm) circuit routing is immensely simplified. Note: The base grid pattern is shown for illustrative purposes only.

Occam Design Advantage Demonstration



DETAILED COMPARISON SUMMARY

Design Feature Value	Original Design	Occam Redesign	Occam Advantage
Board Area	11,900 sq. mm	3400 sq. mm	28% of original
Component lead pitches	2.54, 1.25, 1.0, 0.8, 0.65mm	0.5mm	5x less
Minimum Line/Space	100 μm / 200 μm	50 μm / 50 μm	50% of original
Land size vs termination target	Numerous	100 μm	Single value
Nominal Via Pad Size	610 μm	100 μm	16% of original
Nominal Via Hole/Via Size	305 μm	50 μm	16% of original
Layer Count*	12	6	50% of original
Circuit construction	Rigid FR4 PCB	Rigid Flex Circuit	Foldable circuit

Figure 3: The Occam concept offers significant advantages in design execution and increased simplicity. The design comparison above was performed by Darren Smith of Athena Tech, who designed both assemblies.

The component count and type are the same for both designs, but for this "thought experiment" demonstration, the Occam design used only fully tested components envisioned to have all their terminations located on a 0.5-mm grid pitch. The data in the table speaks for itself.

nations, which erased the advantage enjoyed by previous generation designers. If they had instead chosen a base grid pitch and depopulated the grid to get to their objective, all design would have been much simpler today.

There is much more that can be said about this topic, including a discussion of grid-based versus shape-based routing, and that is a topic for a future article. However, what has been provided should provide a basic appreciation and understanding of the benefits.

Cost

There are numerous factors that need to be accounted for in a cost analysis. The major ones are materials and labor, but there are many less obvious factors that contribute to cost (inspection, test, rework and repair, machine maintenance, etc.). When solder is eliminated from the manufacturing process, numerous process steps are also eliminated as are the various process consumables, tools, and fixturing associated with them. The impact is significant. Depending on the BOM, the savings could range from perhaps as low as 5% to perhaps 35%, maybe more.

When you eliminate solder, you also eliminate the need for a PCB. The materials required are likely less expensive and potentially higher performing as the list of options is greatly expanded. Assemblies can be made smaller, and fewer layers are required (Figure 2). There are also appreciable energy and labor savings and other areas of savings if one applies objective thinking to the subject, but this list should convey the potential.

Performance

Performance is a bit of a loaded word because it can be measured in many ways. The prospective performance boosts stem from some of the same things that help to reduce the cost. Countless millions of dollars were invested in creating materials that would withstand the high temperatures associated with lead-free soldering. When high temperatures are not required, the list of prospectively useful materials expands significantly.

One of the ways to boost performance in electronics is to place components in closer proximity to one another or eliminate solder. Most electronic assembly guidelines have strict rules about component placement to ensure that the assemblies can be cleaned more efficiently following assembly and allow space for component removal and replacement if they do not survive the high temperatures of the assembly process. When solder is not used, components can be placed closer together. The time of flight for signals can thus be reduced considerably. This also can reduce the energy required to transmit the signal across the assembly.

As a side note, when you see the hundreds of I/O on a high pin count BGA, up to 80% are dedicated to power and ground and serve to help get the on-chip signals from one side to the other. Again, there are prospective benefits related to design efficiency and operation. When you fully familiarize yourself with the concept, you will come up with other benefits.

Reliability

Reliability is defined differently in different dictionaries, but the following one seems particularly well suited to the current discussion: The ability of an apparatus, machine, or system to consistently perform its intended or required function or mission, on demand, and without degradation or failure. Like quality, it is somewhat fungible in that the specific demands can vary from product to product. The reliability implications for a child's toy are understandably different from those for an implanted heart pacemaker.

In electronic products, there are many things that can go wrong, but when failures occur, either in assembly or in the field, the failure can be traced with high regularity to the solder or high-temperature soldering process. As mentioned earlier, the electronics industry has been in pursuit of the perfect set of materials and processes that assure first pass 100% yield of electronic products over its entire history without success.

Materials and processes have unquestionably gotten better, but problems remain. Look at the table of contents and advertising of virtu-

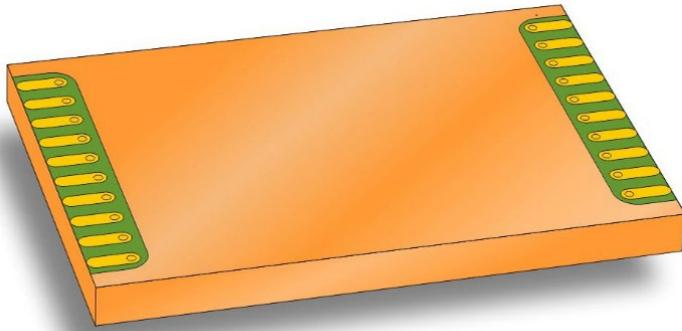


Figure 4: Occam assembly offers the potential provision of an integral full metal jacket (exclusive of I/O access features) of the completed assembly to provide near full hermetic protection along with EMI and ESD immunity.

ally any electronics industry journal or magazine, and you will find a substantial percentage of them devoted to solders; fluxes; soldering equipment; solder process improvement; fault identification, detection, and avoidance; and rework and repair. How can such a complex process with so many steps and pitfalls ever be considered truly reliable? In contrast, when solder is eliminated from the process, things arguably get much simpler. Moreover, a leading cause of electronics failure is bypassed.

Now consider the following: An electronic assembly where the fully tested and burned components with their terminations all on a common lead pitch are bonded to an aluminum substrate (a close CTE match to copper and the CTE of engineered components) and encapsulated in the structure with the circuits and copper via interconnection all on the upper surfaces (Figure 1). Shock, vibration, and drop test reliability concerns largely evaporate. Who has ever seen circuits shaken off of the surface a circuit board?)

When completed, the assembly can be plated with metal (excluding I/O required for connection to the outside world), making the assembly virtually hermetic and ESD and EMI immune (Figure 4). It also provides additional thermal spreading capability.

Summary

What has been described is different than what is currently being done but not impos-

sible. The infrastructure, materials, and processes exist. What is missing is a willingness to try a new approach. Two questions that are invariably asked are, “What about test?” and “How do you rework and repair?” The answer to both questions is basically the same and perhaps best answered in the Socratic method by asking those two questions in reverse. That is “Why do you need to test?” and “Why do you need to rework and repair?”

Testing is important in process development but ideally should not be needed in production where it provides no value. The same also for rework and repair.

These steps should not be required if the right approaches to manufacturing are used, and the processes are done right. In other words, first do the right things, and then do those things right. Think about it.

In conclusion, here is offered some solace for those whose livelihoods are tied to solder and soldering. Solder will be in use long into the foreseeable future in the same way that legacy packages, such as the venerable dual-in-line package (DIP), are still used today. There is a flywheel effect to every established technology. Certain people around the globe still make buggy whips to this day. There are also ways for solder to continue to play a role in the manufacturing of advanced electronics and construction of packages much as it is presently being used in the creation of 2D and 3D modules, which could well be adapted to solderless assembly in the future. It is simply a matter of choice and will.

“Only those who will risk going too far can possibly find out how far one can go.” – T. S. Eliot SMT007



Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending.



MilAero007 Highlights



NASA's Newest Astronauts Ready for Space Station, Moon, and Mars Missions ▶

NASA welcomed 11 new astronauts to its ranks, increasing the number of those eligible for spaceflight assignments that will expand humanity's horizons in space for generations to come. The new astronauts successfully completed more than two years of required basic training and are the first to graduate since the agency announced its Artemis program.

Zentech Manufacturing Acquires Trilogy Circuits ▶

Zentech Manufacturing Inc. is pleased to announce the acquisition of Trilogy Circuits LLC. Following the transaction, Trilogy Circuits LLC will become Zentech Dallas (Texas) and joins the Zentech family of companies that also includes Zentech Baltimore (Maryland) and Zentech Fredericksburg (Virginia).

Defense Speak Interpreted: What in the World Is MINSEC? ▶

The Defense program designated MINSEC (Microelectronics Innovation for National Security and Economic Competitiveness) is probably one that you have never heard of but will likely gather more headlines in the future. Dennis Fritz explains.

Boeing to Deliver AH-64E Apache Helicopters to Three Allied Countries ▶

Boeing and the U.S. Army have finalized orders from three nations to provide their armed forces with the new, more capable AH-64E Apache model. The contracts are for the remanufacture of 47 existing AH-64D Apaches. The total combined value of the orders is more than \$560 million.

U.S. Navy Awards BAE Systems \$175 Million for Guided-missile Cruiser Modernization ▶

BAE Systems has received a \$175 million contract from the U.S. Navy to modernize the guided-missile cruiser USS Vicksburg (CG 69).

AT&S Now in the Top League of Aircraft Suppliers ▶

With the NADCAP accreditation, the Austrian high-tech company has been recognized as a supplier of the highest quality standards in aircraft construction. The accreditation is now opening new doors in the aerospace sector.

Pendleton Marines Put Amphibious Combat Vehicle to the Test ▶

Marines with the Amphibious Vehicle Test Branch, Marine Corps Tactical Systems Support Activity, tested the ACV's maneuverability and performance during low-light and night operations on Marine Corps Base Camp Pendleton's beaches.

A New Tool for 'Weighing' Unseen Planets ▶

A new instrument funded by NASA and the National Science Foundation called NEID will help scientists measure the masses of planets outside our solar system—exoplanets—by observing the gravitational pull they exert on their parent stars. That information can help reveal a planet's composition, one critical aspect in determining its potential habitability.

U.S. Navy Awards Lockheed Martin \$43M Hawkeye Contract Modification ▶

Lockheed Martin received a \$43 million contract modification from the U.S. Navy to upgrade to the AN/ALQ-217 Electronic Support Measures (ESM) system for the E-2D Advanced Hawkeye.

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Increased Miniaturization Poses Soldering Challenges

Feature Interview by the I-Connect007 Editorial Team

The I-Connect007 editorial team speaks with Indium Corporation's Chris Nash, product manager of PCB assembly materials, about how solder and solder paste application technologies seem to be the center of the challenge for moving to smaller components. Chris also addresses the challenges surrounding, solders, fluxes, and materials due to increased miniaturization.

Nolan Johnson: With the dynamic of shrinking feature sizes, packaging, features, and landing pads, and all of the smaller sizes going on in the industry, it seems like solder, solder paste, and solder joints are at the center of it all. You must see some challenges delivering good performance in those products.

Chris Nash: It has been a challenge since the introduction of SMT. Everything has been shrinking for the last 20+ years. The mobile market is driving miniaturization, and they're venturing into the 0201 metric or 008004 component sizes for capacitors or passives. Passives usually get miniaturized first because there are so many on boards, so they need to try to save as much real estate as possible.

After that, then you start talking about some of the components with different pitches, whether it's QFNs with smaller pitches or dual-row QFNs or BGA-type packages with finer pitches down to the 0.25 or 0.3 millimeters.

Barry Matties: What we see is that the focus is on finer pitch, and we have heard that the greatest challenge is getting the solder paste in the right quantity through the stencil onto the board to get high yields.

Nash: You can look at finer pitch, but you could also say that the components are being placed in tighter spacings. If you look at a cell-phone board, for instance, you're not going to see much space between each of the components. They're trying to use every square millimeter of space on those boards.

That can cause challenges with signal integrity and dendritic growth if you don't have solder paste that is developed specifically for tight spacing or clearance.

It can also become difficult for the printing process, as well. When you get into those small apertures for smaller deposits, you have to talk about thinner stencils and smaller area ratios, and it's going to make it extremely challenging

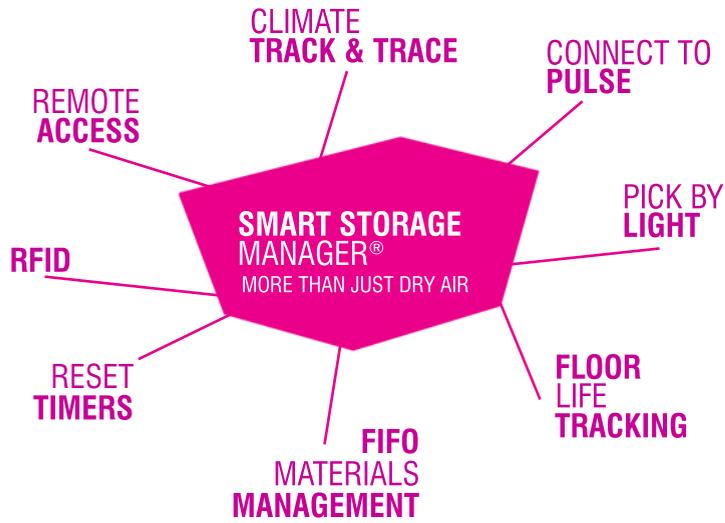




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to get the solder volume that you want, as well as the consistency in solder deposits.

Matties: Do they rely on their suppliers like Indium Corporation to develop products that will suit this application?

Nash: Yes. From a solder paste or a material standpoint, we're challenged with these miniaturization topics, including finer pitch, tighter spacing, etc. Some of the stuff that we work on is finer powders. The industry, especially the mobile industry, is looking at Type 5 powder and Type 6 powder. I haven't seen any mainstream mainboard technology going into Type 7 at this point, but we do see system-in-package (SiP) applications where Type 6 and Type 7 are mainstream solder paste technologies. However, the flux vehicle for the solder paste has to keep up with the finer powders, too.

From a solder paste or a material standpoint, we're challenged with these miniaturization topics, including finer pitch, tighter spacing, etc.

You have a number of things that come into play there, including that higher surface area of the powder creates more oxide/oxygen content, so the flux has a tougher job cleaning the oxides. Essentially, there's more oxide, so it's going to stress the flux a little bit more than normal. But you have less flux present because you have less solder paste volume present with smaller apertures.

From the powder-size standpoint, we don't have an issue. It's well-known that we can go finer in powder size and powder distribution to Type 6, Type 7, and we've done Type 8 before, but when you get to the Types 7 and 8, you're talking more about SiP applications rather than a mainstream circuit board

assembly. Some of the other challenges that you might face with solder paste and the finer powders might be graping where the solder deposit doesn't coalesce completely. You might have greater head-in-pillow challenges because there's not as much solder paste present. A lot of the other challenges would be more focused on the reflow process rather than printing process.

Matties: When a customer comes to you, are they looking at this as a total process? Are they getting recommendations for stencil material, jet, or paste?

Nash: They are. A lot of people are looking at this as cutting-edge technology. Most of the people that are coming to us have never dabbled in it or have dabbled in it a little bit, and they're asking for our recommendations on processes and materials. The two go hand in hand with each other because even if you have the greatest solder paste in the world, you aren't going to be able to fully utilize the material unless your process is also optimized. Thus, it's extremely important to look at the process, and Indium Corporation has done that for quite some time now. We feel that to be successful, you have to focus on both the material and process and optimize both for the assemblies that are being built.

Matties: When you say processes, how do you define those? Where do you set the boundaries—as soon as the data comes in from the factory, or in the imaging area?

Nash: We look at the entire process, which starts at the material supply, ensuring that the customer is getting the material in the best condition as possible. There are a number of processes within manufacturing as well, such as the printing process, which will determine the volumetric transfer efficiency of the solder paste. The SPI equipment will help to determine the consistency of the transfer efficiency and make sure that you don't have any defects with regard to bridging, insufficients, or excessive solder deposits.

After that, you have to consider the pick-and-place process and how the components would be placed, including if there's skewing of the components or if the placement pressure is too great or not enough; all of that can affect how the material is going to reflow. Then, you would focus on the reflow process. You have to optimize each process separately. You can't look at just one process and say, "Printing is great, so we're good to go." It's not going to work well for you if you ignore one or more parts of the manufacturing process. The placement has the least number of eyes on it from a solder paste standpoint, but it comes into play when you're talking about miniaturization and small components.

Matties: We have heard that there are now more opens than bridges because people aren't putting enough paste down. When your customers are working in fine pitch and high density, are they doing an inspection process beforehand?

Nash: With mobile and automotive manufacturing—or any type of circuit board manufacturing, for that matter—most people implement SPI into their process. It's a piece of equipment that could save you costly rework and ensure that you have process optimization on the printing side of things. In my career at Indium Corporation, I've heard a couple of different percentages—anywhere from 60% to 98%. I don't know what the true number is, and I don't know of a study that's been done on this, but the majority of defects at the end of the line can be the result of printing process errors.

Matties: Rectify it before it becomes waste.

Nash: That's exactly why a lot of people are putting SPI equipment into their lines to try to optimize the printing process to avoid defects



Chris Nash

at the end of the line and costly repairs. It is an important step toward cost reduction. In many cases, people look solely at the cost of the solder paste, but they forget that total cost includes the cost of materials, manufacturing, and rework.

Matties: The cost of a recall is extraordinarily high. An open may not be something that affects the whole line, but it can be catastrophic; in some cases, human life is at risk.

Nash: That's an important note to make. What's the cost of a failure in the field? You don't want something like that to happen because that's usually in the millions of dollars when it could have been corrected by optimizing your process and choosing a material that is optimal for your assembly rather than basing the material decision solely on cost.

Matties: And traceability is getting easier and easier as time goes by as well, so liability trickles down the supply chain.

Nash: The other important thing to mention regarding miniaturization is Z miniaturization as well. Many people are trying to pack circuit board designs into a thinner package. If you look at cellphones from 2000 to 2020, they have gotten thinner. Cavity printing was a topic a few years ago. People are doing that, but many are doing stuff in cavities with jetting materials or dispensing materials rather than printing processes. Z-axis is also going to be more challenging because you have to heat the flux properly. You don't want an unactivated flux underneath the component, which could cause a catalyst for dendritic growth formation. Designing materials that have electrical, thermal, and mechanical reliability is important.

Matties: What advice do you give companies from the outset before they move into this type of technology?

Nash: It depends on the technology at hand and what's being addressed. If you were to think about the mobile world and 0201 metric components, printing process challenges are going to one main concern. We have a good take on the material side of things and being able to print materials for 0201 metrics and reflow 0201 metric size deposits; however, the process is going to need to be optimized, and that the main stress point should be process optimization. You're not going to be able to put the assembly and the solder paste on a line and run it without doing process optimization.

Further, process optimization could be a number of things. It could be machine settings or fixtures like tooling fixtures specific to the board that you're using. It could be the stencil technology or the stencil thickness and aperture size. There are a lot of factors that go into optimizing a printing process to be able to manufacture circuit boards with 0201 metric components repeatedly and reliably.

The automotive market is another area where we see a miniaturization trend, but it's not to the levels of the mobile market at this point. When you talk about solder paste materials in the automotive realm, they're transitioning from the typical Type 3 solder paste to a Type 4 solder paste, and, in some cases, there might be applications for Type 5 materials. Again, it's not to the extent of mobile technology.

Matties: Is the medical market moving into this space as well?

Nash: The medical market is a broad market from an electronics standpoint. You might have medical equipment that doesn't need fine pitch-type components, and you might have wearables that need fine pitch or tight spacing on the board. It's a broad range within the medical market. Some of the medical products resemble consumer products more than typical medical products, such as a watch that monitors

heart rate or blood pressure. You can say the same for military and aerospace as well, where some of these applications require small circuit boards, especially if they're wearable devices, because you don't want to wear a bulky electronic device around on the battlefield.

Matties: That will grow at an accelerated pace.

Nash: It will. You will see a lot of wearables in hospitals and medical settings, but they may be throwaway or recyclable items. They might be one-time use products. I know a lot of companies, including Indium Corporation, are looking at recycling within the industry, whether it's on the packaging or materials side. Recycled tin, for instance, is a topic at a number of different multinational companies nowadays.

Matties: Do you see a trend toward low-temperature solders as well? Does that play into this?

Nash: Yes. It has been a topic within the industry for a few years, and a lot of people have exciting thoughts about low-temperature solders. There is a pretty wide array of low-temperature alloys available on the market. Low-temperature soldering is something that Indium Corporation has been involved in from our founding in 1934. At Indium Corporation, we also strive to improve our solder paste flux vehicle technology along with developing new alloys. It is important to ensure the flux technology is current and will handle any of the challenges that manufacturing sees.

Many of the alloy offerings in this realm have been around for quite a while, such as the common indium-based or bismuth-based alloys. Indium-based solders tend to be a little more costly than SAC solders, and many people don't take the time to break down the per board cost to see the marginal difference. Bismuth-based solders tend to be brittle by nature, so drop-shock performance or mechan-



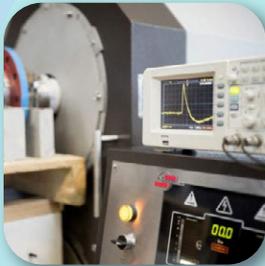


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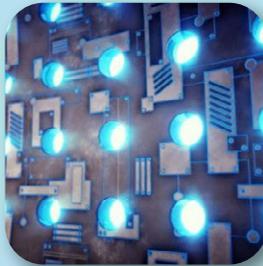
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ical stresses are not going to be good for those particular alloys.

Indium Corporation has developed a unique low-temperature alloy technology that provides high drop-shock performance. Durafuse™ LT surpasses the drop-shock performance of bismuth alloys by two orders of magnitude and is comparable to SAC alloys when an optimal reflow process is employed. We'll be talking about this technology a lot in the coming years as it gains traction in low-temperature applications.

Matties: Do you see more jet technology for solder paste, probably more in North America than Europe and Asia?

It is important to ensure the flux technology is current and will handle any of the challenges that manufacturing sees.

Nash: We see a trend with jetting all over the world, but a lot of times, it's going to be for niche applications, or it's going to be for low-volume, high-mix applications. These low-volume, high-mix applications have a lot of changeover, and the engineers don't want to buy hundreds of stencils for the vast amounts of products that they are building.

Placing components in cavities is another application where we see jetting and/or dispensing technology becoming more popular. Indium Corporation has done a remarkable job with our materials, but we couldn't have done it alone. We've partnered with many of the jetting and dispensing equipment suppliers to ensure that we have materials that will work in their equipment sets and meet the end user's soldering requirements. I believe this technology is trending upward, but I also don't feel that jetting equipment will be taking over for stencil printing any time soon.

Johnson: We started this conversation with the statement that solder, solder paste, and application technologies are the center of the challenge in moving to smaller components. It seems to me like you're suggesting that a key part within that is flux.

Nash: You're correct in saying materials are one piece of the puzzle; however, processes might be a bigger piece of the puzzle than materials. Going one step further within the material scope, flux and powder are your two big areas of concentration on miniaturization. Smaller deposits are going to need a finer powder solder paste. Manufacturing the finer powder is challenging, but we have the capabilities to do it. Standard mainstream applications are going to be using Type 3, 4, 5, and 6 powders at this point in time.

Johnson: What I heard you say was that as boards get smaller, there's less flux overall, but the flux needs to do even more work at the same time.

Nash: Yes, it's less flux, but because you have finer powder, you have more surface area, which means more oxygen content so that the flux has to work that much harder to clean the oxide off of the powder and the substrate metallizations that you're soldering to. Then, it has to perform through a reflow process as well and not burn off to create any hidden pillow defects or coalescence issues. You still want to end up with a smooth solder joint that wets well at the end of the reflow process. The flux has to work that much harder, and there's less of it, so that's a challenge.

Johnson: It doesn't sound like the challenge is in the powder.

Nash: For many of the defects seen within the industry, the challenge is with the flux technology. The flux is the most important technology within the solder paste and soldering process to eliminate any end-of-line defects because it plays a significant role in printing and reflow. However, the process plays a significant role;

making sure that it's optimized is extremely important as well.

Johnson: They run hand in glove. You need the process to make sure that you're properly managing the flux to its greatest capability.

Nash: With the current space within manufacturing, a lot of times, the engineers are taxed and have a lot of jobs to do; they're wearing a lot of hats and relying heavily on the material suppliers to help them with their process to provide the knowledge needed to manufacture their assemblies properly and with as few defects as possible. That's where Indium Corporation does a fantastic job of providing the technical knowhow to support our customers.

Johnson: Earlier, you mentioned partnering with equipment manufacturers. As you work with a customer to optimize their processes, is this a scenario where the customer's equipment engineers and your engineers work together?

Nash: In many cases, we may have the process knowledge to fix issues without requesting help from the equipment suppliers. Other times, it's a more challenging and/or cutting-edge technology and challenge, and we will work with equipment suppliers and other industry partners to fix the customer's challenges.

Matties: Do you ever have contact with the PCB designer? Do they ever have inquiries regarding their design and your process?

Nash: It is one area that I wish manufacturing engineers would have more dialogue with design engineers. A lot of the problems and challenges and defects that the manufacturing engineers deal with daily could be eliminated if the DFM engineers and design engineers would talk more openly. That's a common thread that I've seen throughout the industry since I started in 2005. Although we are getting



better at this over time, there is always room for improvement.

Andy Shaughnessy: It's funny because designers often say they talk to you, but in reality, they don't often communicate.

Nash: They communicate to some extent, but there's room for improvement. Some companies will do it better than others. Some companies have design rules that the manufacturing engineers develop and share with the design group. I've also seen where manufacturing engineers will provide feedback on challenges that they are facing, and they are able to get the recommended changes in the next revision. However, it's not always an easy task for every company or contract manufacturers.

Johnson: There are times when you're having a conversation, and what it comes down to is, "We'd be able to do better with this particular product if we had better landing pads. Everything else is doing its job as best as it can."

Nash: Definitely. One example might be solder beading, for instance. Often, what's happening is people miniaturize their boards and leave the designs the same. They're saying, "We can get 0201s a lot cheaper than we can 0402s because the mobile industry has driven the component suppliers to smaller passive components." I've seen companies place 0201 components on an 0402 pad instead of redesigning the board for that particular compo-

ment. It causes challenges with the solder beading performance, or tombstoning occurrences might increase. There are still some corners that people try to cut to save a little bit of cost, which could open up major cost implications on the back end with rework.

Shaughnessy: What advice would you give to designers and the EEs upfront other than communicating with you earlier?

Nash: It's not just communicating early; it's also about communication throughout because the manufacturing engineers are the ones dealing with the problems in real-time. They come back to the suppliers and say, "We have challenges with this. We can't fix it with the current material. What else do you have?" Then, we try to work with them on both the material and process improvements to eliminate the issue. But if you redesigned your pads for these components, you wouldn't have the problems with this current solder paste that you're using. The ideal scenario would be a continuous conversation, or regular meetings, between the manufacturing engineers, design for manufacturing engineers, and design engineers.

Happy Holden: I noticed in our reporting of the CES Show that more and more consumer products are wearables, which requires high-density circuit boards. Is assembling products like that the same type of challenge as packaging or SiP assembly?

Nash: The technology around SiP assembly and heterogeneous integration is what people are calling higher-density circuit board manufacturing. For example, they might be trying to put a Wi-Fi and Bluetooth module into one package, and that will help with the circuit board density. Before, you might have had two separate packages doing the same thing as the SiP would do. However, they're also trying to generalize these technologies and make them more cookie-cutter, as well as customizable, so that you can take three or four different things and plug it into one, but those three or four different things are standardized. One customer

might put two in one, and another customer might put five in one package, but the ability to do that is there. That way, you can put a lot more stuff on, including four or five different SiP packages on the same circuit board in half the footprint.

Holden: Does it take specialized solder paste if you're going to embed the component inside the circuit board where it's going to go through lamination and even later surface assembly?

Nash: If you think about it from a packaging standpoint or SiP, for instance, you use the solder paste to build a mini circuit board, and then you use some sort of molding compound to mold over the package to protect it for a number of different reasons, whether it's proprietary or environmental.

Some flux technology has to be compatible with the over-mold, or people clean off the flux residue to eliminate the compatibility uncertainty altogether. The majority of people building SiP over-mold the package, but most of them use either a water-soluble flux vehicle in a solder paste where they can clean it with DI water or a no-clean material and a solvent-based cleaner.

The same holds true for any coating materials or encapsulation materials, whether it's a potting compound, conformal coating compound, or molding compound. You need to do your due diligence up front and make sure if you are going to leave the solder paste flux residue behind, that you have some knowledge that the materials are going to be compatible. In other words, the conformal coating or molding compounds are going to be compatible, electrically and/or mechanically (adhesion) with the no-clean flux residue that's already present. Again, the same holds true for the circuit board. Is the solder mask compatible with the molding, compound, conformal coating compound, etc.?

Matties: This has been very helpful, Chris. We appreciate your time.

Nash: Thank you. SMT007



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Market Insights From Epoch International's President



Interview by Barry Matties I-CONNECT007

Epoch International is an EMS company specializing in front-end engineering. Barry Matties speaks with Epoch President Foad Ghalili at productronica 2019 about the company's ability to maintain low employee turnover, challenges they're facing, and expected growth in the U.S. market.

Barry Matties: Foad, we're in Munich right now, but where is your headquarters located?

Foad Ghalili: Our headquarters is in Fremont, California, and we have other facilities around the world, including Dalian, China.

Matties: Talk a little bit about what you do.

Ghalili: Epoch is an engineering services manufacturing company. We put a lot of emphasis on front-end engineering. Most of the customers that we work with are looking for IP protection, and that also gives us leverage to bring about socially responsible companies because I think they are interlinked. You cannot segre-

gate IP from socially responsible companies, so that is one of the areas where we're strong. We've been at the forefront of that industry. We are working with large corporations where IP becomes a key element for them. At our company, we have had zero turnover on our manufacturing floor. In the entire company, we have about 4% turnover, which dictates how we run the operation. That gives you an idea of our company culture and environment.

Matties: For reference, how many people are in your organization?

Ghalili: We have 150 people in China and about 10–15 running the Fremont operations. We bring value to the employees because the company shares its profit. About 25% of the profits are distributed with the employees. They have free education. For example, our production manager started as a technical high school employee on a production floor. She now has her MBA degree through the company, and she's running our production department. We have a lot of those stories where employees have grown with the company and have been able to bring a lot of value to the organization.



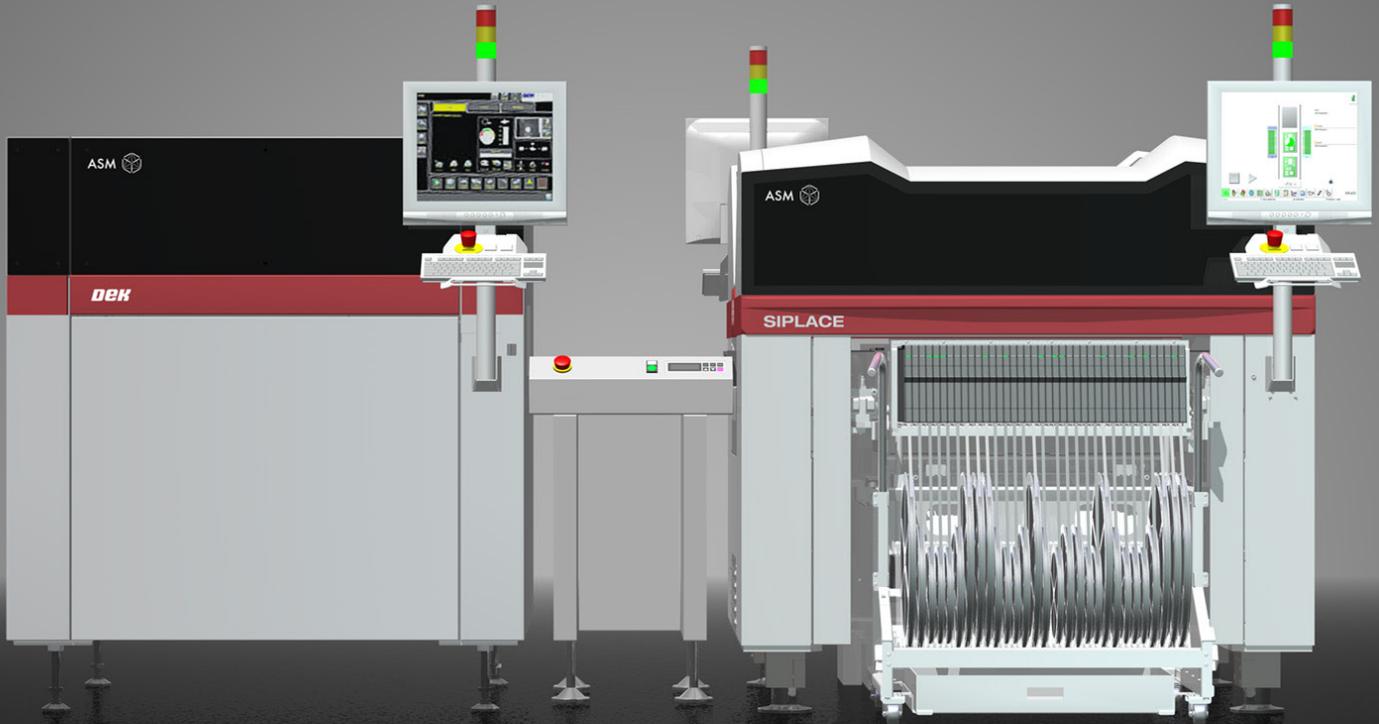
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Matties: Are you the founder of the company?

Ghalili: I am one of the founders. The company celebrated its 25th year anniversary last year.

Matties: Congratulations. So, the culture is based on your values.

Ghalili: That's right.

Matties: In China, there's a culture that may not be congruent with what you're discussing.

Ghalili: Exactly. Again, when I first went to China, I was a general manager of a joint venture company in China running a ceramic chip capacitor, and I've always thought that we need to bring in different companies that bring value to society; I felt that would be an area to begin with. In those days, many of the foreign companies thought, "How can we bring products so that we feel confident that our IPs are protected?" Then, we asked, "How can we bring a foreign company that does not abuse the labor force and use them only for their labor to produce a product?" We were able to marry these two concepts together and bring that force into Dalian.

Matties: That's good for the region as a model for others as well. We know during Chinese New Year, most companies lose a large or a percentage of employees, and that's a big problem. As you know, it creates an interruption in fabrication services.

Ghalili: Exactly. In a discussion with one of our customers, they mentioned that every time after the New Year, they go through completely retraining their employees at their other contract manufacturing site. However, with us, they have worked with the same employees for the past 10 years, so they can continue building on the past experience.

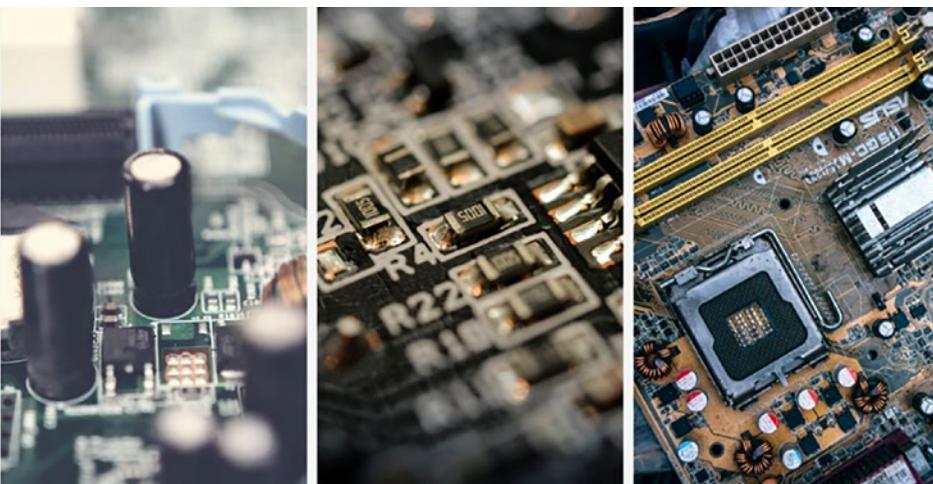
Matties: You described it as an EMS company with a front-end engineering strength.

Ghalili: Exactly. We have 40% of our employees on the manufacturing floor, and 60% are on the front-end. We have 30–35 R&D engineers involved in the design development phase. Then, you have our quality, supply chain, and other staff, many of them with engineering degrees. We are heavy in the front-end, going into manufacturing.

Matties: In manufacturing, one of the highest costs has been around labor, and we've seen labor prices increase in China, so we see a lot more of the digital factory. How are you responding to the digital factory?

Ghalili: Our engineering R&D people are starting to implement some of these digital concepts. Our hope is to grow but not necessarily add labor to the operation. In the past 25 years, we've never had a layoff because of lack of work. We want to continue on the same path and not reduce our labor force as we are growing into the digital environment; instead, we want to use the same labor force and move them up the value chain. They're going to perform these higher-end value production through the constant training we provide to them.

Matties: Your values toward education easily fit with that philosophy. Because you're exactly right that you can grow and retain the people that you have, which is great. What's the greatest challenge in your business?



Ghalili: Our greatest challenge is bringing these concepts to the customers and other people. Many people look at the hard, mechanical, tangible, or build value.

Matties: You're talking about the intellectual or social value.

Ghalili: Yes. Those things are hard to quantify or put finances to. Again, one of our challenges has been, "How do we educate our customers, suppliers, and the whole chain that there is a value to what we are bringing into the work environment?"

Matties: For many, it's about the bottom-line dollar, though.

Ghalili: Exactly. People don't see that in reality, it also brings financial value when you don't have that turnover, when you're not going through constant reeducation, and when you don't have the quality problems because of these turnovers. Somehow, people cannot look at these values from a financial perspective.

Matties: But what you're selling is stability, and when you have stability in your supply chain, you have a better supply chain. What type of customers do you primarily deal with?

Ghalili: We deal heavily with customers looking for IP and front-end engineering needs.

Matties: Are there any market segments that you're specializing in, or is it across the spectrum?

Ghalili: We are not involved in the low-end market. We mostly do products that bring high-end value to the customers. We do a lot of test boxes on the systems that are business-to-business products.

Matties: There's a regional trend going on in manufacturing: build it where you need it. As we see labor costs being eliminated in



operation, we're realizing that factories can be built anywhere, especially on the assembly box build side. With the amount of work that you're producing in China, how much of it is being exported, and how much is being retained domestically?

Ghalili: Right now, 85–90% is shipped in China, and 10–15% is exported.

Matties: Are you happy with that mix?

Ghalili: We're fine with that. Our long-term objective, again, is to build it in the region for the region. I do not understand why we are wasting resources shipping goods from one part of the world to the other part. For me, energy efficiency and environmental impact are bigger issues than anything else.

Matties: Fuel, energy, and time are all major factors. When you look at the U.S., how do you see the market? With the shift in politics and tariffs, is there more opportunity for you now?

Ghalili: Definitely. The U.S. market is strong because of various cultural integration. The strength of the U.S. is its diversity, and that's what brings its R&D expertise. I think manufacturing will grow in the U.S. and the type of manufacturing will not be what we are

thinking of today; the mode of manufacturing is changing, irrespective of what the political situation is.

Matties: If we can drive cost out, that's where opportunity exists. What about supply chain management? We know that we've had some supply shortages in the recent past, but it sounds like those have been smoothed out.

Ghalili: Again, I think the U.S. is also going through its learning curve from infrastructure to manufacturing, especially in electronics. That manufacturing infrastructure is much stronger in China. No matter what you say, they have been doing this for the past 15–20 years. The infrastructure is starting to build again in the U.S. Again, my personal feeling is it has nothing to do with politics, and it's going to take some time for it to build U.S. manufacturing infrastructure, especially in the supply chain. Today, we build parts in the U.S., but we bring the fab from China. This has to shift at one point, so these are the areas that still need to go through the process of change.

Matties: You mentioned the politics of it, but in business, what we have to do is react to the situation; it doesn't matter what it is, but we have to be smart in that circumstance.

Ghalili: Correct.

Matties: Where is your business headed?

Ghalili: We see growth in the United States, and long term, we see our growth in India. Once the fundamentals are built in the U.S., the next market for us is to set up manufacturing facilities in India. Again, this is a reality. When you look at the population of the world, it's China, India, and of course, the United States with all of North America, so those would be our next areas of growth.

Matties: Foad, it has been great meeting you, and I appreciate your time and insights. Thank you very much.

Ghalili: Thank you. SMT007

Hitachi High-Tech Group to Lead Japanese Distribution of Kurt J. Lesker Company's Thin-film Deposition Systems

Hitachi High Technologies America Inc., a subsidiary of Hitachi High-Technologies Corporation, announced that HTA has made an agreement with Kurt J. Lesker Company® for HTA and affiliated companies in the Hitachi High-Tech Group to serve as the exclusive distributor in Japan for Kurt J. Lesker's PRO Line™ PVD 75™ Thin-film Deposition System and PRO Line™ PVD 200™ Thin-film Deposition System. Information regarding the systems is currently available to Hitachi High-Tech Group's customers in Japan.

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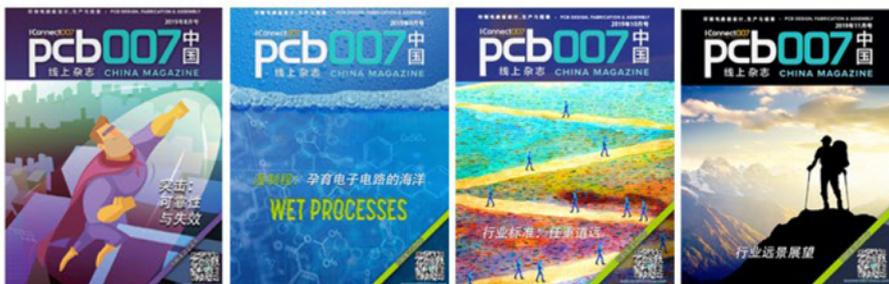
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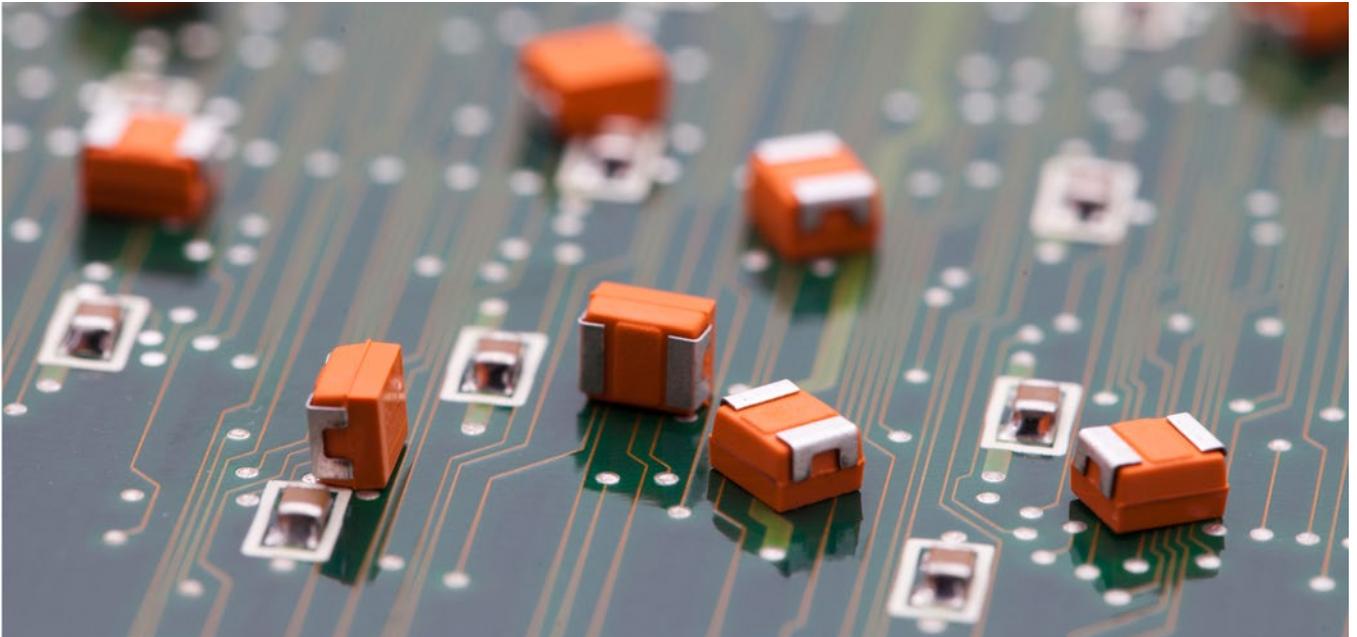
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Embedding Semiconductors

Article by Vern Solberg
CONSULTANT

Embedding components within the circuit board structure has evolved from the more basic and mature passive component integration to more complex process methodologies developed for embedding new generations of very sophisticated semiconductors. While techniques developed for embedding and terminating the semiconductor within the circuit structure have not reached universal acceptance, progress in developing high-volume manufacturing capability for performance-critical applications has accelerated throughout the high-end technical community.

The decision to embed components within the multilayer printed circuit board or package substrate structure must be reinforced with a compelling need to improve product performance, minimize product size, or meet stringent operating environmental concerns. Companies have found that embedding components is not a trivial endeavor and should include a strong and reliable support group of experienced suppliers. This is because there will be a significant amount of preparation required

when embedding the semiconductor element into the layer structure of the circuit board or package substrate.

The developer must first determine the most efficient method for the electrical interface of the die element. For example, the initial semiconductor fabrication process commonly furnishes an aluminum bond pad that is compatible with traditional gold wire-bond interface processing. However, when alternative direct surface interface methods are required, the semiconductor terminals must be furnished with an alternative alloy that is compliant with the selected attachment material or interface method.

Furthermore, with larger and high I/O semiconductors, it is often necessary to add metalization onto the die surface to accommodate the redistribution for the closely spaced peripherally located terminal sites to a wider-spaced and more uniform row and column, array pattern. The separation of the array pattern configured terminals will better accommodate circuit routing efficiency.

There are a number of methods successfully utilized for interconnecting the uncased semiconductor components. Some processes have



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Material Management is now one of the biggest challenges of Electronics manufacturers. This is due to the ongoing shift to high-mix, low/mid volume manufacturing with smaller lot-sizes batches and the significant cost of materials in PCB assembly.

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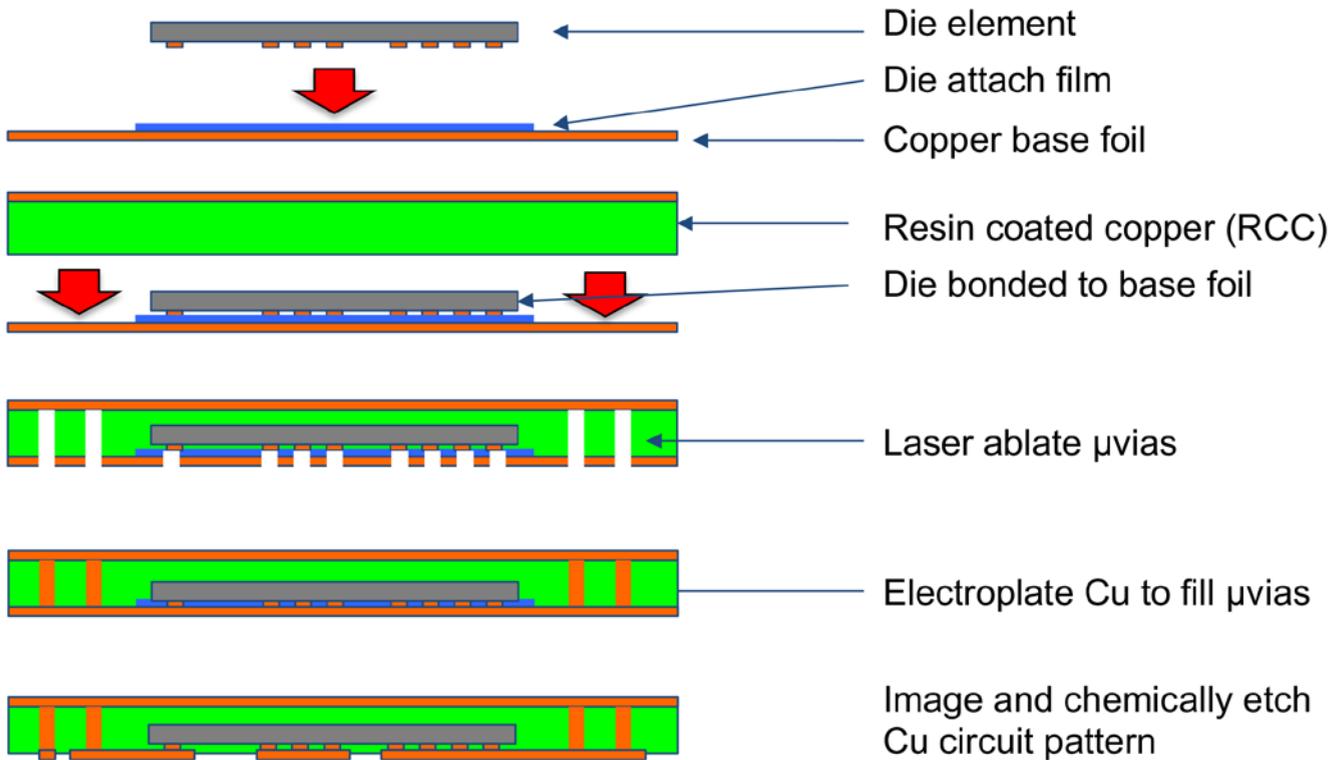


Figure 1: Die first coreless assembly process sequence.

evolved through joint development programs between a number of government and industry organizations and technical universities. In addition to these joint development programs, several independent laboratories and package assembly service providers have successfully developed a number of proprietary processes for embedding the uncased bare die elements. Without encroachment into proprietary technical detail, a general overview of process variations can be offered here.

Facedown and Face-up Process Variations

The semiconductor(s) may be mounted onto a designated layer of the core substrate in a face-up orientation or with the active surface facing down. Facedown mounting is typically selected for direct interface to a pattern of mating terminals on the circuit structure's core surface. Semiconductors that are furnished with raised alloy terminals will rely on some form of flip-chip attachment processing. For example, semiconductor die with wire-bond sites greater than 400 microns may

be furnished with alloy or conductive polymer bump features for termination. However, when the terminal spacing on the die is less than 400 microns, companies may consider implementing a selective plating process to furnish small solid copper pillars.

Attaching the semiconductor with the active surface of the die facing up is preferred for wire-bond processing or microvia termination. In preparation for wire-bond termination, a recessed area or cavity is generally provided in the substrate to afford clearance for both die attach and terminal interface. Following the wire-bond process, the cavity will be filled during the subsequent buildup layer lamination procedure.

When employing the microvia interface process, the thinned die element is first bonded onto the surface of the designated core circuit layer. In preparation for microvia termination, the terminal sites on the semiconductor must be furnished with a copper surface. Following the placement and lamination encapsulating the die element, laser systems are employed to

ablate material at each terminal site, followed by a sequence of plating, imaging, and etching processes to complete the interface from the die to the buildup circuit layer.

Microvia interface methodology is favored by a growing number of companies because they can eliminate several process steps: material dispensing, thermal curing or reflow processing, cleaning, and underfill application. Although the core-mounted semiconductor element described above is a popular technique for embedding active die, a number of innovative coreless embedding methodologies have evolved.

International Package Innovation

Several companies in Europe, Taiwan, Japan, and Korea have successfully embedded semiconductors in a broad range of products. A consortium of industry and Academia in Europe, for example, developed and refined what they call the “die first” assembly method. The process begins with first embedding then interconnecting the semiconductor die elements, a variation of the Occam Process extensively promoted by Joseph Fjelstad, the distinguished innovator.

As described by the developers, the process begins with laser marking fiducial targets on the surface of an ultra-thin copper foil that serves as a base layer. A pattern of adhesive material that is slightly larger than the semiconductor outline is then printed onto the copper surface and partially cured to furnish a stable tacky surface for device attachment. Using the fiducial target features on the copper surface as a guide, the component(s) is(are) placed into the partially cured adhesive pattern with the copper-plated terminal features of the die facing down.

A thermal curing process follows to complete the bonding of the semiconductor element to the copper foil base. Resin-coated copper (RCC) foil is next laminated over the backside of die, encapsulating the element, followed by a microvia ablation and plating procedure similar to that outlined previously. Additional circuit layers are sequentially added to complete interconnects to components mounted on the

outer surface(s) of the substrate or printed circuit board or package substrate.

Outsourcing Embedded Semiconductor Processing

In addition to processing the circuit board or package substrate, the designated PCB fabricator must be prepared to perform precise die attachment, have process capability for implementing a wide range of interconnect methods, and provide full functional electrical test of the embedded semiconductors at the substrate level.

Key issues to be addressed include:

- Procurement of semiconductors in a wafer format
- Outsourcing wafers for process-compatible metallization and thinning
- Singulation process capability and bare die handling systems
- Precise die placement and in-process termination capability
- Electrical testing of the active embedded semiconductor

Three questions that will need clarification are:

- How should you test?
- What should you test?
- What features are needed to enable testing?

Ideally, the originating companies will bring together the two primary suppliers: the circuit board fabrication specialist and the assembly service provider. **SMT007**



Vern Solberg is a technical consultant specializing in SMT and microelectronics design and manufacturing technology. He has served the electronics industry for more than 35 years in areas related to both

commercial and aerospace electronic product development and is active as an author and educator, focusing on technical issues related to PCB and flexible circuit design with an emphasis on electronic manufacturing using surface mount and related microelectronic components. [Read past columns or contact Solberg.](#)

Sharpening Your Organization's Competencies

Operational Excellence
by Alfred Macha, AMT PARTNERS

Successful organizations invest in developing their employees into high performers and continuously recruit top talent to join the organization. These actions require effort and commitment from the organization's leadership, given that employee development and strategic recruitment is a journey of growth and long-term sustainability where a positive return on investment may take years to realize.

The foundation of a successful employee development program is to evaluate and sharpen your employees' competencies and recruit prospective candidates that possess the desired competencies for which that you are looking. In this column, I will provide an approach on how to develop an employee development program driven by competencies.

How Is Competence Defined?

Competence is constructed from three elements: skill, knowledge, and attribute ^[1]. A

skill is something you do well—your ability to choose and perform the right technique at the right time. It's usually developed through training and practice. For example, you could become a skilled writer by practicing writing in a particular style, and you can become skilled at being safe in the workplace by practicing techniques during classroom exercises or labs.

Knowledge is information you know—including theories, facts, and procedures—and the ability to apply this information in different situations. For instance, you could have knowledge about different communication styles, or you may know the key steps to plan a program or project and be well-versed in strategies for evaluating success.

An attribute is an inherent characteristic or quality and is often expressed through what you think, do, and feel. For example, you could be known for staying positive and calm in chal-



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lenging situations. You may also bring a can-do attitude to your work.

Leadership Competencies

It starts at the top. Harvard Business Review did a survey with 195 global leaders who were asked to rate 74 leadership qualities [2], and 10 leadership competencies rose to the top (Table 1). Your organization should prepare an assessment to evaluate your leadership competencies strengths to these top 10 leadership skills and prepare a development plan to strengthen these top competencies as needed within your executive team.

Develop a Framework of Key Competencies for All Employees

Your company culture is defined by core values. The core values will define the DNA of your organization, and employees will demonstrate behaviors that are aligned to those core

values. The second component to strengthen your culture is to have a well-defined set of competencies that your organization values in its employees and prospective candidates that will join the company.

Here is an assessment tool based on 38 core competencies defined by Korn Ferry’s research guide and technical manual [3]. These competencies are grouped into factors. The goal is for your executive team to designate a weighted score for each competency. This allows you to provide higher value to a given competency that supports your customers’ values and vision (Table 2).

Once you have built the evaluation tool, you should evaluate each employee to identify areas where improvement is needed. This tool should be a positive and collaborative exercise between a manager and an employee. Employees appreciate seeing the areas where they need to improve on to achieve a high level of consistent performance.

Top 10 Leadership Competencies



Table 1: Top 10 leadership competencies.

Factor	Competence	Weighted Value	Evaluation Score	Weighted Score
Results	Ensures accountability			
	Plans and aligns			
	Drives results			
	Directs work			
	Resourceful			
	Optimizes work processes			
	Action-oriented			
Thought	Manages complexity			
	Cultivates innovation			
	Decision quality			
	Strategic mindset			
	Global perspective			
	Business insight			
	Customer focus			
	Financial acumen			
	Tech savvy			
Balances stakeholders				
Self	Nimble learner			
	Courageous			
	Situationally adaptable			
	Resilient			
	Demonstrates self-awareness			
	Instills trust			
	Manages ambiguity			
	Self-development			
People	Attracts top talent			
	Persuades			
	Builds networks			
	Drives vision and purpose			
	Builds effective teams			
	Drives engagement			
	Communicates effectively			
	Manages conflict			
	Organizational savvy			
	Develops talent			
	Interpersonal savvy			
	Values differences			
	Collaborates			

Table 2: Key competencies.

Legend: Table 2

- Factor = Area of evaluation that consists of several competencies
- Competency = Competency definition that will be assessed
- Weighted value = The value given by the executive team to that competency
 1. Low
 2. Medium
 3. High
- Evaluation Score = The assessment value given to an employee for that competency
 1. Not adequate
 2. Adequate
 3. Meets
 4. Exceeds
- Weighted score = Evaluation score * Weighted value

Hire Talent Based on Desired Competencies

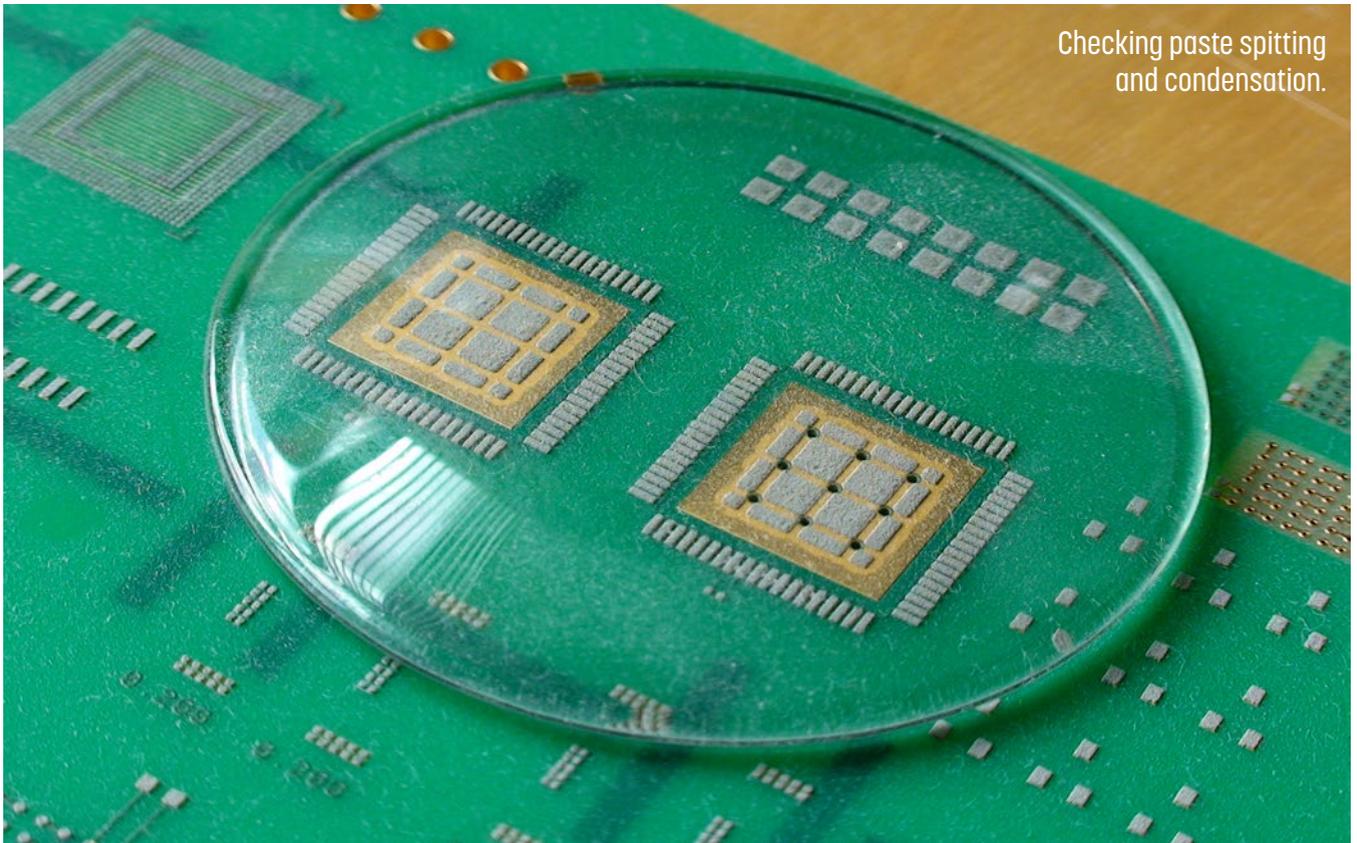
Once you have defined a competencies framework and evaluated your workforce, the next step is to recruit and hire new employees by evaluating their competency level to this framework. This allows you to have an objective and quantitative approach to your hiring strategy. Develop an interview worksheet that uses the competencies in the framework. Given the limited time during the interview time that you have with a prospective candidate, I suggest you select a minimum of 10 critical competencies that are most relevant to the position you are hiring for and assess your candidates with those selected competencies. **SMT007**

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1. CGMA, "CGMA Competency Framework: 2019 Update," 2019.
2. S. Giles, "The Most Important Leadership Competencies, According to Leaders Around the World," *Harvard Business Review*, March 15, 2016.
3. Korn Ferry, "Korn Ferry Leadership Architect: Global Competency Framework—Research Guide and Technical Manual," 2014-2017.



Alfred Macha is the president of AMT Partners. He can be reached at Alfred@amt-partners.com. To read past columns or contact Macha, [click here](#).



Checking paste spitting
and condensation.

Solder Paste **Evaluation** and Simple Tricks of the Trade

Article by Pete Starkey
I-CONNECT007

“I’m a hands-on person who likes to do hands-on stuff to understand technology and how defects occur.” This was how Bob Willis described his personal methodology as he presented a comprehensive and informative online webinar on solder paste basics. A specialist in PCB soldering processes, design for manufacturing, and failure analysis since his early days with GEC-Marconi, Willis has been involved with the introduction and implementation of lead-free soldering technology since the turn of the century, providing “how to do it,” hands-on, lead-free training workshops and winning awards from SMTA and IPC for his industry support.



Bob Willis

“Solder paste quality and performance is important, and considerable engineering goes into its production. Selecting the best materials for your product and assembly process is key to high yield and your customers’ satisfaction,” said Willis. He continued, “Solder paste must be compatible with your equipment and other processes you use like cleaning, coating, and electrical testing. Working with suppliers to achieve the best performance is vital, but so is a periodic review of materials used. There are always improvements being made to printing and jetting technology, and it is important that engineers consider if there are technical or commercial reasons to change. We look at common testing methods and some of the simple shop floor techniques used over the years to understand the different types of process failures.”

Based on his own industry surveys, Willis had ascertained that solder paste printing and reflow soldering accounted for a substantial proportion

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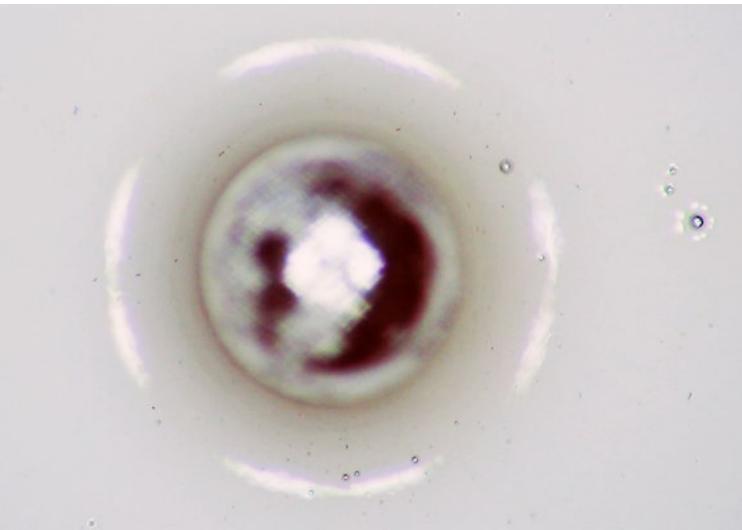
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Solder balls after reflow.

of defect levels in surface mount assembly, and he set out to explore and explain basic facts and to suggest practical test methods. “Understand the materials and the differences in the materials that are offered to you. Let’s understand what’s actually happening with solder paste,” he said. Willis made it clear that all major suppliers to the industry provided good and consistent products, and that the variations or specific features of one product over another might be difficult to detect or just unique to a company’s specific requirement.

What classes of solder paste were available? Willis listed solder pastes for printing, dispensing, jetting, dipping, and rework and repair. He commented that most paste types were designed for a no-clean process, but because an increasing number of customers preferred to clean, then techniques were being developed for cleaning “no-cleans” and several pastes had been specifically designed to be cleaned. Regarding storage, provided stocks were carefully controlled first-in, first-out, and used within a few days. Refrigeration was generally not necessary, and containers of paste could more easily normalise in the production environment.

Stencil printing had been established as the standard application technique, but as features became finer, dispensing and jetting had become increasingly used as alternatives: they’re slower but independent of hard tool-

ing and adaptable to very small batch sizes. Dipping paste was very fluid and exceptionally good for rework and repair on area-array packages. The component was dipped in the paste and placed on the substrate.

Willis showed illustrated examples of jetting and dipping for package-on-package assembly and rework, using video clips to demonstrate joint formation with traditional j-lead and gull-wing packages. He described a video reflow simulation technique capable of replicating the profile of a convection reflow oven, permitting direct monitoring of actual assemblies with LGA and QFN packages. The addition of X-ray enabled the technique to be used for process optimisation and fault-finding on area-array packages. X-ray simulation was also effective in characterising the formation and movement of voids, particularly in inaccessible areas, such as via-in-pad or underfill, where there was no direct escape route. It was also useful for studying the characteristics of pin-in-hole intrusive reflow.

Next, Willis described simple but effective methods for a quick, initial assessment to characterise the property or effect and understand the nature of the problem and its probable causes before spending time and money carrying out an in-depth investigation. In many cases, these simple, shop-floor test methods had been used in the industry for solder paste evaluation since the pioneering days of SMT. Semi-automatic equipment was now available for testing solder paste in line with IPC standards, which allowed solder paste tack and slump, wetting, and solder-balling to be assessed and measured under a microscope and recorded on video.

In the absence of specialised equipment, an effective shop-floor comparison test to give an indication of initial tack and usable tack-time was to print a series of paste samples, place representative components after various time intervals, tilt the substrate to a steep angle, and observe any slippage or loss of adhesion. Willis commented that some pastes could maintain their tack for several days after printing. It was interesting to observe the extent to which components could move out of position as the

assembly entered the reflow zone. Provided the movement was not excessive, surface tension would pull them back into place as the solder joints were formed, but in cases where the substrate was thin or flexible, supporting pallets were necessary to maintain yield.

Willis demonstrated a simple test involving printing dots of solder paste on ceramic tiles with an etched stencil and using a microscope and video camera to observe and record their behaviour when reflowed at 250°C. His video examples showed two different pastes compared for solder-balling, one considerably better than the other, although he commented that present-day paste formulations displayed less tendency to balling effects. A somewhat more elegant test was to print paste onto the copper sheet through a stencil based on J-STD-005 apertures chosen to represent the most difficult features of the design. The IPC-TM-650 Test Methods Manual listed a series of tests for solder paste, including powder size, metal content, viscosity, slump, solder-balling, tack, and wetting.

Further, a series of joint industry reference standards (J-Standards) had become established as the predominant authority for electronics assembly manufacturing worldwide. IPC J-STD-001 covered requirements for soldered electrical and electronic assemblies, describing materials, methods, and verification criteria. IPC-J-STD-004 covered requirements for soldering fluxes with IPC-J-STD-005 addressing soldering pastes and IPC-J-STD-006 covering solder alloys.

Having discussed phenomena such as spitting and solder spotting and a technique for observing them using a watch glass, Willis considered ways in which solder paste residues could be assessed, initially by using glass slides to simulate component stand-off height and enable the performance of cleaning systems to be monitored. Large components presented particular challenges. For example, after surface insulation resistance (SIR) testing, it was difficult to optically inspect without

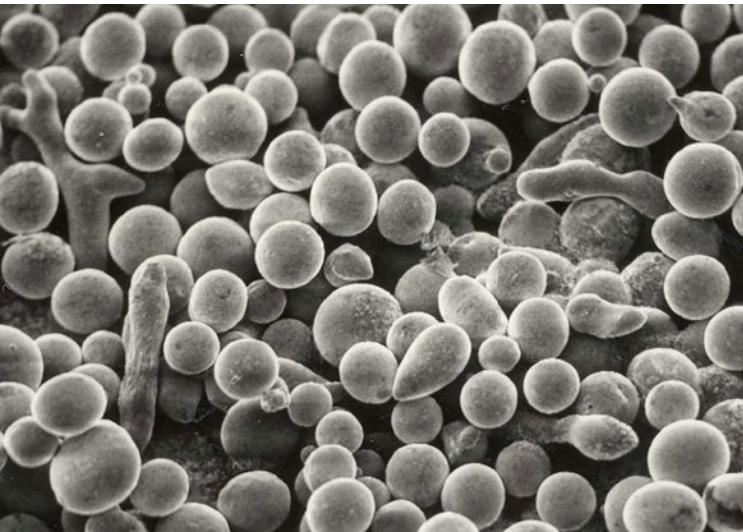
removing components and possibly destroying evidence of dendrites. X-ray or back-grinding were possible alternatives. He showed video illustrations of dendrite formation and examples of good and bad SIR traces.

Willis examined some of the details of solder paste printing with reference to the requirements of the IPC-7527 standard for positional accuracy and shape of deposit and demonstrated simple test procedures using plastic film overlays for trial prints to minimise wastage of test coupons or production PCBs. Turning his attention to the assessment of solderable finishes on PCBs, he described the solder spot test pattern he had developed in cooperation with the National Physical Laboratory, which could be used either to compare the solderability of different finishes under different conditions, or, alternatively, to assess the wetting characteristics of solder pastes or to compare reflow cycles.

Willis also discussed “over-printing” in the context of pin-in-paste through-hole-reflow technology, where it was necessary to print a large amount of paste on to the pads in order to fill the complete plated-through-hole with solder, but the pad size was not large enough for the total volume required. The technique was to print over-size, beyond the immediate pad



Poor paste release from stencil apertures.



Solder paste particles from the 1980s were not good.

area, and onto the solder mask. Precise control was vital to avoid solder-balling. Solder paste print inspection was becoming a critical operation in the surface mount assembly process, and state-of-the-art 3D systems were capable of measuring height, volume, and area of paste deposits, computing stencil offsets and detecting defects such as bridges and missing features.

Willis concluded his presentation with an introduction to low-temperature, lead-free sol-

der alloys and pastes. Alloys were based on tin-bismuth or tin-bismuth-silver, melting in the range of 138–140°C, and with typical peak-reflow temperatures in the range of 160–170°C. His experiences of early versions were that they had a tendency to slump, could display a range of particle sizes and shapes, and could exhibit minor solder-balling. However, they were useful for heat-sensitive assemblies and were sometimes used in conjunction with SAC305 alloys.

A lively Q&A session occupied the next half-hour, with Willis responding to queries on tack testing, cleaning chemistries, printing problems, temperature profiling, stencil design, mechanical support of assemblies, ESD control, and intrusive reflow. “All good fun, and I get to play as well!” With his encyclopaedic knowledge and emphasis on practical process assessment to help attendees gain a proper understanding of the problem and get the most out of basic common-sense methods—before turning to more elegant and expensive instrumental techniques and his extensive collection of unique video clips to illustrate and demonstrate every aspect—Bob Willis’s relaxed and entertaining style provided an exceptional learning experience. **SMT007**

Aerojet Rocketdyne CEO and President Eileen Drake Selected to Serve on National Board of Directors of Girl Scouts of the USA

“We’re pleased to welcome Eileen Drake to our Board of Directors,” said GSUSA National Board President Kathy Hopinkah Hannan. “Eileen is an extraordinary businesswoman who has served our nation first as an Army aviation officer and now as a leader in the aerospace and defense industry. Her leadership experience will be of tremendous value to our organization as it forges ahead into a dynamic future.”

Girl Scouts is the nation’s preeminent leadership development organization for girls, with programs from coast to coast and across the globe.

“I am honored to be selected to serve on Girl Scouts’ National Board of Directors,” said Drake. “Over its 107-year history, Girl Scouts has made huge contributions to

the development of girls as leaders and citizens. With our nation’s growing needs in STEM, leadership and diversity, this organization’s work is more important than ever.”

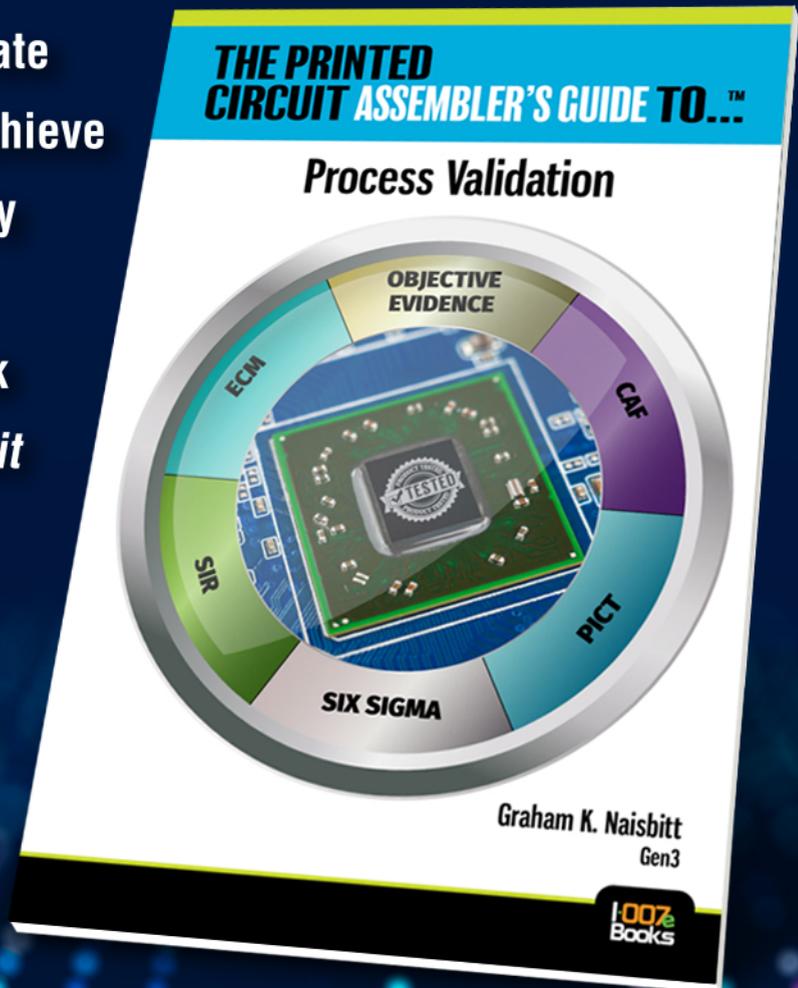
Drake joined Aerojet Rocketdyne in March 2015 as chief operating officer. A former Army aviation officer, Drake also worked in leadership roles at Ford Motor Company and United Technologies. Since becoming CEO at Aerojet Rocketdyne, Drake has overseen a fundamental reorganization of the company, creating efficiencies and developing new capabilities.

Drake also serves on the board of Woodward Inc., as well as the Board of Governors and Executive Committee of the Aerospace Industries Association. Throughout her career, Drake has been passionate about promoting STEM initiatives and advancing the work of Girl Scouts.



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Editor's Picks from SMT007.com

1 Quest for Reliability: Old Dogs, New Tricks ▶

Eric Camden hears two phrases way too often on a production floor: “We have always done it this way.” But times change, and technology changes even faster, and if you don’t keep up, you will be left behind. Camden explains how these phrases are not very helpful regarding reliability, and how you should focus on emerging technologies and the associated risk that may be unique to that package.



Eric Camden

2 IPC Government Relations Team Offering Education and Fun at IPC APEX EXPO ▶

Your IPC Government Relations team is preparing a variety of activities to educate and engage you on these issues. IPC’s Chris Mitchell discusses some of the highlights attendees will see at IPC APEX EXPO from a government relations perspective.

3 Powerful Prototypes: Five Technological Shifts in the New Decade ▶

Depending on your perspective, we are either starting the last year of the old decade or starting the first year of the new decade. But regardless of what you call the decade, a lot of change is in store. Duane Benson shares five of the more significant technological shifts directly ahead of us and how to respond.



Duane Benson

4 What You Need to Know About the Digital Factory ▶

Barry Matties spoke with Oren Manor, director of business development for Mentor, A Siemens Business, during productronica about the many benefits of a digital factory and what’s keeping companies from becoming one. Oren also gives examples of big data analytics along with the move to a lot size of one.



Oren Manor

5 Smart Factory Insights: What You No Longer Need to Learn ▶

Naturally evolving layers of technological applications allow us to build and make progress, layer by layer, rather than staying relatively stagnant with only incremental improvement. To gain ground in manufacturing, Michael Ford explains how we need to embrace next-layer hardware and software technologies now so that we can focus on applying these solutions as part of a digital factory.



Michael Ford

8 Engaging STEM Students at IPC APEX EXPO 2020 ▶

At this year's IPC APEX EXPO, you're likely to see quite a few high school students moving amongst all the normal show activities thanks to the IPC APEX EXPO STEM Outreach Program. Launched two years ago at IPC APEX EXPO 2018, the 2020 version of the STEM Outreach Program will be larger and more immersive than ever before.



Gunter du Plessis

6 Updates on Cleaning Standards and Committees ▶

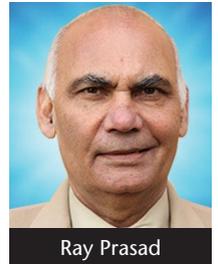
Graham Naisbitt of Gen3 discusses the changes he sees in cleaning, including how the WP-019 white paper has caused a closer look at electrochemical reliability. As a long-time head of committees, Graham also breaks down many of the topics he hopes are addressed at this year's IPC APEX EXPO.



Graham Naisbitt

9 SMT Solver: Choosing the Right Defect ▶

Ray Prasad addresses some key issues that are important for all of us to be aware of and learn about, especially for managers in SMT assembly and engineers who aspire to be future managers. Topics covered include choosing the right defect and developing a DFM and process recipe.



Ray Prasad

7 Zulki's PCB Nuggets: Successful PCB Microelectronics Assembly ▶

In addition to coverage of PCB microelectronics subjects, Zulki Khan addresses one of the most crucial areas: PCB fabrication that creates the circuit board undergoing microelectronics assembly. The burning question is, "Why is fabrication vitally important when it comes to successful microelectronics assembly?"



Zulki Khan

10 Digi-Key Electronics Supports Startups With CES 2020 Activities ▶

At CES's Eureka Park, Digi-key launched its Startups Survival Guide, which features tools, resources, and first-hand accounts from successful startups to help guide innovators in their journey from ideation through production and beyond.



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Career Opportunities



CAM Engineer

Eagle Electronics is seeking a CAM engineer specific to the printed circuit board manufacturing industry. The candidate should have a minimum of five years of CAM experience and a minimum of two years of experience in Frontline InCAM software. The candidate should also be fluent in PCB and CAM language pertaining to customer and IPC requirements. The ideal candidate has experience with scripting Frontline InCAM software.

This is a first-shift position at our Schaumburg, Illinois, facility; this is not a remote/off-site position. Any offer would include relocation costs to the Schaumburg, Illinois, area along with competitive salary and benefits.

If interested, please submit your resume to HR@eagle-elec.com and include "CAM Engineer" in the subject line.

About Eagle—Since 1979, Eagle Electronics has provided customers with the highest quality printed circuit boards at fair and competitive prices. From providing customers with short standard lead times to very low premiums on quick turns, Eagle strives to provide the best total value in high technology rapid turn-around PCBs in the industry.

[apply now](#)



West Software Application Engineer

This position reports directly to the Orbotech West software support manager and works with customers to support Orbotech's pre-production software products. Acts as a focal point for technical issues, manages product implementation projects, provides customer training, and supports the sales process. Advanced knowledge of Frontline PCB products, including InCam, InPlan, InStack, InSight, Genesis, and Genflex. Ability to travel and manage time to maximize results. Requires both written and oral technical communication skills. Skilled in the use of scripting languages, including C-Shell, Perl, or Python. Knowledge of relational databases and HTML/XML highly desirable. Knowledge of PCB manufacturing processes. Familiar with the processes used in front-end engineering departments at PCB fabrication sites. Requires use of project management skills to organize and complete projects that involve the implementation of sophisticated software tools used in printed circuit fabrication facilities.

An expected average of 35%+ travel. College degree or equivalent technical education, in addition to a minimum of five-plus years of related experience. Experience supporting sales and sales activities is a plus. U.S. citizen with the ability to work and travel within the U.S., Canada, and internationally.

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Career Opportunities



ventec
INTERNATIONAL GROUP
騰輝電子

OEM Sales Manager Chicago/Home-Office-Based

Want to advance your career by joining a globally successful and growing world-class CCL manufacturer and help drive that success? We are seeking to hire an OEM sales manager to grow and manage key customer accounts with OEM's and Tier 1 manufacturers in the USA, focusing on Ventec's core market segments: mil/aero, automotive, and medical, offering a full range of high-reliability materials, including polyimide, IMS, and thermal management products.

Skills and abilities required for the role:

- Non-negotiable: Drive and tenacity!

Required:

- 7 to 10 years' experience in the PCB industry in engineering and/or manufacturing
- Detail-oriented approach to tasks
- Ability to manage tasks and set goals independently as well as part of a team
- Knowledge of MS office products

Full product training will be provided.

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits.

Please forward your resume to
jpattie@ventec-usa.com and mention
"Technical Sales Engineer—Chicago"
in the subject line.

[apply now](#)



Sr. PCB Designer—Mentor Xpedition

Freedom CAD is a premier PCB design service bureau with a talented team of 30+ dedicated designers providing complex layouts for our enviable list of high-tech customers. Tired of the commute? This is a work-from-home, full-time position with an opportunity for additional compensation for overtime work at time and a half.

Key Qualifications

- EXPERT knowledge of Xpedition VX 2.x
- Passionate about your PCB design career
- Skilled at HDI technology
- Extensive experience with high-speed digital, RF, and flex and rigid-flex designs
- Experienced with signal integrity design constraints encompassing differential pairs, impedance control, high speed, EMI, and ESD
- Excellent team player who can lead projects and mentor others
- Self-motivated with the ability to work from home with minimal supervision
- Strong communication, interpersonal, analytical, and problem-solving skills
- Other design tool knowledge is considered a plus (Altium, Allegro, PADS)

Primary Responsibilities

- Design project leader
- Lead highly complex layouts while ensuring quality, efficiency, and manufacturability
- Handle multiple tasks and provide work leadership to other designers through the distribution, coordination, and management of the assigned workload
- Ability to create from engineering inputs, board mechanical profiles, board fabrication stackups, detailed board fabrication drawings and packages, assembly drawings, assembly notes, etc.

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Career Opportunities



Advanced Connectivity Solutions

Senior Development Engineer

Rogers Corporation is seeking a senior development engineer accountable for the development of more complex products and processes, the establishment of sound technical bases for these developments, and effective interaction with technology, process, and platform innovation; operations; sales and marketing; and process engineering personnel to commercialize these developments.

Essential Functions:

- Design and conduct experiments and interpret the results
- Report on projects in both written and verbal formats at all levels of the organization
- Perform technical troubleshooting of new products and processes; act as new product/concept incubator for new technologies and platforms, identifying opportunities for improvement and incorporation design for manufacturing requirements resulting in a viable, scalable product
- Provide ongoing process and manufacturing support to newly launched products as applicable
- Provide support in terms of analytical equipment maintenance, methods development, material analysis, and documentation of new process or products
- Manage capital projects for the purchase and installation of new process or support equipment; train employees in new processes

Required Education and Experience:

Ph.D., Ch.E., M.E., or material science, or B.S. or higher in a technical discipline with accomplishment in product development and project management.

Rogers Corporation provides equal employment opportunities to minorities, females, veterans, and disabled individuals as well as other protected groups.

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Gardien Is Hiring!

The Gardien Group, a leading solutions provider in the PCB industry, is looking to fill multiple openings in their China, Japan, Taiwan, and United States service centers.

We are looking for electrical engineers, operations managers, machine operators, and sales executives. Prior experience in the PCB industry is beneficial but not essential. Training will be provided along with excellent growth opportunities, a benefits package, and periodic bonuses.

Our global teams are from diverse cultures and work cohesively as a tight-knit unit. With performance and initiative, there are plenty of opportunities for professional growth.

Gardien is an equal opportunity employer. Employment decisions are made without any regard to race, color, religion, national or ethnic origin, gender, sexual orientation, age, disability, or other characteristics.

Interested candidates, please contact us with your resume and a cover letter. Kindly note that only shortlisted candidate will be contacted.

[Apply at careers@gardien.com.](mailto:careers@gardien.com)

[apply now](#)

Career Opportunities



eptac

TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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Technical Account Manager Chicago/Minneapolis

Insulectro, the largest national distributor of printed circuit board materials, is seeking a talented sales superstar for a Technical Account Manager role based out of either our Chicago or Minneapolis office. This role will focus on maintaining the existing customer base and developing new business within the assigned territory in both the printed circuit board and printed electronics industries. We are looking for the perfect fit of education, experience, and attitude that matches our company culture and enhances the service level to our customers.

Qualifications:

- A self-motivated business professional who is driven to succeed with a minimum of 3 years outside sales experience in the PCB or PE industry
- Proven sales/business development record
- Excellent communication and interpersonal skills
- OEM and electronic assembly experience is a plus

We offer:

- Competitive salary and commission plan with a comprehensive benefits package
- A fun, high-energy company with an entrepreneurial spirit
- A great group of people to work with!

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Career Opportunities



APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

[apply now](#)



Development Chemist Carson City, NV

Develop new products and modify existing products as identified by the sales staff and company management. Conduct laboratory evaluations and tests of the industry's products and processes. Prepare detailed written reports regarding chemical characteristics. The development chemist will also have supervisory responsibility for R&D technicians.

Essential Duties:

- Prepare design of experiments (DOE) to aid in the development of new products related to the solar energy industry, printed electronics, inkjet technologies, specialty coatings and additives, and nanotechnologies and applications
- Compile feasibility studies for bringing new products and emerging technologies through manufacturing to the marketplace
- Provide product and manufacturing support
- Provide product quality control and support
- Must comply with all OSHA and company workplace safety requirements at all times
- Participate in multifunctional teams

Required Education/Experience:

- Minimum 4-year college degree in engineering or chemistry
- Preferred: 5-10 years of work experience in designing 3D and inkjet materials, radiation cured chemical technologies, and polymer science
- Knowledge of advanced materials and emerging technologies, including nanotechnologies

Working Conditions:

- Chemical laboratory environment
- Occasional weekend or overtime work
- Travel may be required

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Career Opportunities



Multiple Positions Available

The Indium Corporation believes that materials science changes the world. As leaders in the electronics assembly industry we are seeking thought leaders that are well-qualified to join our dynamic global team.

Indium Corporation offers a diverse range of career opportunities, including:

- Maintenance and skilled trades
- Engineering
- Marketing and sales
- Finance and accounting
- Machine operators and production
- Research and development
- Operations

For full job description and other immediate openings in a number of departments:

www.indium.com/jobs

apply now



SMT Field Technician Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

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Career Opportunities



U.S. CIRCUIT

Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

- Candidates must have previous PCB sales experience.

Compensation:

- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

[apply now](#)



ZENTECH

Zentech Manufacturing: Hiring Multiple Positions

Are you looking to excel in your career and grow professionally in a thriving business? Zentech, established in Baltimore, Maryland, in 1998, has proven to be one of the premier electronics contract manufacturers in the U.S.

Zentech is rapidly growing and seeking to add Manufacturing Engineers, Program Managers, and Sr. Test Technicians. Offering an excellent benefit package including health/dental insurance and an employer-matched 401k program, Zentech holds the ultimate set of certifications relating to the manufacture of mission-critical printed circuit card assemblies, including: ISO:9001, AS9100, DD2345, and ISO 13485.

Zentech is an IPC Trusted Source QML and ITAR registered. U.S. citizens only need apply.

Please email resume below.

[apply now](#)

Career Opportunities



BLACKFOX

Premier Training & Certification

IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

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AD
HERE

For information, please contact:
BARB HOCKADAY
barb@iconnect007.com
+1 916.365.1727 (PACIFIC)

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Events Calendar

IPC APEX EXPO 2020 ▶

February 1–6, 2020
San Diego, California, USA

Pan Pacific Microelectronics ▶

February 10–13, 2020
Big Island, Hawaii, USA

The LED Show ▶

February 11–13, 2020
San Diego, California, USA

Embedded World ▶

February 25–27, 2020
Nuremberg, Germany

WIN EURASIA (Electrotech) Tüyap Fair Convention and Congress Center ▶

March 12–15, 2020
Istanbul, Turkey

Electronica China ▶

March 18–20, 2020
Shanghai, China

Semicon China ▶

March 18–20, 2020
Shanghai, China

LOPEC Exhibition and Conference ▶

March 24–26, 2020
Munich, Germany

SAMPE 2020 ▶

May 5–6, 2020
Seattle, Washington, USA

SMTconnect ▶

May 5–7, 2020
Nuremberg, Germany

Additional Event Calendars



Coming Soon to *SMT007 Magazine*:

MARCH 2020: Digital Factory Implementations

The value side of the digital factory, from implementation to profitability, implementation, resources, and designing, including how to know when and why to implement the model.

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