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MAY 2013

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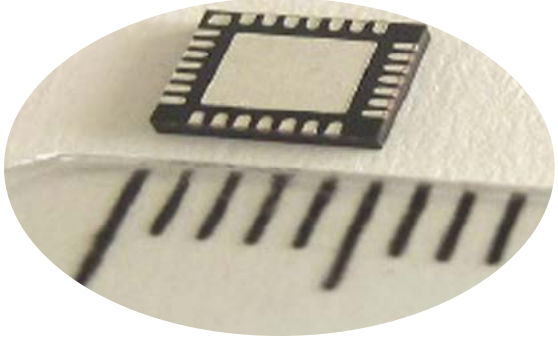
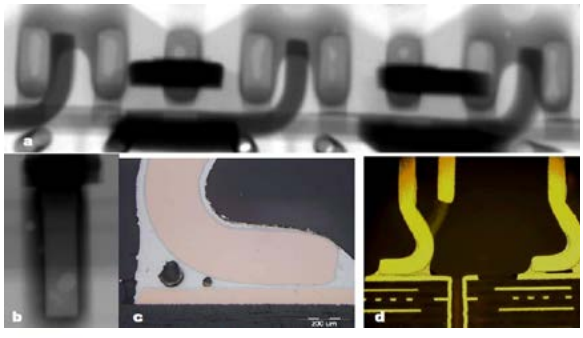
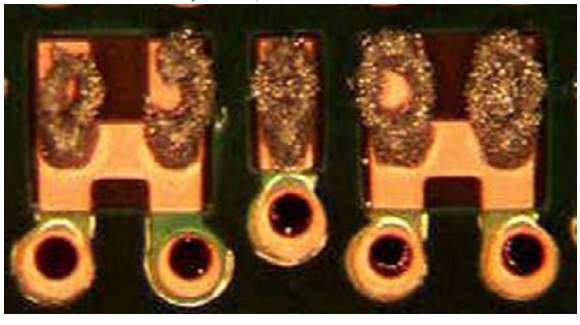
May 2013 Featured Content

SMT Assembly Processes, Part 2: SOLDERING TECHNOLOGY

The May issue of *SMT Magazine* focuses on soldering issues, including voiding in QFN packages and gull wing joints, the formation of tin whiskers, solder capacity, and lead-free soldering. The issue features authors from Rehm Thermal Systems and Balver Zinn who examine the surface tension and load-carrying capacities of solder and Seth J. Homer and Dr. Ron Lasky of Indium who discuss ways to reduce voiding in QFN packages. Additional articles and columns from industry experts, including, Dr. Jennie Hwang, Zulki Khan, Sjef van Gastel, Karla Osorno, and new columnist Rachel Short can be found in the issue as well.







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MAY 2013
VOLUME 28
NUMBER 5
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THE WAY I SEE IT

Think Globally, Act Locally

by Ray Rasmussen
I-CONNECT007

SUMMARY: Serving two masters, IPC has to walk a fine line. Maybe the organization has to delineate itself a bit more, by region, so that it can better support its members in different parts of the world.

The Manufacturers Alliance for Productivity and Innovation (MAPI) issued a new econometric forecast model based on a report by The Aspen Institute in early April that shows "ample potential for U.S. manufacturing to undergo resurgence by 2025." Thomas J. Duesterberg, Aspen's executive director, stated, "The robust results presented in the study are achievable with only modest acceleration of current trends, and none of the policy recommendations mark a radical departure from current policy trajectories. But they require a willingness to change in a disciplined way."

The report goes on to give specifics:

• "The manufacturing share of value-added in the resurgence scenario would grow to 15.8% of GDP in 2025, a proportion not seen since 1998, compared to 11.1% in 2025 under the baseline forecast."

• "Manufacturing employment in the resurgence scenario would grow by 307,000 per year, or an increase of 3.7 million jobs by 2025, compared with essentially flat growth, or 23,000 workers per year, in the baseline scenario."

The 32-page report is worth taking a look at, especially if you're invested in U.S. manufacturing. It looks at trade, energy, and regulatory policy, in addition to labor force, taxes, and research. I haven't looked at all the issues

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THINK GLOBALLY, ACT LOCALLY *continues*

involved in something like this, but on the surface it sounds like it's doable and a good idea.

Divided Loyalties

I get a regular newsletter from MAPI. There's plenty of good stuff about U.S. manufacturing. Although I've never seen much about our industries, MAPI is all about supporting U.S. manufacturing. That's their charter. No confusion there.

That brings me to IPC. On the one hand, IPC's strong push into global markets makes a lot of sense to its globally-focused members. Having IPC on the ground in China, India, and elsewhere, to establish its standards and educational services and prepare the masses to build products for their global customers (and IPC member OEM, EMS, and PCB companies), seems to make a lot of sense. There's another side to this, though.

IPC's membership is made up of mostly small, regional manufacturers servicing domestic markets. They don't care that IPC is a global association and most believe they don't benefit from those efforts. In fact, many believe IPC's international focus hurts their businesses. The more educated and technically proficient foreign competitors become, the harder it is for a domestic manufacturer to compete. I would argue that globalization along with truly free trade (which is rare) will theoretically benefit even regionally focused manufacturers since the markets for their customer's products are increased by opening markets around the world, ultimately. If a domestic fabricator or EMS can offer the best value to their customers, then they will reap the benefits of the huge new markets opening up for their customers around the world.

Serving two masters, IPC has to walk a fine line. With many IPC board members representing multinational companies, there's a lot of pressure for IPC to have activities in the markets its members serve. Those members (board members) understand the importance of the markets around the world. They have based their business models on global business strategies. But what about the rest? Who's watching out for them?

It almost seems like it would be a conflict of interest these days for this now-global association to aggressively work to promote and support a business climate that would enhance the environment for manufacturing…in the U.S. only. What about members in other countries? Why should they pay dues to strengthen the U.S. manufacturers? It seems to be a conflict of sorts. IPC does invest in U.S. government relations programs, which are mostly focused on environmental issues or issues like conflict minerals. And IPC did spend resources to help with equipment depreciation recently, which helps lower costs for U.S. manufacturers, but does nothing for IPC dues payers in Malaysia, the UK, or Brazil.

Now, I know that the groups pushing IPC increasingly onto the global stage probably have two reasons for doing so. First, it's self-serving. They need a consistent playing field from which to operate around the globe. Second, IPC will become decreasingly relevant if it doesn't step up and play a strong role where electronics manufacturing is taking place. Having "our" association as a premier global organization on par with SIA, SEMI, etc., is ultimately good for our industry, here in the U.S.

It's Not New

The industry has been struggling for decades over IPC's forays into global markets. Even in the '80s and '90s, IPC was challenged by smaller members to not lose sight of the U.S. market and focus its efforts at home. Since IPC has been the de facto global industry association since the beginning, it has always been pulled to far corners of the globe by fledgling industries seeking support. IPC gladly sent its reps to

THINK GLOBALLY, ACT LOCALLY *continues*

give presentations and workshops. Those early trips helped lay some of the groundwork for the industries we see today.

This report got me thinking, again, about the importance of a national association that supports manufacturing in North America. Maybe IPC has to delineate itself a bit more, by region, so that it can better support its members in different parts of the world. IPC NA for example or IPC Europe could have a board made up of domestic fabricators, assemblers, and suppliers with its own domestic agenda. Certainly, aspects of that agenda would dovetail with what IPC Global is doing and vise-versa. Maybe this is already underway with IPC's recent hire of an IPC China president and vice president. But, as the IPC puts on a more universal face, it might be time to consider regionally autonomous leadership at the board level.

IPC President John Mitchell and his crew have been tasked with doubling membership. Much of that effort will be as a result of member satisfaction (perceived value from current members as well as from potential members). One way to do that is to be sure members feel the love and know that their investments into their association aren't all going overseas to educate and support their competitors. Giving smaller companies a home might be a great way to drive membership growth and truly offer domestic companies (wherever your "domestic" may be) a collective voice, responsive to their very specific needs. And, when we need it, we have IPC Global to quash the next lead-free initiative to come down the pike.

That's the way I see it. **SMT**

Ray Rasmussen is the publisher and chief editor for I-Connect007 publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine.* Contact Rasmussen here.

SMT PERSPECTIVES AND PROSPECTS

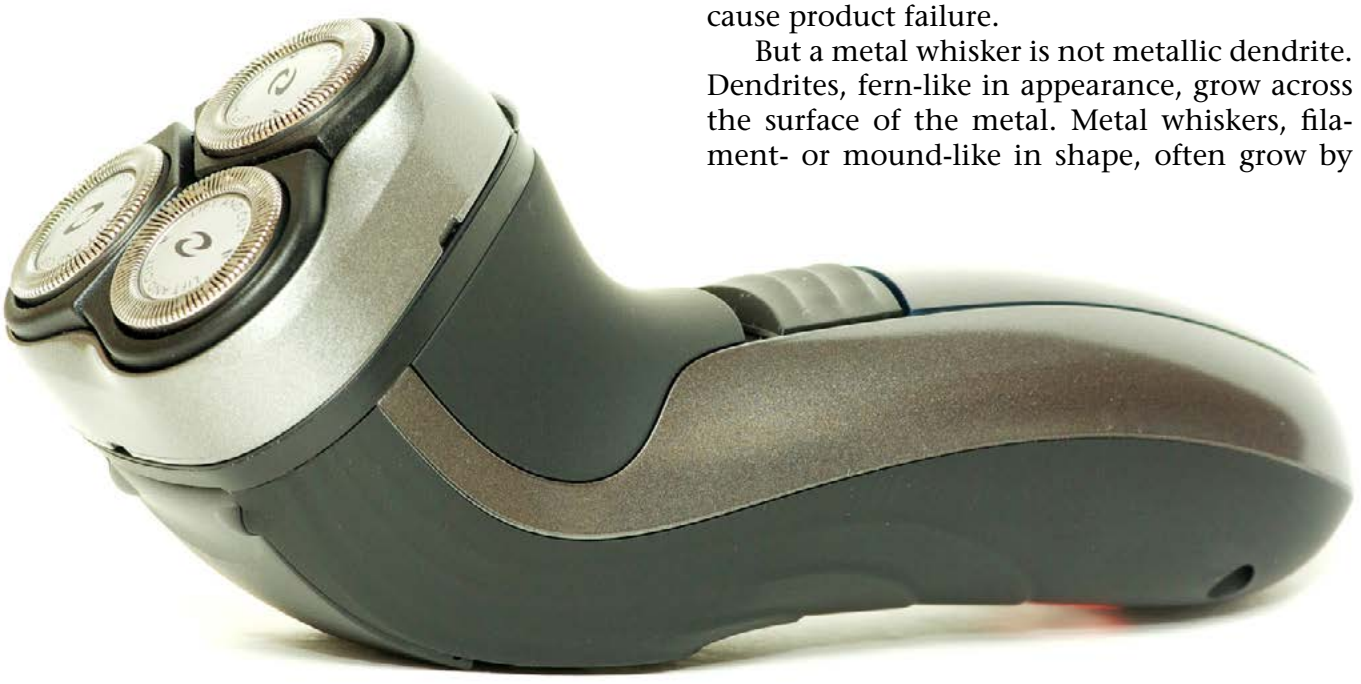
Tin Whiskers: Clarity First

by Dr. Jennie S. Hwang
H-TECHNOLOGIES GROUP

SUMMARY: Lead-free solder comprises a wide array of alloy systems and each system can be modified in numerous ways. A test scheme to represent lead-free is a daunting task with an astounding price tag. Dr. Jennie Hwang advises that any tin whisker propensity study be conducted with a specific alloy composition, as clarity is the name of the game.

Concerns over tin whiskers have intensified in recent years. Various research and studies have delivered burgeoning reports and have appeared in industry publications. The tin whisker issue, and its potential mishaps, has been recognized for more than six decades in electronic, electrical, and industrial applications. So, what is new?

This series will address the practical and pragmatic aspects of the tin whisker phenomenon with a light touch on scientific background. Before I delve into the gist of tin whiskers, several areas should first be clarified.



Metal Whiskers

Metal whiskers formed from the surface of metals are not limited to tin whiskers. In addition to tin, metals that have exhibited whiskers include: Zinc, cadmium, silver, gold, aluminum, copper, and lead. Whisker formation and its resulting shape and size depend on the time, temperature, substrate, surface condition of the substrate, surface morphology, plating chemistry, and plating process. The rate of whisker growth also depends on a list of factors including those mentioned above.

Whiskering is an intricate and complex process, calling for atomic-level considerations. A plausible metallurgical mechanism of tin whisker formation is yet to be detailed and I will address this in a future column.

Whiskers Versus Dendrites

Whiskers share commonality with dendrites in two ways: 1) Both are the result of a physical metallurgical process, thus following the principles of physical metallurgy; and 2) both can cause product failure.

But a metal whisker is not metallic dendrite. Dendrites, fern-like in appearance, grow across the surface of the metal. Metal whiskers, filament- or mound-like in shape, often grow by

protruding from the surface at a right angle. Whisker growth does not require moisture. In contrast, dendrite growth requires moisture that is capable of dissolving the metal into a solution of metal ions. The metal ions are then redistributed by electromigration in the presence of an electromagnetic field. Tin whisker formation does not require either dissolution of the metal or the presence of an electromagnetic field.

Tin Whisker Versus Tin Pest

Pure tin, a silver-white, lustrous, malleable metal at room temperature, has two allotropic forms—beta phase and alpha phase. An allotropic transformation is found to occur at approximately 13°C and significantly accelerated at approximately -30°C. At the transformation temperature, tin changes from its metallic crystalline form (white tin) to a non-metallic powdery form (grey tin). This transformation from beta-phase with crystal structure of bcc to alpha-phase of diamond cubic crystal leads to a large-volume expansion, resulting in brittle structure and frailty. This process is known as tin pest. Tin pest creates another concern for the use of pure tin in end-use applications.

Tin whiskers and tin pests are separate metallurgical phenomena. However, tin whiskers can be accelerated by autocatalytic "tin pest" expansion under extreme environments, aggravating the probability of product failure.

Practical Criterion

Metals can whisker when the right conditions are met so the evaluation of tin whisker propensity and growth rate should be put in the context of relative formation rate under a select set of conditions. For electronic and electrical applications, the renewed concern about tin whiskers is largely the result of the conversion from tin-lead coatings to lead-free (or tin coatings) for component leads and PCB surface finishes.

Thus, the relative performance in reference to a tin-lead benchmark which has demonstrated satisfactory whisker-resistance should be the criterion, not the absolute performance.

Whisker-Resistant, Not Whisker-Proof

It is reported that 90Sn10Pb coating has grown whiskers under elevated temperature aging. It should be noted that there is not an absolute alloy remedy since 90Sn10Pb coating was found to produce whiskers as well. Overall, for testing or evaluation on the whisker propensity of an alloy, key questions to address are:

- Is the system whisker-prone or whisker-resistant (not whisker-proof)?
- What is the system's whisker resistance when compared to the intended benchmark?

> ***"For electronic and electrical applications, the renewed concern about tin whiskers is largely the result of the conversion from tin-lead coatings to lead-free (or tin coatings) for component leads and PCB surface finishes."***

Lead-Free Solder Versus Tin Whiskers

An SAC alloy (SnAgCu alloy) is lead-free, but a lead-free alloy is not necessarily an SAC. This designation is particularly important as more viable lead-free alloys become commercially available. A number of SAC alloy compositions are commercially available and the number of the compositions is looming. A specific composition of an SAC should be noted; e.g., SAC105 has different mechanical behavior and physical phenomena from SAC305.

In whisker phenomenon, the physical metallurgy engaged in the process is complex and intricate—a compositional shift and/or an addition of extraneous elements to a base alloy system can dramatically change its whisker propensity.

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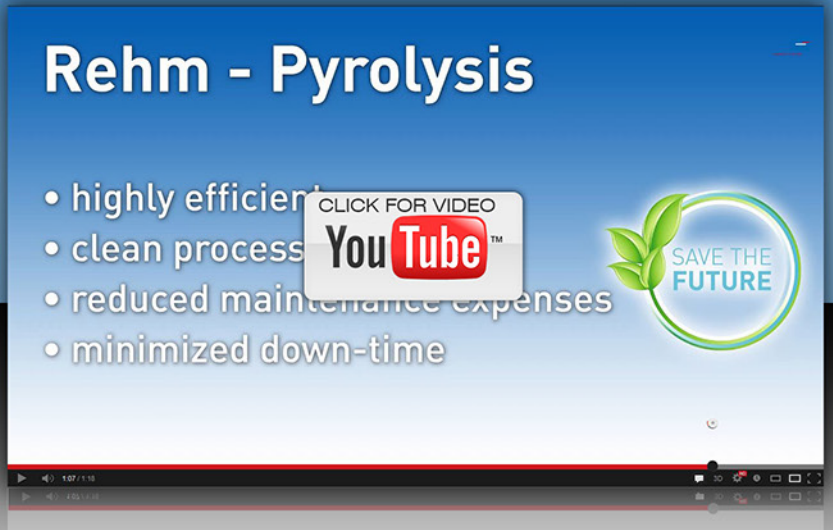

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TIN WHISKERS: CLARITY FIRST *continues*

The bottom line is that an alloy, SAC or otherwise, does not represent the material world of lead-free unless a sufficient testing scheme comprising representative materials is designed and the representative tests are conducted to validate the representation. Lead-free solder comprises a wide array of alloy systems, not to mention that each alloy system can be modified in numerous ways. A test scheme to represent lead-free is a daunting task with an astounding price tag. Tin whisker propensity studies should be conducted with a specific alloy composition, as clarity is the name of the game. **SMT**

Dr. Hwang will present two lectures related to electronics manufacturing at the International Conference of Solder Reliability, May 14, 2013, in Toronto, Canada.

Dr. Hwang, a pioneer and longstanding contributor to SMT manufacturing since its inception as well as to the lead-free development, has helped improve production yield and solved challenging reliability issues. Among her many awards and honors, she has been inducted into the WIT International Hall of Fame, elected to the National Academy of Engineering and named an R&D Stars to Watch. Having held senior executive positions with Lockheed Martin Corporation, Sherwin Williams Co., SCM Corporation and IEM Corporation, she is currently CEO of H-Technologies Group providing business, technology and manufacturing solutions. She is a member of the U.S. Commerce Department's Export Council, and serves on the board of Fortune 500 NYSE companies and civic and university boards. She is the author of 350+ publications and several textbooks and an international speaker and author on trade, business, education and social issues. Her formal education includes four academic degrees, as well as the Harvard Business School Executive Program and Columbia University Corporate Governance Program. Contact her at (216) 577-3284; e-mail JennieHwang@aol.com.

Novel Technique Could Lead to Better Capacitors

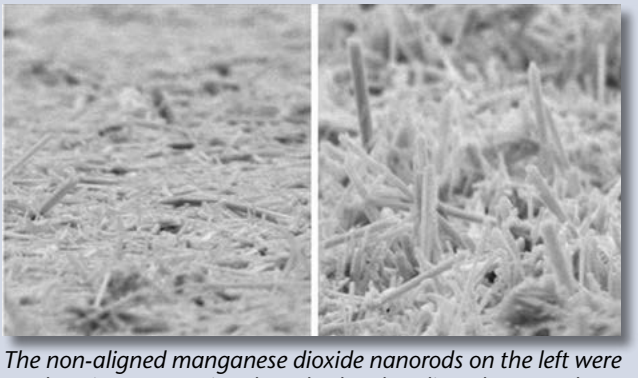
A new process for growing forests of manganese dioxide nanorods may lead to the next generation of high-performance capacitors.

As an energy-storage material for batteries and capacitors, manganese dioxide is cheap, environmentally friendly, and abundant. However, chemical capacitors made with manganese dioxide have lacked the power of the typical carbon-based physical capacitor.

Michigan Technological University scientist Dennis Desheng Meng theorized that the situation could be improved if the manganese dioxide were made into nanorods, which are like nanotubes, only solid instead of hollow. Until recently, researchers have been able to grow nanorods that either have the best crystalline structure or were aligned, but not both.

Now, Meng's research group has developed a technique to grow manganese dioxide nanorods that are not only straight and tall (at least by nano-standards), but also have the optimal crystal structure, known as α-MnO_2.

The nanorods display minimal internal resistance, allowing the capacitor to charge and discharge repeatedly without wearing out.



The non-aligned manganese dioxide nanorods on the left were made using conventional methods. The aligned nanorods on the right were grown in Dennis Desheng Meng's lab using electrophoretic deposition. Photos by Sunand Santhanagopalan.

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- Workmanship PCB with components for practical exam

Course Objective:
Upon successfully completing this learning activity, attendee will have received:

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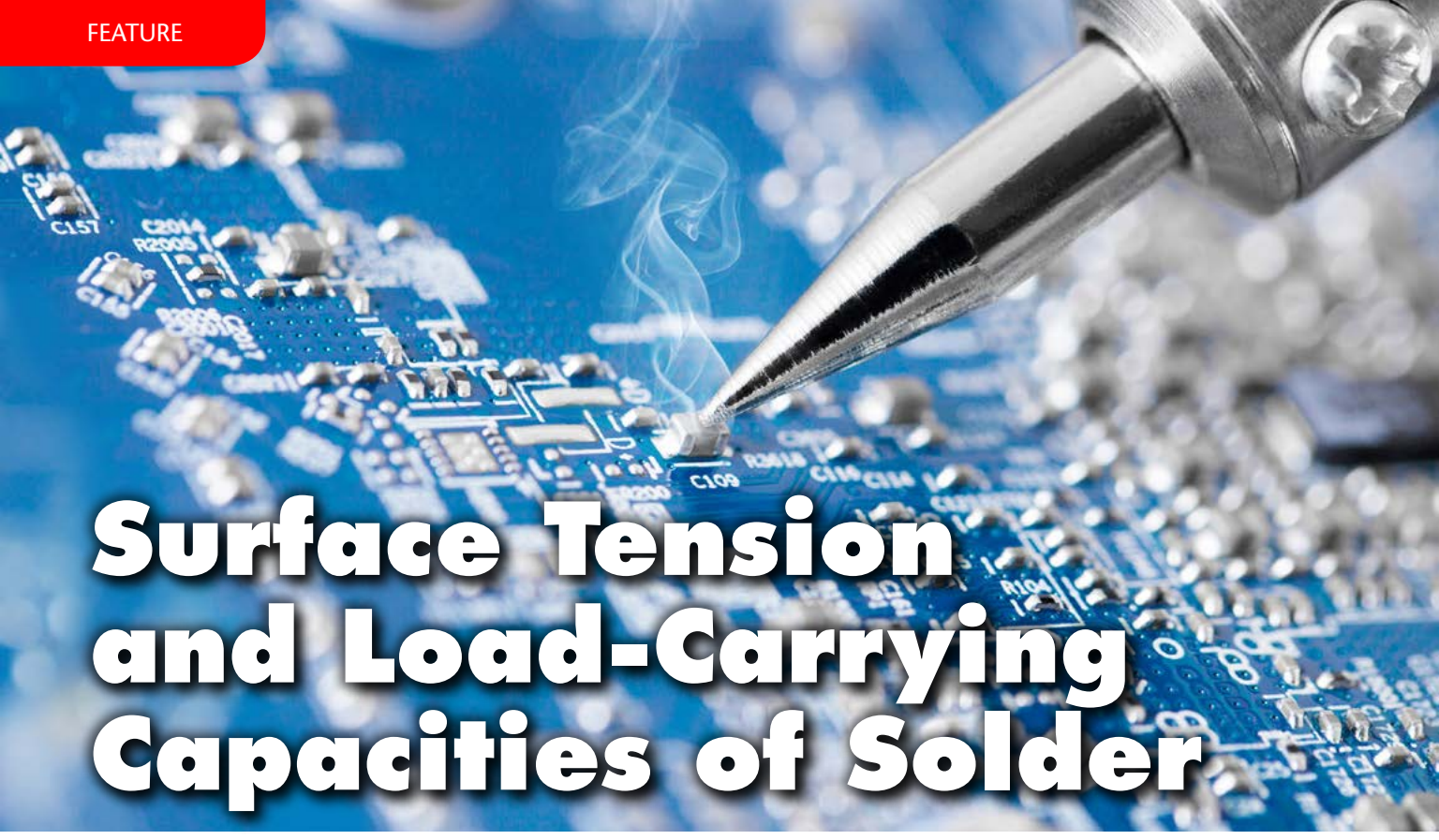

Surface Tension and Load-Carrying Capacities of Solder

by Dr. Hans Bell, REHM THERMAL SYSTEMS,
in cooperation with **Thomas Kolossa and Peter Fischer, Balver Zinn**

SUMMARY: Manufacturers rely heavily on the load-carrying capacity of molten solder millions of times a day. An in-depth knowledge of surface tension values makes it possible to confirm which components are compatible with an upside-down soldering process. This article reveals the processes, and results, used to determine the surface tension values of various solders.

Introduction

Reflow soldering on both sides of a board is standard procedure in the SMT manufacturing process. When the second component side is soldered, the components hang upside-down on the PCB. When the reflow process reaches its peak range, the possibility of remelting previously finished solder joints cannot be ruled out, which leaves the component hanging directly from the molten solder.

Manufacturers count on the load-carrying capacity of molten solder millions of times a day. Figure 1 shows a component hanging from a drop of solder. Molten solder is entirely capable of bearing considerable component weight.

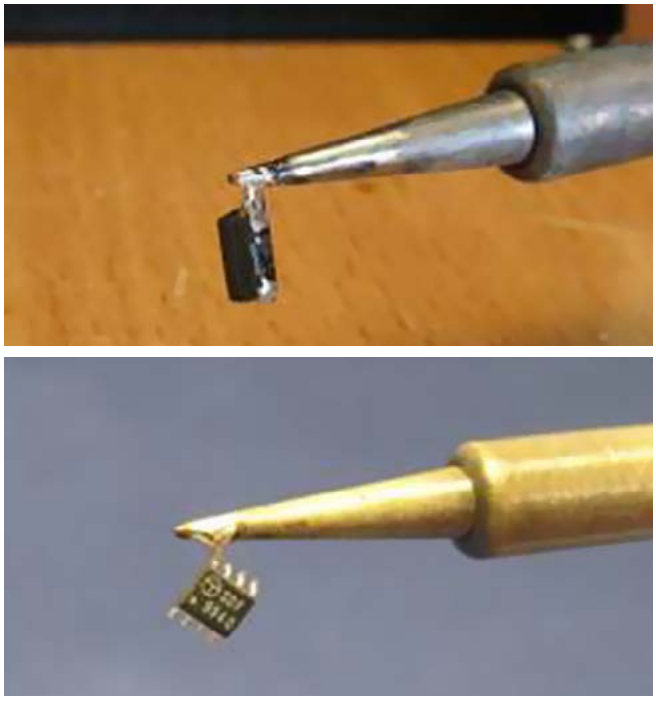

Figure 1: Demonstration of the load-carrying capacity of molten solder.

The surface tension (s) of the molten solder is decisive with regard to the load-carrying capacity in the event of a second reflow process. Knowledge of surface tension values makes it

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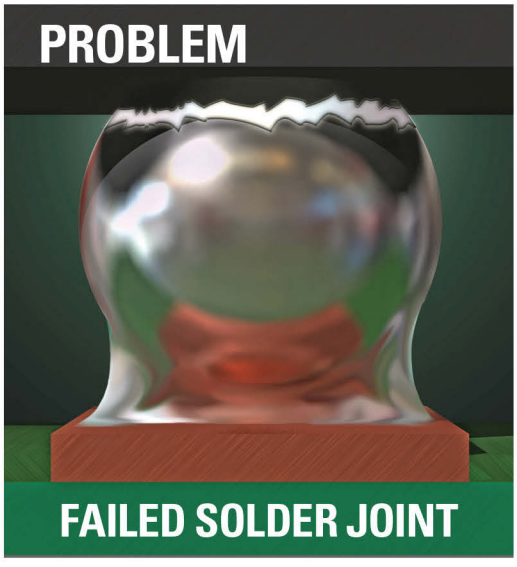

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possible to successfully determine which components are compatible with an upside-down soldering process. Surface tension is defined as the force (F) required to stretch the surface divided by the length of border line (L).

Load-carrying capacity C_{LC} of molten solder can thus be calculated as follows:

$$C_{LC} = \sigma \cdot L$$

The circumference wetted by the molten solder is defined by border line (L). For a chip capacitor or a resistor, this is the circumference of both front surfaces and lands; for a multipole component L is, for example, the sum of all circumferences of the gull wing solder joints of an SO component.

Surface Tension of Molten Solders

In collaboration with Balver Zinn, the surface tension values of various solders were determined (Table 1).

Sn60Pb40 is a solder for lead-containing applications. Solder bath temperatures of 245 to 255°C (depending on PCB layout) are recommended for wave soldering. Depending on technical requirements (e.g., selective soldering), soldering temperatures may lie within a range of 245 to 300°C.

The Sn99Cu1 alloy can be used for wave soldering and hot-dip tinning wherever noticeable copper leaching does not affect the reliability and usability of the solder joint. Special attention must be paid to solder bath management. Depending on copper drag-in into the solder bath, it may be necessary to recharge with Sn99.9 (pure tin) instead of the solder alloy, to limit copper content.

SN96C solder (SnAg3.8Cu0.7) is a standard, lead-free eutectic solder commonly used in Europe, with whose processing many years of experience has been gained in the field of lead-free electronics production. SnAg3.8Cu0.7 can be used for wave soldering, selective soldering, and hot-dip tinning. It has the lowest melting point of all lead-free tin-copper and tin-silver alloys.

However, no special demands can be placed upon copper leaching when this alloy is used, which can be seen in the comparison shown in Figures 2 and 3. Copper leaching tests were executed with a selective soldering system at a solder temperature of 360°C in a nitrogen atmosphere. Loss of mass was determined for a copper wire with a diameter of 6 mm during dwell time in the selective soldering system's dynamic solder bath.

As a specialist for micro-alloyed solders, Balver Zinn presents the optimized i-SAC305 alloy based on SnAg3.0Cu0.5. The solidifying characteristics of SnAg3.0Cu0.5 have been improved by adding cobalt (Co). Cobalt (Co) results in a finer and more homogenous microstructure (Figure 4). The homogenous microstructure leads to a smooth, glossy solder joint. Furthermore, the solder is doped with germanium to reduce dross formation and to improve the flow characteristics of silver-containing solders.

Alloys (e.g., SAC0703) are doped with nickel (Ni) and germanium (Ge) to compensate for

Solder Wire/Alloy	Diameter [mm]	Melting Point or Melting Range	Flux Content [%]
S-Sn60Pb40	1.0	183-190° C	With flux
S-Sn60Pb38Ag2	0.3	176-189° C	2.5
Sn60Pb38Cu2	1.0	183-190° C	2.2
SN100C SnCu0.7Ni	1.0	227° C	2.2
SN96C-SnAg3.8Cu0.7	1.0	217° C	2.2
Sn99Cu1; FC 2.2%	0.7	227° C	2.2
SCAN-Ge 0703; FG 3,5%	1.0	217-228° C	3.5
i-SAC305-SnAg3.0Cu0.5Co	1.2	217-219° C	2.2

Table 1: Examination of the utilized solders.

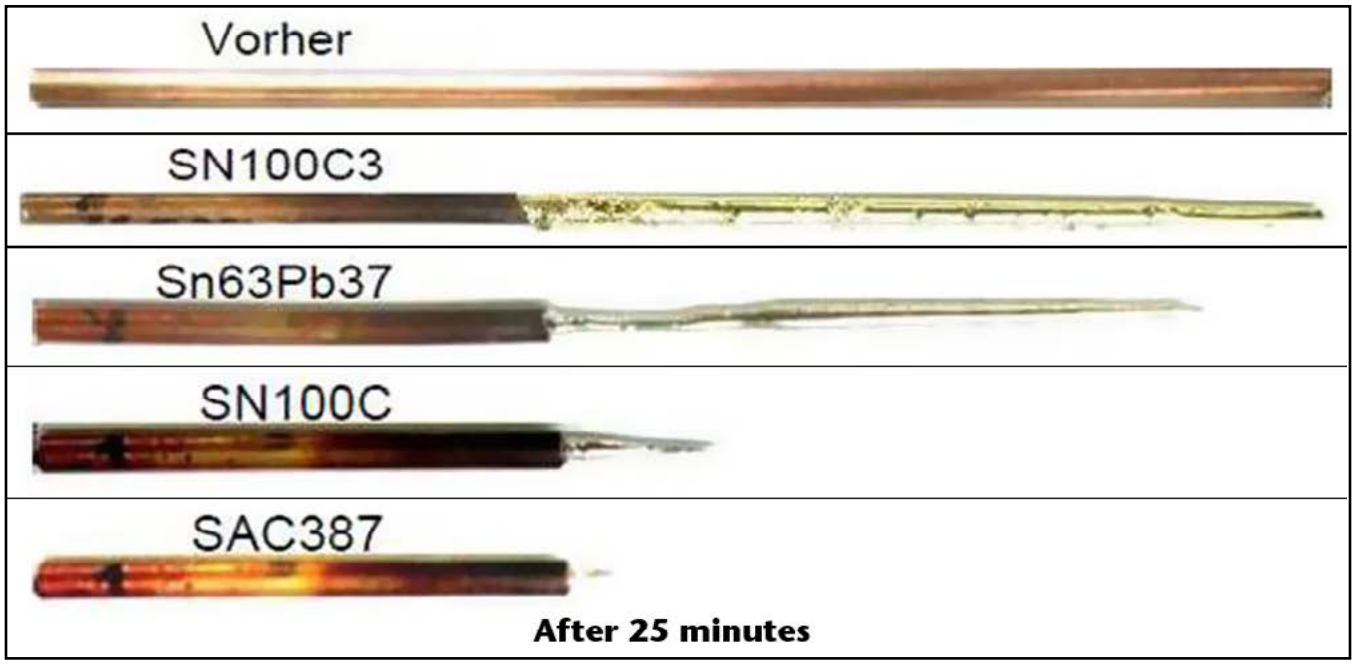

Figure 2: Copper wire ø 6 mm, miniwave 360°C, immersion time 40 min/25 min. (Source: Balver Zinn 2012)

the less than ideal flow characteristics of silver-containing solders. These solders, which are doped with nickel and germanium, belong to the patented SCAN-Ge product range with varying copper and silver content. Micrographs for Sn3.5Ag0.5Cu with and without Ni doping are shown in Figure 5. Shrinkage voids are significantly decreased after Ni doping, thus reducing surface roughness and increasing glossiness.

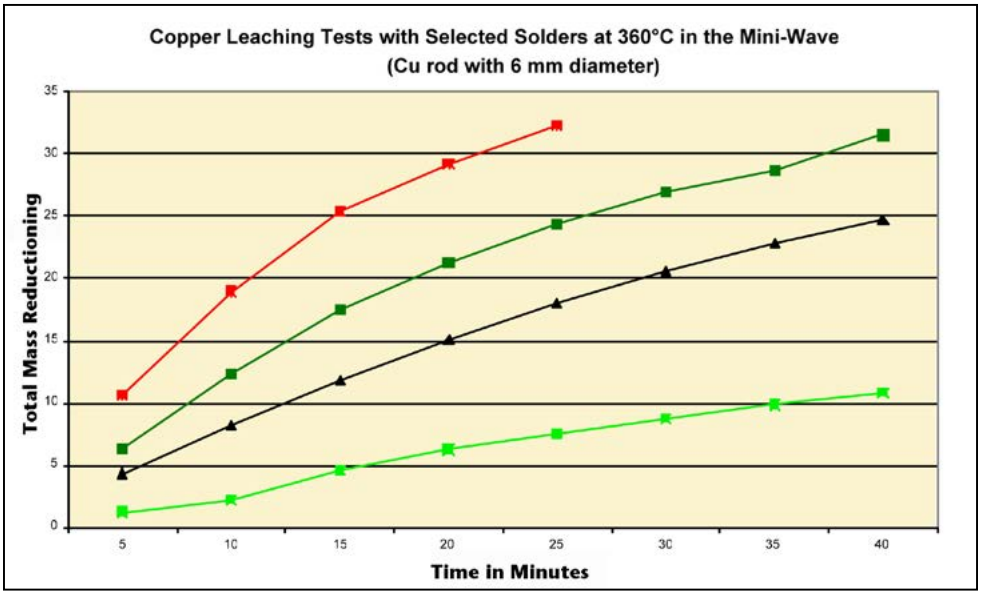

Figure 3: Copper alloy with use of different solders. (Source: Balver Zinn 2012)

Germanium is an antioxidant agent which reduces dross formation (oxide formation). Combined doping of the solder with Ni and Ge allows for improved tear-off performance of the solder when the PCB is removed from the solder wave. This results in significantly reduced bridging.

The SN100C alloy is a nickel-stabilized (Ni), eutectic tin-copper solder (SnCu0.7Ni), which is additionally doped with germanium to permanently reduce oxidation of the solder. Depending on the soldering process and the process conditions, the antioxidizing effect of germa-

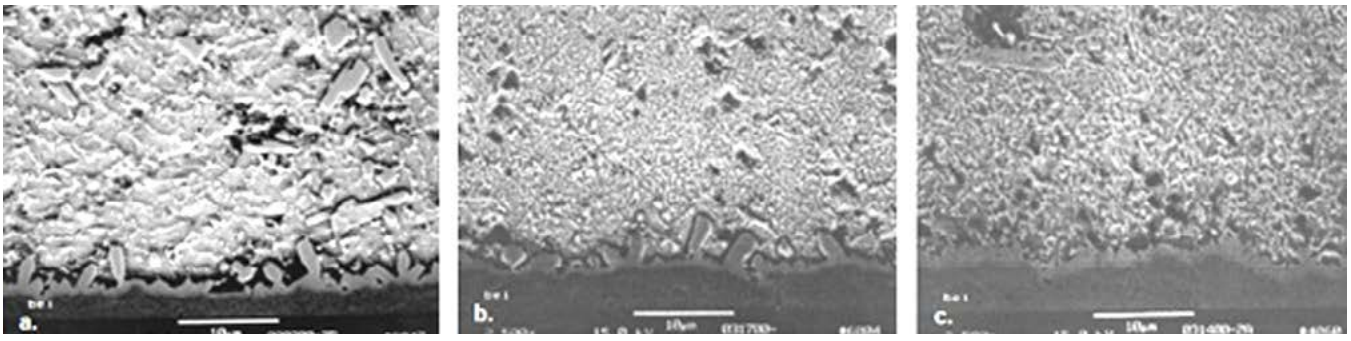

Figure 4: Characteristics of the structure and the intermetallic phase—4a (left), Sn3,6Ag1,0Cu; 4b (center), Sn3,6Ag1,0Cu0,15Co; and 4c (right), Sn3,6Ag1,0Cu0,45Co. (Source: I. E. Anderson et al, "Alloying Effects in Near-Eutectic Sn-Ag-Cu Solder Alloys for Improved Microstructural Stability")

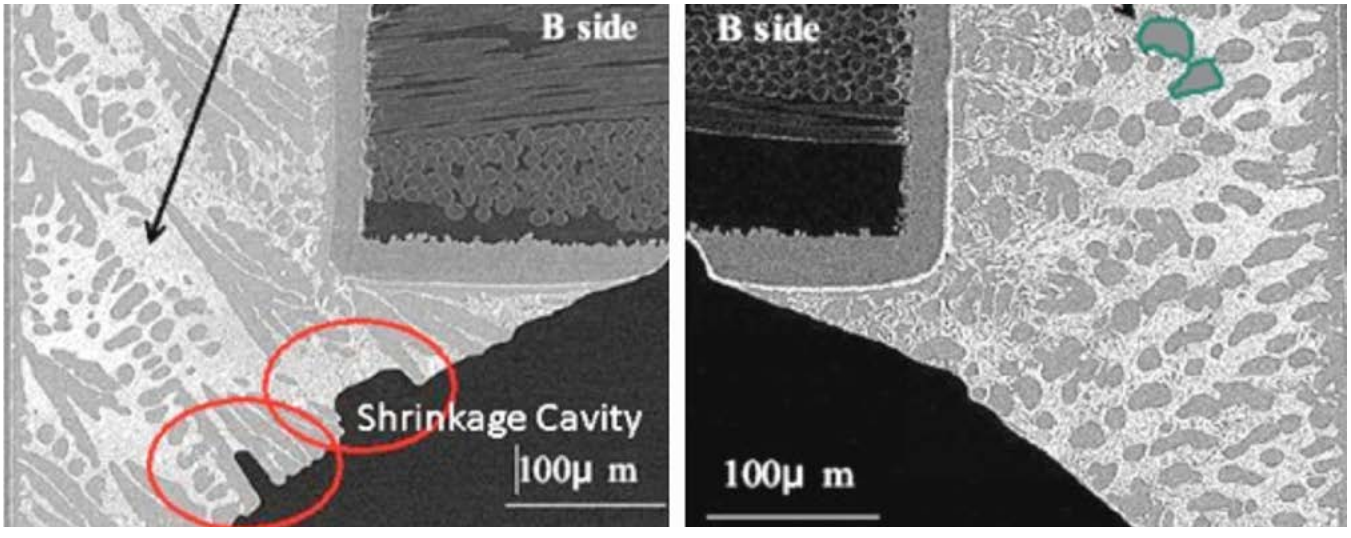

Figure 5: Micrographs of THD solder joints—5a (left), Sn3,5Ag0,5Cu, and 5b (right), Sn3,5Ag0,5CuNiGe. (Source: N. Hidaka et al, Nihon Superior and Balver Zinn, 2006)

nium may be diminished as of a Ge content of less than 0.002%. The Ge content of solder baths can be adjusted through the use of DESOXY RSN (SnGe1).

The use of SN100C results in solder joints with gloss characteristics similar to those obtained with lead-containing solders. Compared with conventional SnCu and SnAgCu solders (Figures 6 and 7), SN100C causes substantially less copper leaching, minimizing the risk of unacceptable reduction in electric and thermal conductivity. And, thus, reduced copper leaching allows for more constant process management and helps to reduce material consumption. Reduced tendency toward bridging must be especially stressed for SN100C.

According to an independent ELFNET study, SN100C is the most widely used wave solder in Europe. In particular, this alloy is preferred for the higher process temperatures associated with selective soldering.

Figure 3 elucidates the fact that at higher process temperatures, the use of SN100C with increased copper content (SN100C3, Cu content: 3% by weight) is advisable to minimize copper leaching.

In 2005, Balver Zinn lot SN100C was deemed the most reliable soft solder for wave soldering on the basis of tests conducted by NASA.

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SURFACE TENSION AND LOAD-CARRYING CAPACITIES OF SOLDER *continues*

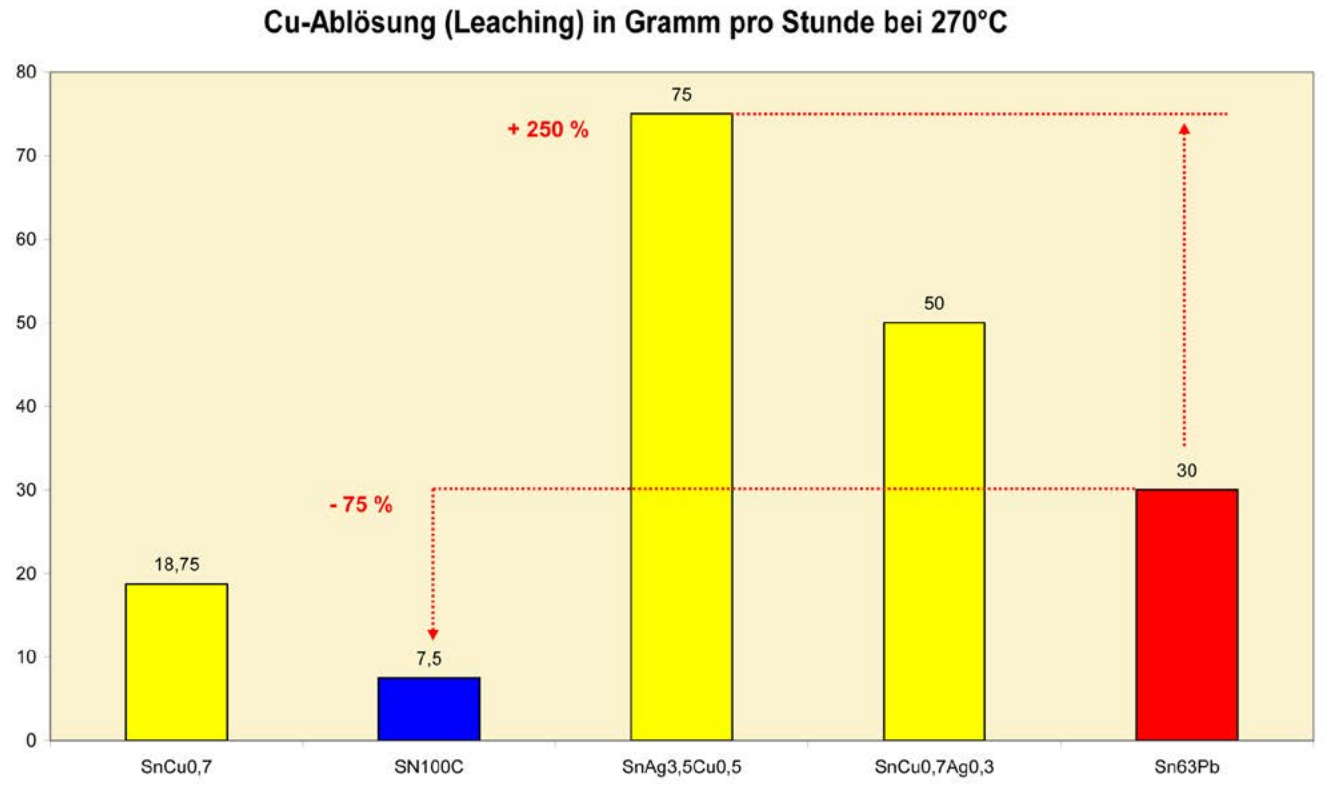

Figure 6: Copper alloy with usage of different solders. Selective soldering system solder bath temperature 270°C. (Source: Balver Zinn)

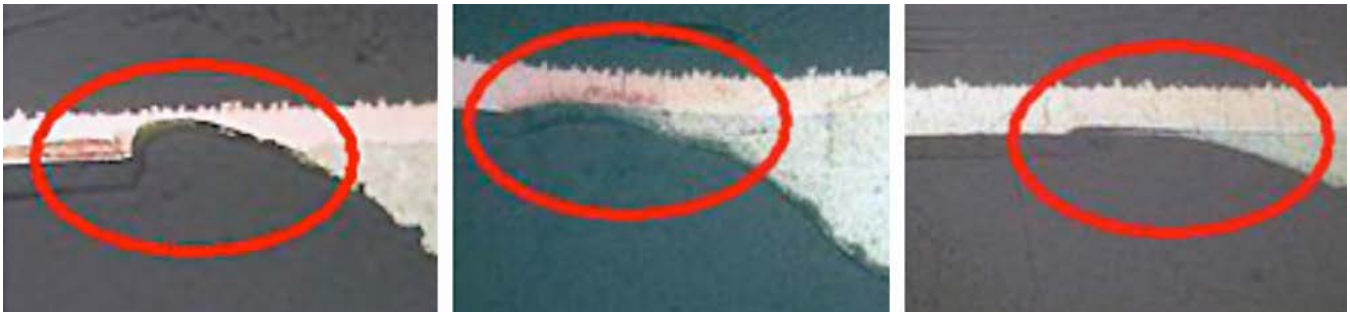

Figure 7: Copper alloy with usage of different solder alloys—7a (left), SnAg3,8Cu0,7; 7b (center), SnAg3,5Cu0,5; and 7c (left) Sn100C. (Source: Keith Sweatman, Nihon Superior und Balver Zinn 2012)

Experimental Setup to Determine Surface Tension of Molten Solders

A relatively simple test setup was used to determine surface tension, which consisted essentially of a temperature-controlled, handheld soldering iron with temperature measurements conducted at its tip by means of a thermocouple and a thermal imaging camera. Figure 8 shows this test setup with the additional externally attached thermocouple. The thermal imaging camera made it possible to assess heat distribution within the molten solder at the tip of the soldering iron and the test object hanging from it (Figure 9).

Various types of components and lengths of copper wire were used as test object.

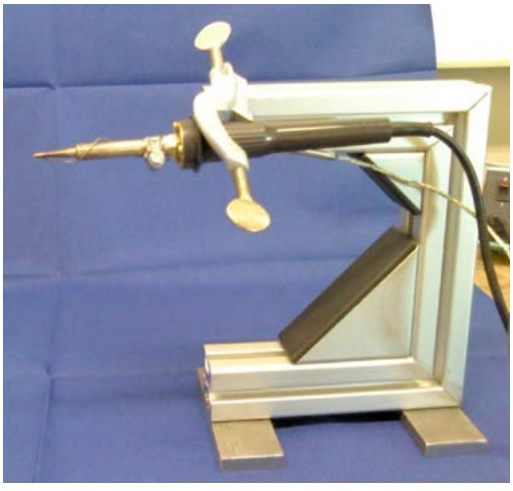

Figure 8: Test setup for determining surface tension.

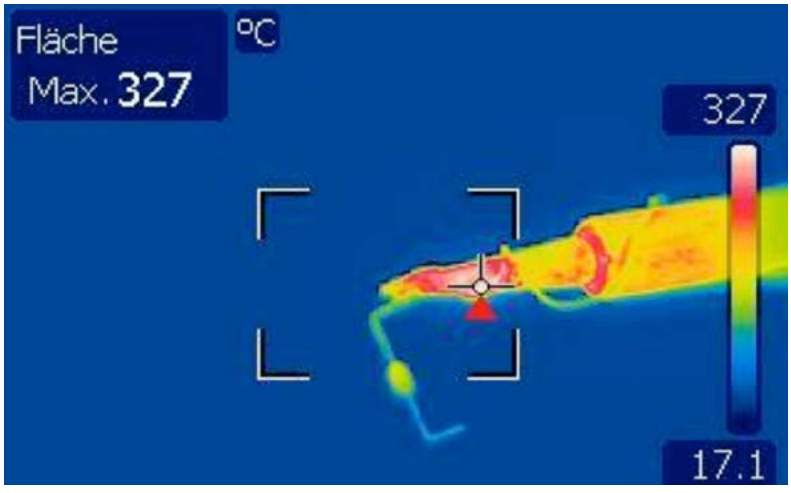

Figure 9: Thermal image obtained during a measurement.

Results

While the measurements were being performed, it quickly became apparent that actual components are not suitable for ascertaining meaningful surface tension values. This is due to greatly differing wetting characteristics which result in a widely varying border line (L). Table 2 shows the results obtained with i-SAC305-SnAg3.0Cu0.5Co solder for an average solder temperature of 308°C.

These values are considerably lower than those found in the literature. Tauchmann [Jens Tauchmann Messer Group, April 21, 2005, SMT Trade Fair, Nuremberg, Germany] indicates a value of 490 mN/m for lead-free SnAg3.8Cu0.7 solder in an air atmosphere. Components are not suitable for determining surface tension, but values obtained with them can be compared with laboratory values to arrive at safety factors for soldering upside-down. A comparison of the mean value shown in Table 2 with values specified in the literature would indicate that a safety factor of greater than 2 is entirely reasonable for actual production conditions. We will return to this aspect at the end of this article.

Measurements conducted on lengths of copper with specified diameters (1.35 and 1.75 mm) were much more successful. Surface tension was determined at various solder temperatures—the soldering station was set to the following temperatures: 320, 330, 340 and 350°C. Temperatures measured at the tip of the soldering iron were used for evaluation. Table 3 lists several of the results obtained with a solder temperature of 320 to 330°C.

Component	Surface Tension [mN/m]
	Mean Value
	189
	Individual Values
SMD supercap	253
SMD supercap	261
SMD supercap	153
SOT232-3	223
SOT232-3	169
SMD diode	148
SMD diode	174
Micro-fuse	163
SMD pushbutton	150
SMD ceramic capacitor	200

Table 2: Values for actual components; solder type i-SAC305-SnAg3.0Cu0.5Co.

On the basis of other measurements as well, the fact is confirmed that SnPb solders (in this case Sn60Pb40) have less surface tension than lead-free SAC305 (in this case i-SAC305-

SURFACE TENSION AND LOAD-CARRYING CAPACITIES OF SOLDER *continues*

Solder Wire/Alloy	Solder Temperature [°C]	Surface Tension [mN/m]
S-Sn60Pb40	326	323
S-Sn60Pb38Ag2	327	330
Sn60Pb38Cu2	326	342
SN100C SnCu0.7Ni	321	313
Sn99Cu1; FC 2.2%	325	325
SN96C-SnAg3.8Cu0.7	323	315
SCA 0703; FC 3.5%	325	311
i-SAC305-SnAg3.0Cu0.5Co	324	336

Table 3: Surface tension of various solders.

SnAg3.0Cu0.5Co), thus frequently resulting in better wetting characteristics for tin-lead solder. As temperature rises, the solder's surface tension drops as a rule. Figure 10 shows the mean values of our measurement results for SAC solders, as well as the calculated trend lines (linear regressions).

The reason that surface tension drops as temperature rises can be found in the physics of liquids. Work must be executed to cause a molecule to move from the inner regions of a liquid to its surface. At higher temperatures, the mobility of the liquid's molecules increases, and thus less work is required to enlarge the surface.

However, in the case of soldering, we're dealing with chemical and metallurgical processes which stand in opposition to this general trend. During soldering, the solder interacts with its bonding partners; in our case the copper in the

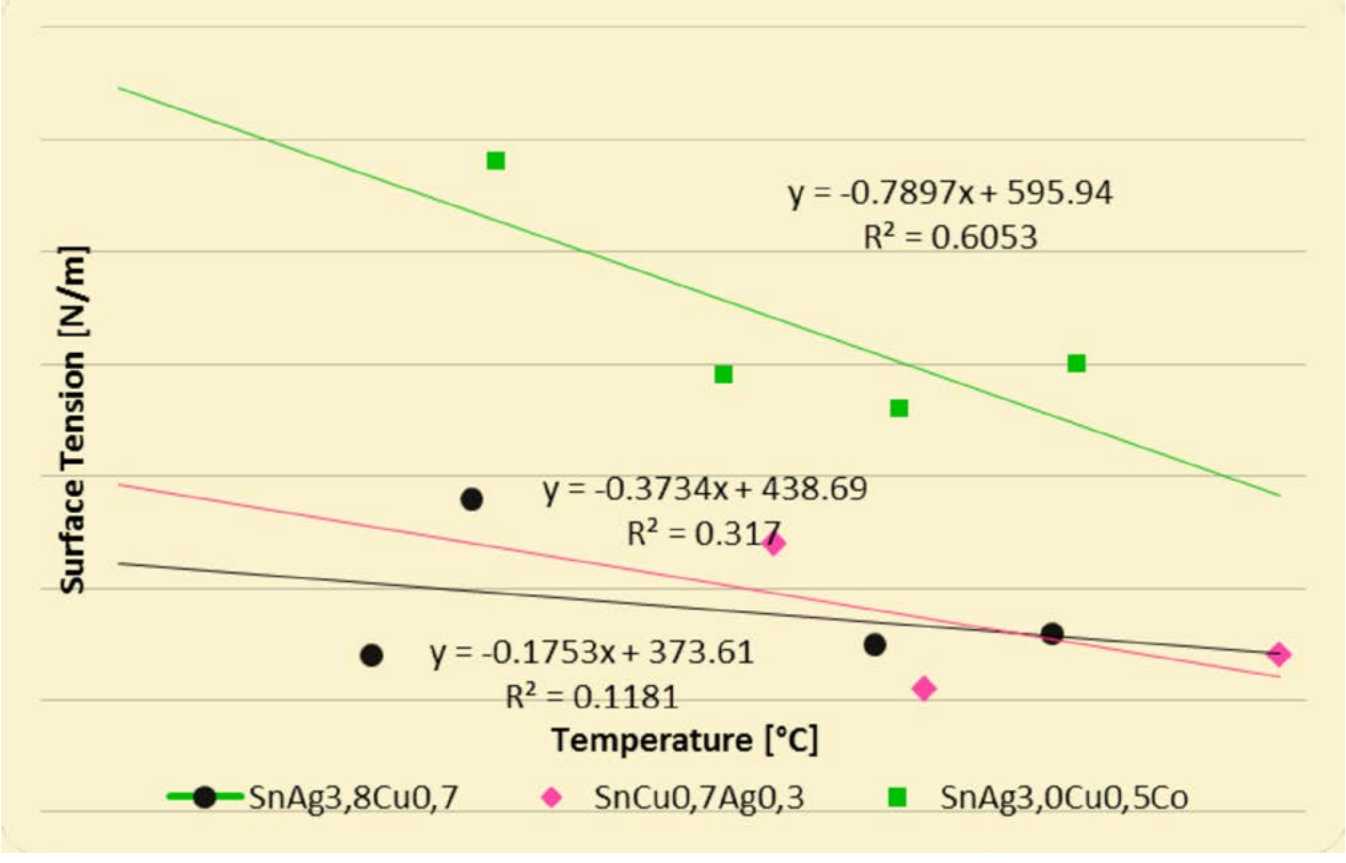

Figure 10: Surface tension of SAC solders.

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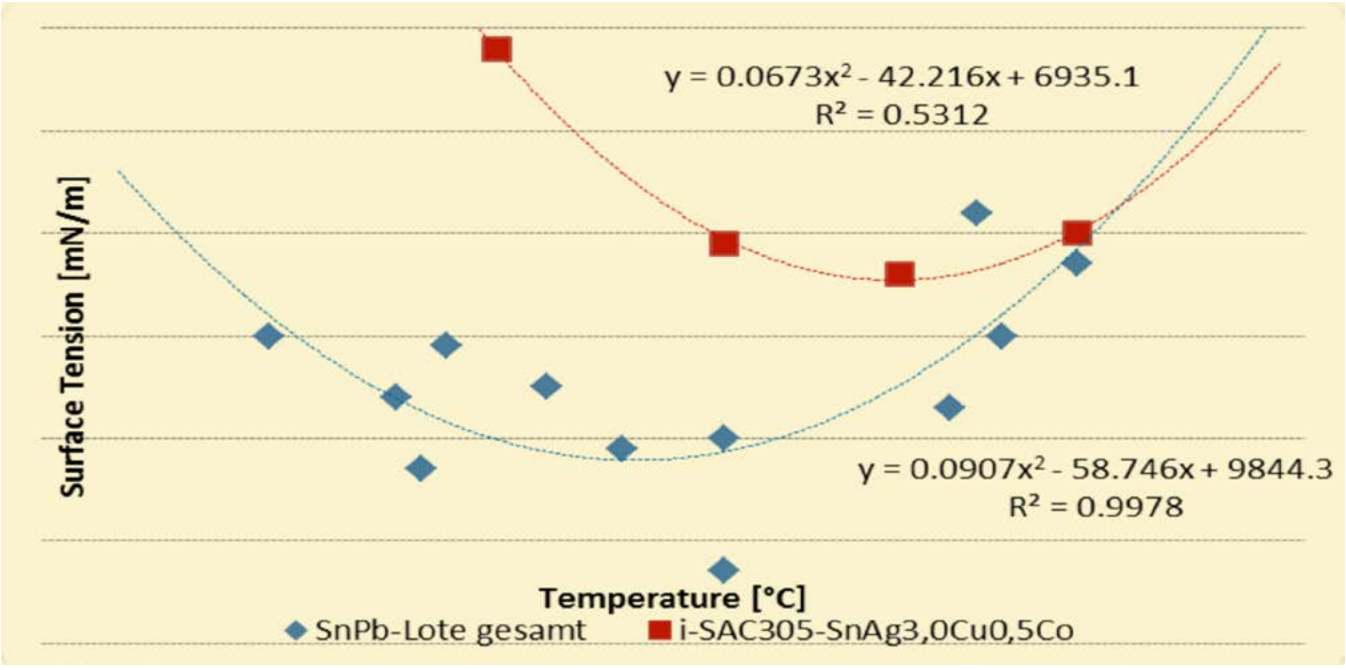

Figure 11: Surface tension trend lines: Quadratic regression.

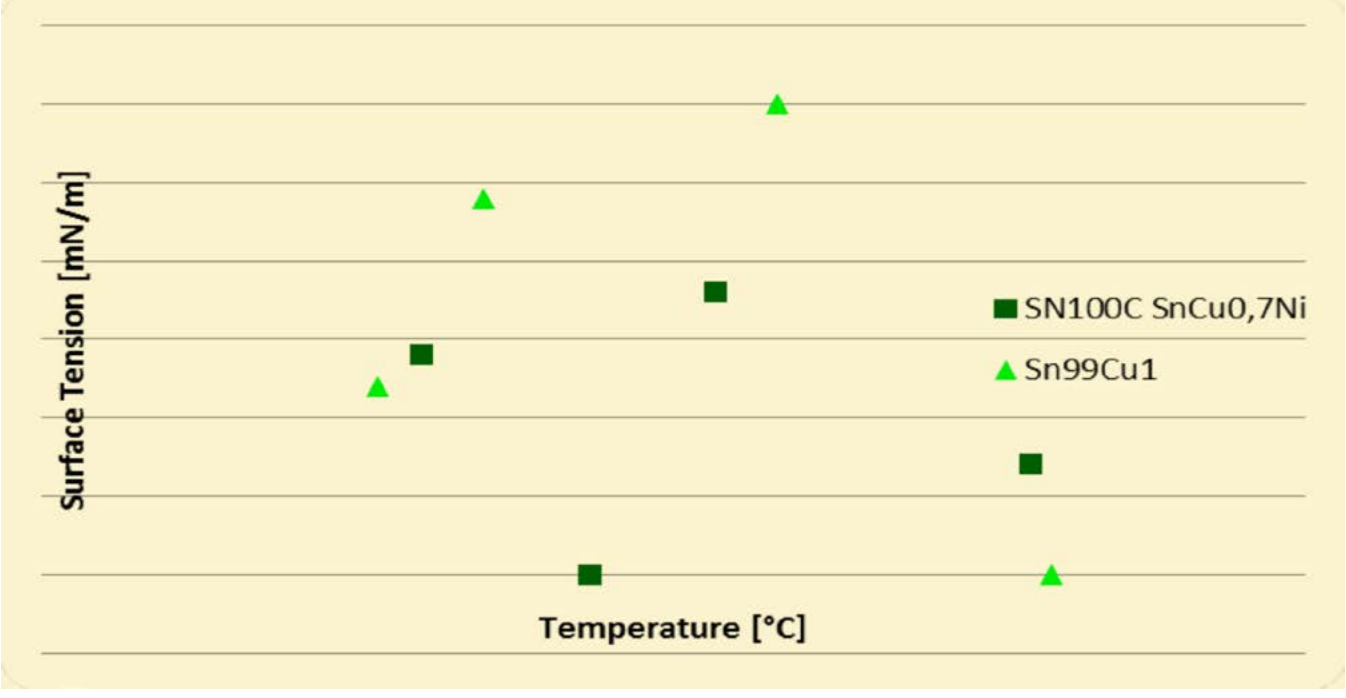

Figure 12: Surface tension for tin-copper solders.

lengths of copper wire used as test objects. The consequence is dissolution of copper into the solder and the formation of an intermetallic phase—the original composition of the solder is thus changed during the soldering process.

Our measurement results also demonstrate this effect (Figure 11). At first, the surface tension of all examined SnPb solders and the i-

SAC305 solder comply with the general trend of decreasing values. But this trend is reversed at a temperature of between 320 and 330°C, and surface tension increases again.

If solders with reduced leaching characteristics are used (in our examinations the following tin-copper solders: SN100C SnCu0.7Ni and Sn99Cu1), the trend is not reversed within the examined range of temperatures (Figure 12).

Load-Carrying Capacities of Molten Solder

The load-carrying capacity of the molten solder must always be greater than weight force ($F_{W)}$ of the respective component. The weight force of the component can be determined with a scale. For example:

The diode shown in Figure 1 (left) weighs approximately 0.18 g and the solder has wetted a circumference of approximately 5 mm. If the surface tension of i-SAC305 (Table 3) is plugged into this sample calculation, we arrive at a load-carrying capacity of C_{LC} = 336 0.004 = 1.7 mN. Effective weight force ($F_{W)}$ of the diode amounts to roughly 0.17 g 9.81 m/s² = 1.7 mN. Figure 1 also shows how the solder already begins to become elongated—in this case its load-carrying capacity is nearly exploited.

To assure reliable manufacturing, load-carrying capacity ($C_{LC)}$ should be at least twice, and preferably four times as great as, the weight force ($F_{W)}$ of the upside-down component. This safety factor is necessary because additional influences may minimize load-carrying capacity in the actual soldering process. The fact that wetting deficiencies can reduce maximum achievable border line (L) has already been discussed above (Table 2), and leaching effects change the composition of the solder as well and, thus, its surface tension during the reflow soldering process. In addition to this, the actual manufacturing process is subject to vibration and acceleration which are transferred from the reflow system's conveyor to the PCB. The effective weight force of the component at any given moment is influenced by changing acceleration.

Due to the fact that in most cases only those surface tension values which are cited in the literature are available to the manufacturer, and since wetted border line (L) in not precisely known, a safety factor is advisable in any case when estimating load-carrying capacity.

For example, a safety factor of 4:

$$F_W \pounds 4\times C_{LC}$$

$$F_W \pounds 4\times s\times L$$

where L = n l

n: Number of connectors on the component
l: Length of a connection wetted by the solder
s: Surface tension of the solder
F_W: Weight force of the component
C_{LC}: Load-carrying capacity of the solder **SMT**

Dr. Hans Bell is head of the Development and Technology department at Rehm Thermal Systems. He began his career developing sensors at Applikationszentrum (application centre) Berlin. Dr. Bell worked for several years in the Werk für Fernsehelektronik and was responsible for the optimisation and development of manufacturing technologies for optoelectronic components. Until 1999 he was a manufacturing technologist in charge of production-oriented tasks in the development of solder bonding technologies at DeTeWe in Berlin. He received his doctorate at the Technical University of Munich.

Balver Zinn Josef Jost GmbH & Co. KG, located in Balve, Germany, is a leading manufacturer of solders, high-quality anodes, alloys, and wires for the electronic industry. Lead-free products are one of the company's core competencies. The family-owned and operated company became active in the metal and metalworking industry in the late 19th century. Today, third-generation family members, Josef and Gregor Jost manage the company which employs more than 100 globally, including global sales and distribution.

Minimizing Voiding in QFN Packages Using Solder Preforms

by Seth J. Homer and Ronald C. Lasky
INDIUM CORPORATION

Editor's Note: This paper was first published as part of SMTA International Proceedings.

SUMMARY: QFNs can be a challenge to assemble, especially when it comes to voiding, but the addition of a solder preform can reduce the problem by increasing the solder volume of the joint—all without adding flux volume.

Abstract

According to Prismark Partners, the use of quad-flat no-leads (QFNs) is growing faster than any package type except for flip-chip chip-scale packages (CSPs). Prismark projects that 32.6 billion QFNs will be assembled worldwide by 2013, which represents 15% of all integrated circuit (IC) packages.

However, QFNs can be a challenge to assemble, especially when it comes to voiding. In most QFN assembly processes, solder paste is used as a means of attachment. This approach can be problematic, as excessive voiding often occurs due to the lack of standoff on the component and the high flux content of the paste. The addition of a solder preform can reduce such voiding by increasing the solder volume of the joint without adding flux volume.

Adding preforms to an assembly process is very easy. Preforms are packaged in tape-and-reel for easy placement by standard pick-and-place machines, right next to your components. The focus of this paper will quantify the preform requirements and process adjustments needed to use preforms in a standard SMT process. In addition, experimental data showing void reduction using preforms will also be presented.

Introduction

Advances in flux formulations and particle size distribution have led to increased capabilities for solder paste; however, some challenges still exist, especially as related to specific components. One component in particular is quad-flat no-leads (QFNs).

QFNs are close to the size of a chip-scale package. In addition to having no leads, QFNs

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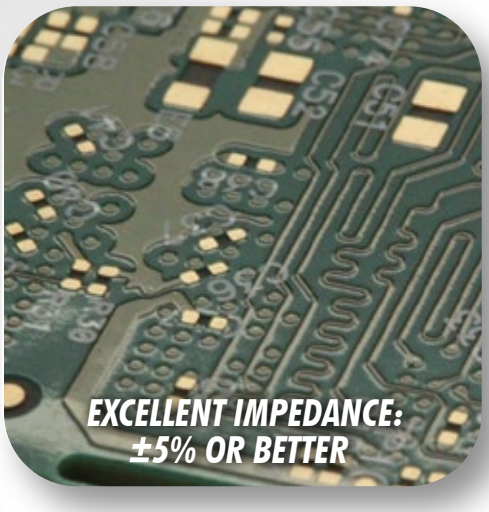

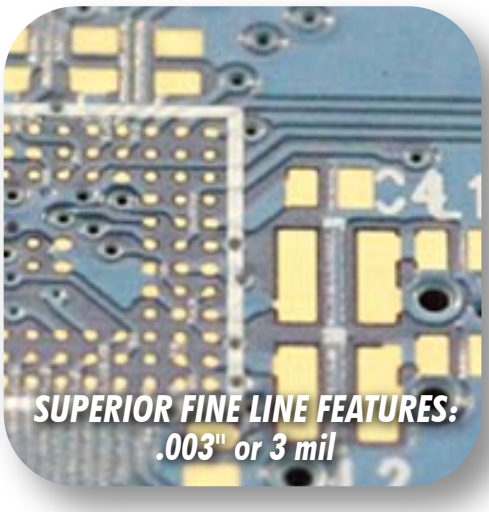

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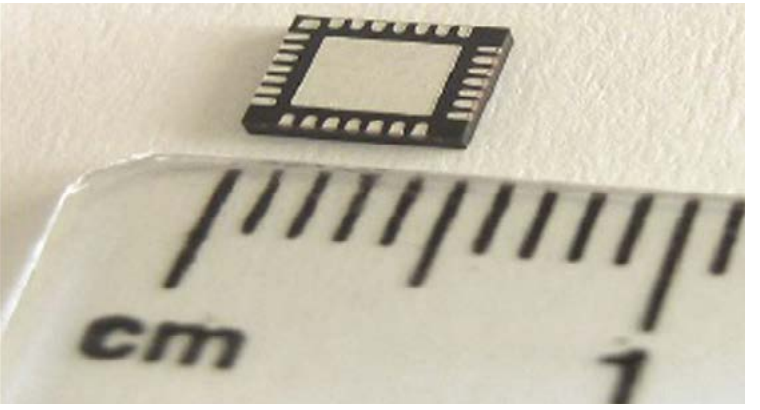

Figure 1: A QFN showing its leads and thermal pad.

have a thermal pad to conduct heat out of the integrated circuit (IC) in the QFN into the printed wire board (PWB). Figure 1 shows a QFN with its leads and thermal pad.

QFN packages are slated to have one of the highest growth rates in the next few years, predicted to be over 15% per year by Prismark Partners. This growth is understandable as QFNs are desirable for assembling miniaturized personal electronic devices such as mobile phones. With approximately 3 billion worldwide mobile phone subscriptions, a number approaching half of the world's population, mobile phones are rapidly becoming the defining electronic device of this era. So, miniaturized packages, such as QFNs, will continue to be in demand into the foreseeable future.

Unfortunately, when assembling QFNs, voids can form in the reflowed solder paste under the thermal pad. This paper will review steps to minimize this type of void formation by using solder preforms.

How Voids Form in QFNs

In the typical QFN assembly process, solder paste is printed on the PWB lead pads, as well as the PWB pad for the QFN thermal pad. The QFN component is then placed. The QFN design leaves little vertical space between the QFN thermal pad and the PWB pad. Therefore, during the reflow process, it is difficult for all of the flux volatiles to escape from the area of the QFN thermal pad.

This phenomenon is exacerbated by the fact that solder paste is approximately 50% flux by volume. As a result of these trapped volatiles, voiding is common (see Figure 2). In addition to this concern, some QFN designs are too large and demand more solder than printed paste can deliver to the solder joint. In these cases, the lack of solder is responsible for the voiding, which can result in poor thermal conductivity between the QFN pad and the PWB. This poor thermal conductivity can lead to the IC overheating and can then cause near-term IC failures, in addition to long-term IC reliability risk. Figure 3 shows a thermal image of such an overheating IC.

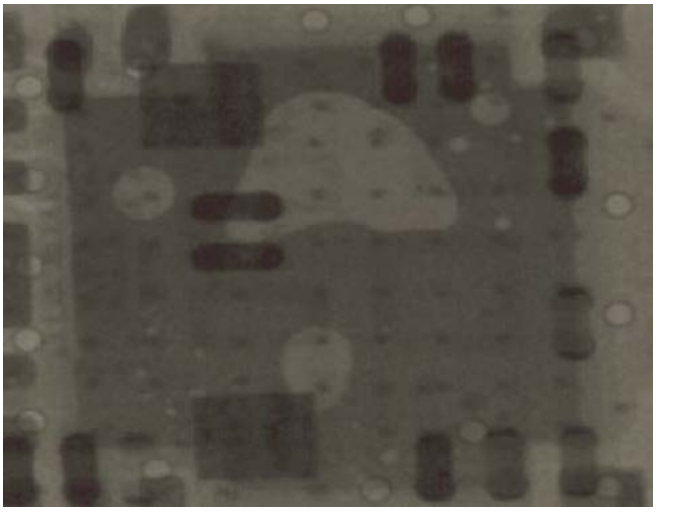

Figure 2: An X-ray image of the voiding between the QFN thermal pad and the PWB.

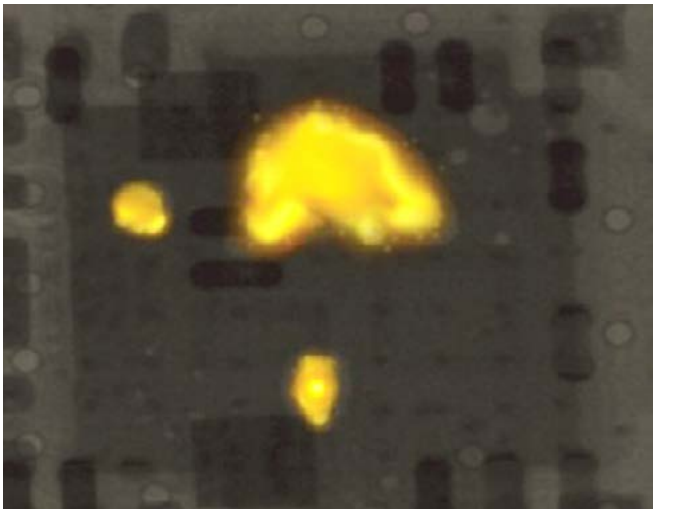

Figure 3: Illustration of the result of thermal path obstruction and localized heating.

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Application Note

AN1902
Rev. 4.0, 9/2008

QFN	PCB Land Pattern				Stencil Aperture			
	4 x 4		9 x 9			4 x 4		9 x 9
Version	E	S	E	S	E	S	E	S
Lead pad width (mm)	0.37	0.37	0.28	0.28	0.32	0.32	0.28	0.28
Lead pad length (mm)	0.92	0.92	0.69	0.69	0.75	0.75	0.69	0.69
Pitch (mm)	0.65	0.65	0.50	0.50	0.65	0.65	0.50	0.50
Thermal pad width (mm)	2.15	2.15	7.25	7.25	2.15	2.15	7.25	7.25
Thermal pad length (mm)	2.15	2.15	7.25	7.25	2.15	2.15	7.25	7.25
Aspect ratio	—	—	—	—	2.52	2.52	2.20	2.20
Area ratio	—	—	—	—	0.88	0.88	0.78	0.78

Table 1: An example of stencil calculation based on the Freescale QFN Application Note AN1902.

Acceptable voiding level criteria vary depending on the component and the application, but the most common QFN concern is with the largest void created on the thermal pad. A solder preform, in conjunction with the paste deposit, will assist in reducing the size of these large voids, as well as reducing overall quantity of voids.

QFN Voiding Solution Using Solder Preforms

Approaching a solution using a solder preform requires attention to the following areas:

- Stencil design;
- Preform geometry;
- Placement parameters;
- Preform flux coating; and
- Reflow profile.

Stencil Design

Stencil design parameters vary when using a solder preform. However, results indicate that stencil designs that maximize the solder paste under the component result in less voiding, indicating that a maximum amount of solder is required under the QFN. Following the QFN manufacturer's design recommendations is a good starting point.

Preform Geometry

Experimentation has shown that the best results are achieved when the solder preform occupies approximately 80 to 85% of the area of the PWB pad, and is approximately 50% of the printed paste thickness. However, a minimum preform thickness of 0.0015" is required to prevent preform bending.

The ratios in Table 2 are not fixed; they are merely a starting point. For instance, a larger pad area might require a solder perform closer to 80% of the pad area. However, the solder paste must provide tack for the preform and the QFN. Therefore, allowing for paste around the perimeter enables the solder paste on the edge of the preform to provide good tack to the QFN. This will help prevent skewing during reflow.

Preform Design:

QFN	
4 x 4	9 x 9
Thermal Pad	
2.15 x 2.15	7.25 x 7.25
Preform Geometry	
1.83 x 1.83	7.25 x 7.25
.002"	.002"

Table 2: Calculation for a suggested solder perform dimension.

Figure 4: Illustration of a rectangular solder preform placed on the solder paste.

Placement Pressure Preform	Placement Pressure Component	Placement Performance
2n	2n	Poor
5n	3n	Fair
4n	3n	Good

Table 3: Placement pressure in Newton's.

Placement Recommendations

Since the solder preform is packaged in tape-and-reel, its placement can be manipulated easily to achieve the desired result. To ensure there will be sufficient tack to hold the QFN component, the preform must be pushed into the paste far enough to allow for the solder paste contact to the QFN (Figure 4). If this result isn't achieved, component floating will occur. The solder preform placement force is critical, as the preform still needs to be as flat as possible after it is placed into the paste. In addition, component placement pressure should be increased to ensure that the component seats well in the paste along the perimeter of the preform (Table 3).

Increased placement pressure on the solder preform can result in its bending. The pick-and-place nozzle should occupy the most surface area possible on the preform (Figure 5). The best nozzle will support the preform to preserve flatness, as bending can result in skewing of the QFN at reflow.

Flux Coating

The interface between the top of the solder preform and the thermal pad on the QFN does not contain paste; therefore, there is no flux to prepare the surface for solder wetting. This shortcoming can also cause excessive voiding. The solution is a flux-coated solder preform (Figure 6). A solder preform, coated with NC-9 flux at 1 to 1.5% by weight, will be sufficient to ensure good wetting without incurring voiding. The flux coating must be deemed compatible with the paste used.

Reflow Profile

When adding a solder preform to the process, reflow profile adjustments are not specified or required. In cases of low thermal mass, a more linear profile is acceptable, but in cases of high thermal mass, a soak profile is required. The addition of a solder preform has actually

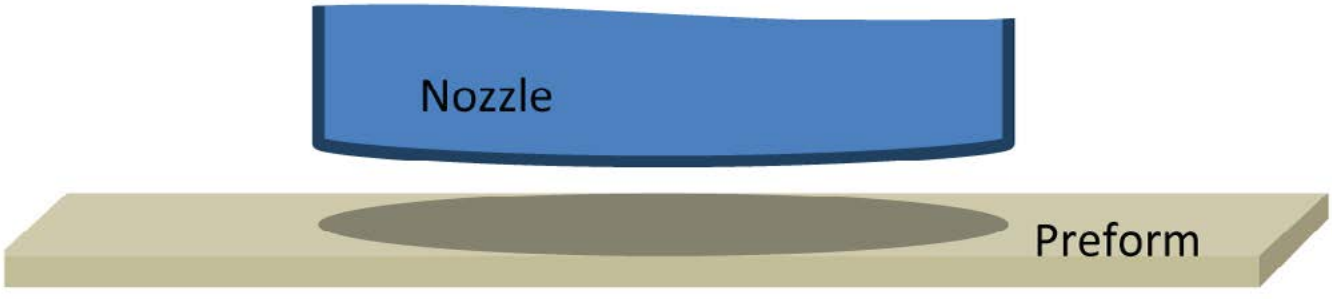

Figure 5: The desired relationship between the nozzle and the solder preform.

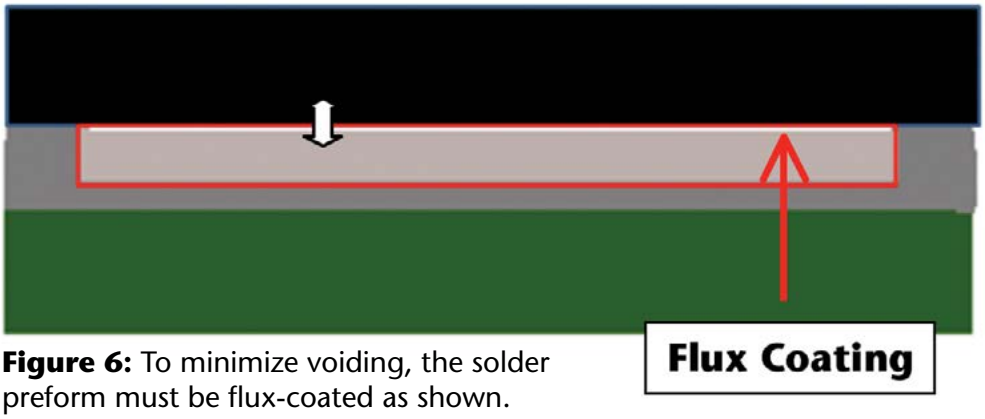

Figure 6: To minimize voiding, the solder preform must be flux-coated as shown.

been shown to reduce variability from one board to the next and is tolerant of reflow profile adjustments.

Collaborative Testing Overview

To evaluate the effectiveness of solder preforms in minimizing voiding in QFNs, a collaborative investigation was performed. The critical parameters in this study are listed below

- QFN thermal pad dimensions (dims): 2 mm x 2 mm;
- Paste: No-clean solder paste with 89% SAC387, Type 3;;
- PWB pad dims: 2 mm x 2 mm;
- Stencil dims: 2 mm x 2 mm x 0.004" thick;
- Preform dims: 1.7 mm x 1.7 mm x 0.002" thick;
- Flux coating: NC-9 @ 1.0% by weight; and
- Profile: Soak.

The resulting voiding average was less than 10% and improvement from the initial voiding average can be as much as 50% or more of the solder joint.

Conclusion

As stated, voiding under QFNs is attributed to flux entrapment and/or lack of solder in the joint. The addition of a solder preform dramatically increases the solder content without excessive flux. The additional solder density residing in the center of the pad also inhibits the development of a large void.

To minimize voiding, design considerations should include

- Stencil design: Manufacturer recommended;
- Solder preform geometry: Approximately 85% thermal pad dimensions and 50% paste thickness;
- Placement parameters: Increase placement pressure, muzzle selection;
- Flux coating: Required for solder preform/QFN interface; and
- Reflow profile: Dependent/flexible. **SMT**

Seth Homer, product support specialist for Engineered Solder Materials at Indium Corporation, serves as manufacturing supervisor for various engineered electronics assembly materials, including solder spheres, sputtering targets, indium chemicals, and solder preforms. Homer has also worked extensively with company Customer Support teams, especially those in China, Singapore, and Europe. He can be reached at shomer@indium.com.

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Supplier/New Product News Highlights

Indium Releases New PoP Solder Paste

Indium9.91 is a no-clean solder paste designed for use in package-on-package (PoP) applications 0.3 mm and larger. Its rheology optimizes both dipping and package retention. The paste eliminates defects due to package warping, provides excellent solderability, features a long pot life, and provides consistent solder paste volumes.

Koh Young Truck Tour Rolls Through the U.S. Southwest

The tour brings the best that 3D inspection technology leader Koh Young has to offer in SPI and AOI systems to 25 states throughout the continental U.S. for a span of 90 days. The tour involves more than 60 hands-on equipment demonstration locations designed to make it easier and more convenient for engineers to experience the equipment first-hand.

JTAG CoreCommander Checks-Out FPGA Zone

CoreCommander for FPGAs, from JTAG Technologies, offers a generic solution based on VHDL code that allows engineers to bridge from the standard JTAG test and programming port (TAP) to proprietary IP cores (e.g., DDR controllers, E-net MAC, USB controllers, etc.) and harness them for test purposes.

EMS Provider BTW Invests in Aegis MOS Software Suite

EMS provider BTW Inc. has purchased an entire suite of Aegis MOS software modules to support their continued expansion into demanding military and medical market areas. This investment was to provide speed to revenue, mistake-free manufacturing processes, and accelerated reporting capabilities for use by both BTW's management and customers.

Fuji Electric Partners with Zollner on EV Chargers

"Fuji Electric has built a 90-year reputation on its high manufacturing standards, and Zollner Electronics Inc. immediately jumped to the top of our list when we were seeking a U.S. partner for local design and manufacturing of our DC Quick Charger," said Larry Butkovich, Fuji Electric's general manager of EV Systems. "Working with Zollner allows us to continue using Fuji Electric's core technology while quickly responding to local market demands here in the U.S."

Manncorp Unveils BR790-HD Rework System

The BR790-HD rework system allows operators to safely remove, align, place, and solder BGAs, CSPs, ultra-fine-pitch QFPs, and other delicate, heat-sensitive SMDs with ease. The system's 1.3 million pixel, split-vision optics, and 15" high-resolution display make fast, accurate work of component alignment via superimposed images of leads and solder pads.

Indium Continues Expansion; Creates Nanotech Team

Indium Corporation announces the creation of a Nanotechnology Team to support the company's continued expansion into novel nanotechnology materials and markets. "Nanotechnology" is a term that describes materials that are less than 100 nanometers (0.1microns) in one or more dimensions. It also encompasses products that are made using nanotechnology, as well as products that are used in nanotechnology-based processes and materials manufacturing.

Chemtronics Debuts Konform Utra

Chemtronics' Konform® ultra-fast-dry acrylic conformal coating is formulated to provide maximum process throughput while maximizing insulation protection against high-voltage arcing and corona shorts. It quickly dries to the touch, allowing for fast production turnaround. The coating provides a hard, durable protective barrier against humidity, salt, corrosive vapors, and fungus for PCB and electronic assemblies.

LPKF StencilLasers Can Now Produce Step Stencils

Exciting news from LPKF's process engineers: StencilLasers can now produce high-precision steps in solder paste stencils, given suitable process control. The process was presented at SMT Nuremberg 2013 by the Garbsen, Germany-based specialists in laser-based micromachining and is described in detail on the company's website.

Scorpion Implements eez-Technology

Essemtec has implemented eez-technology for its dispensing system Scorpion. The technology is already successfully used on the pick-and-place machines Paraquda and Cobra. Scorpion can dispense up to 120,000 dots per hour with an accuracy of 51 µm (3).

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Inclusion Voiding in Gull Wing Solder Joints

by Theron Lewis, Jim Wilcox, and Cheikhou O. Ndiaye
IBM CORPORATION

SUMMARY: While solder voiding in BGA solder joints has been extensively investigated and characterized, solder voiding phenomena in other SMT soldering configurations and their reliability impact have not been as clearly identified. Authors from IBM define and examine voids encountered in gull wing solder joint geometries.

Editor's Note: This paper was originally published in the Proceedings of IPC APEX EXPO, Las Vegas, Nevada, February 28-March 1, 2012.

Abstract

Solder voiding in ball grid array (BGA) solder joints has been well characterized and documented in IPC-A-610 and IPC-7095 which define industry recommended BGA solder workmanship criteria and methods of inspection. Solder voiding limits associated with other, non-BGA, SMT solder joint types however are neither well defined nor well understood in the industry.

According to IPC guidelines, the amount and size of solder voids are simply to be specified by customer/vendor agreement. In the absence of well-defined voiding criteria though, the morphology of solder joint fillets seen in final visual inspection often becomes the sole arbiter of solder workmanship and quality. Among the various SMT solder interconnect designs used in IBM applications, one of the more common SMT leaded structures is the gull wing design found on SMT connectors.

Three distinct types of solder voiding have been observed in these gull wing solder joints: Solder inclusion voids, solder exclusion voids, and solidification hot tears. The most prevalent of the three has been inclusion voids, also known as solder process voids. Such solder inclusion voids in SMT leaded solder joints have been observed using either IR/convection or vapor phase reflow processes.

This paper provides definitions of the different voiding types encountered in gull wing solder joint geometries. It further provides corresponding reliability data that support some level of inclusion voiding in these solder joints and identifies the final criteria being applied

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for certain IBM server applications. Such acceptance criteria can be applied using various available X-ray inspection techniques on a production or sample basis. The bulk of supporting data to date has been gathered through RoHS server exempt SnPb eutectic soldering operations, but it is expected to provide a reasonable baseline for pending lead-free solder applications.

Background

Solder voiding has been a common phenomenon in mass reflow soldering processes used in the server/telecomm industries, being variously characterized as process anomalies, process indicators and/or solder defects. As surface mount technologies have taken precedence over pin-through-hole (PTH) technologies, ball grid array (BGA) components have been the main vehicle for industry classification of solder joint voiding. A solder void is defined here as a hole or enclosed volume of space within the solder joint that lacks solder material. This space may be comprised of a combination of gas, solid residues and liquid non-metallic materials, or possibly vacuum. The main classifications of solder voiding within BGA and PTH soldering applications have been identified by Aspandiar [1] as the following:

Inclusion/Macrovoids: Voids containing by-products that result from fluxing reactions inherent to the solder reflow/melting process. Also known as process voids, these voids generally do not affect interconnect reliability unless they are present at interfacial regions of the solder joints where cracks can form or they accumulate at other regions of local stress concentration.

Planar microvoids: Small voids residing substantially in a common plane at the interface between the PCB lands and the solder. These voids are uncommon on PCBs using OSP finishes, but can occasionally be found on PCBs with fusible metal surface finishes such as immersion silver [2]. Such metal surface finishes can entrap hollow caverns within the finish deposit as an artifact of the deposition process. These caverns would, in turn, locally outgas during soldering to produce fine arrays of interfacial voids. Planar microvoids are generally not detectable in time zero functionality test, but can seriously degrade solder joint reliability.

Shrinkage voids: Voids caused by the volume shrinkage of the solder alloy on the phase change from liquid to solid. There is a low incidence of shrinkage voids in SnPb eutectic soldering. They are seen more frequently with SnAgCu solder alloys. These voids necessarily form in the regions of the joint that are last to solidify, most frequently in the middle regions of the solder joint furthest removed from the interfacial intermetallic regions formed between the solder and base metals of the components leads or PCB lands. There are no documented instances showing that shrinkage voids affect solder joint reliability.

Microvia voids: Voids that are formed from the outgassing of microvias in a PCB land, either capped or open. Voids are usually a consequence of solder reflow and the characteristics of the micro-via. Large micro-via voids located in stress concentration points within solder joints and high stress areas of a package can possibly affect reliability of the interconnect [3].

Intermetallic microvoids: Voids that form within the intermetallic compound (IMC) between the base metal of the component lead or PCB land and the solder. These voids do not form immediately during the soldering process, but grow after extended thermal aging. IMC microvoids can substantially degrade the interconnect reliability through embrittlement of the interfaces [4].

Pinhole microvoids: Voids caused by entrapped PCB fabrication chemicals within pinholes of the Cu lands or PTH walls that react during the reflow soldering process. The pinholes occur due to outgassing within the copper plating process at the PCB fabricator [1].

IPC-A-610 [5] and IPC-7095 [6] define BGA solder workmanship criteria and methods of inspection, respectively. Solder voiding limits associated with other, non-BGA, SMT solder joint types however are neither well defined nor well understood in the industry. According to IPC guidelines, the allowable level and size of non-BGA solder voids are simply to be specified by customer agreement. In the absence of well-de-

fined voiding criteria though, the morphology of solder joint fillets seen in final visual inspection often becomes the sole arbiter of solder workmanship and quality. The objective of the present work is to provide meaningful acceptance criteria for solder voids encountered in gull wing solder joint geometries.

This work provides supporting reliability data to safely allow some level of inclusion voiding in such solder joints and further identifies the final acceptance criteria being applied for certain IBM server applications. The proposed criteria can be applied using available X-ray inspection techniques on a production or sample basis with verification by destructive techniques such as cross sectioning or dye-and-pry inspection. The bulk of supporting data have been gathered from SnPb eutectic soldering operations (RoHS server exempt), but are expected to provide a reasonable baseline for pending lead-free solder applications as well.

According to IPC guidelines, the allowable level and size of non-BGA solder voids are simply to be specified by customer agreement. In the absence of well-defined voiding criteria though, the morphology of solder joint fillets seen in final visual inspection often becomes the sole arbiter of solder workmanship and quality. The objective of the present work is to provide meaningful acceptance criteria for solder voids encountered in gull wing solder joint geometries.

Industry Specifications for Solder Voiding

As stated previously, the most commonly referenced industry standard for solder joint workmanship, IPC-A-610, defines acceptability criteria for solder voids within BGA solder joints. For most IBM server applications, Class 2 requirements apply and IPC-A-610 workmanship criteria are followed with only minor modifications. For Class 2 product, IPC-A-610 defines BGA solder voids to be a defect is when the cumulative projected area of all voids in any given solder ball is greater than 25% in an X-ray image. IPC-7095 is much more comprehensive in its treatment of voiding in BGA solder joints; describing sources of voiding, how to calculate the void percentage guidelines, how to inspect for voiding, providing recommendations for control limits for multiple applications and providing methods of process characterization with multiple corrective action recommendations for specific BGA applications.

Of note, IPC-7095 states that, "Current industry data suggests that voids in the solder joint are not a reliability concern. In fact, the appearance of a void after assembly reflow is an indicator that the reflow process has taken place and the BGA ball has changed characteristics." Most research agrees that voids by themselves are not a reliability concern, but rather the location of the voids within the solder joint that determines their negative impact, if any, on the reliability of the joint. Voids forming at the intermetallic layers/interfacial surfaces near the base metals of the component metal leads or PCB lands can be stress concentration points for cracking during aging and environmental stress situations [7].

For non-BGA solder joints IPC and other industry standards for voiding are not as rigorous. IPC-A-610 declares, "Blowholes, pinholes, voids, etc.," to be process indicators for Class 2 product "providing the solder connection meets all other requirements." Thus it stipulates no limits on the size of internally contained solder voids in SMT gull wing joints. IPC-A-610 does define acceptable and unacceptable workmanship criteria for solder joint fillets. If the amount of voiding is acceptable to the customer and the solder fillets meet IPC-A-610 workmanship criteria then the solder joint meets required form, fit, and function for all classes. IBM restrictions on solder voids have in the past also been vague, in that for non-BGA solder joints the solder voiding shall be less than 25% of the solder joint [8]. At the present, there is no viable non-destructive technique that can be used to implement this acceptance criterion in production, limiting its

usefulness. Considering that server applications are using increasingly more solder interconnects that are non-BGA, including SMT array backplane connectors, this criterion needs to be redefined [9].

Voids Observed in SMT Array Connector Gull Wing Joints

Inclusion Voids

The most frequently observed solder voids in leaded SMT array connectors are inclusion voids. Similar to BGA process voids, these gull wing inclusion voids are large macrovoids generated by flux reaction by-products entrapped in molten solder. Solder inclusion voids are a long recognized, and virtually unavoidable, consequence of SMT solder paste assembly. Most entrap fully activated, no-clean flux residues. In gull wing SMT joints, these voids range in shape from roughly spherical to highly-elongated (cigar-shaped) morphologies. All have a bubble-like appearance with smooth walled surfaces. Figure 1 shows several examples of inclusion voids in gull wing solder joints.

Solder Exclusion (Squeeze-out) Voids

Conventional SMT solder joints are designed to form an equilibrium shape through the action of liquid surface tension as the component floats unconstrained in the molten solder. The surface tension induces component centering on the PCB copper pads as well as component floating off the PCB surface and thus formation of joints with a finite solder bond line thickness. In the case of high-mass SMT backplane connectors however, the mass of the component far exceeds the capacity for solder surface tension to maintain its equilibrium position on the PCB surface pads.

Moreover, in applications where SMT connectors or components are sensitive to vibration or mechanical disruption, locking alignment pins must be used. Such connectors must be constrained in position through the reflow cycle using external mechanical fixturing and/or guide pin locking mechanisms.

Further, the coplanarity of gull wing leads is generally difficult to maintain within the limits of the solder paste deposit height and board surface flatness over large arrays. Consequently, the mechanical positioning fixture of these connectors must also impose a hold down compressive load to force additional coplanarity onto the lead array. This applied load will be predominately borne by some fraction of the lead array that contacts the seating surface before other SMT leads and will necessarily squeeze out the solder paste deposit from under the highly loaded leads. This squeeze-out of a solder paste is visible in the paste impression of Figure 2. Paste squeeze-out locally forms zero bond line thickness between SMT leads and the PCB surface and prevents solder from adhering to the two attachment surfaces.

Since no solder is present under this highest leads, X-ray inspection images will show a

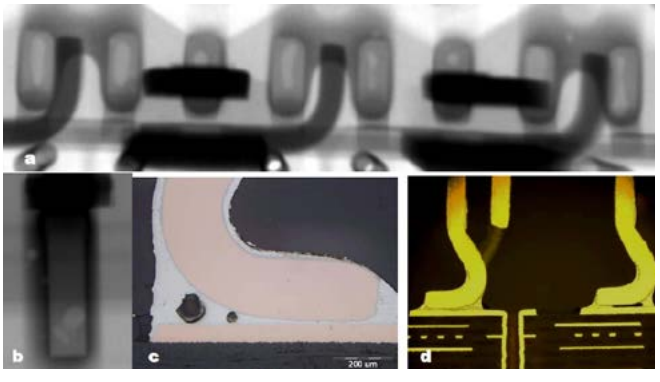

Figure 1: Inclusion voids observed in SMT gull wing solder joints with 2D X-ray (a, b) and cross section (c, d).

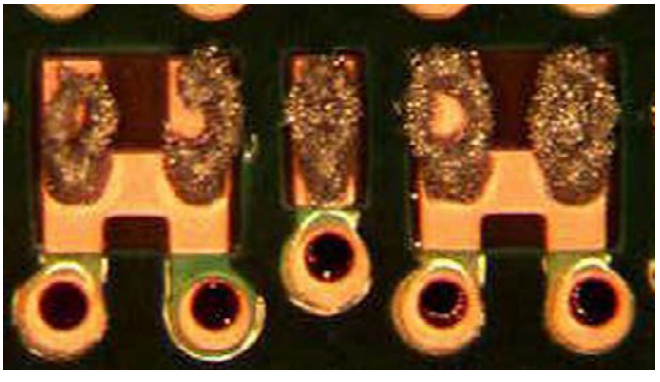

Figure 2: Solder paste impression showing solder displaced (squeezed out) from under the highest leads.

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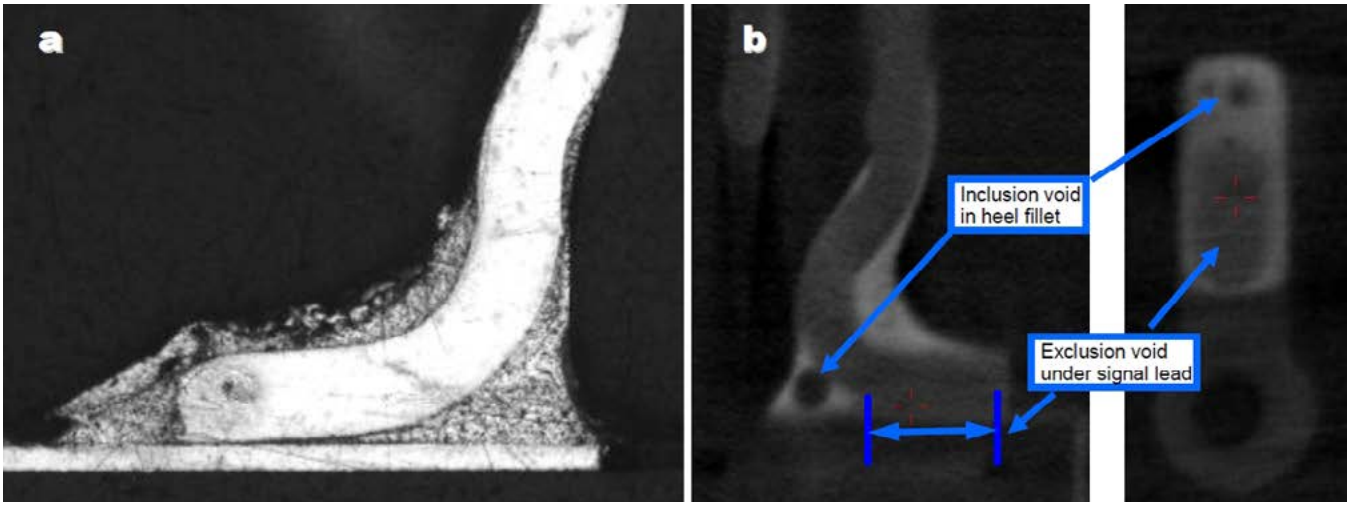


Figure 3: Solder exclusion voids found in SMT gull wing solder joints viewed in a.) cross-section and b.) 3D X-ray scans.

locally-voided region. Examples of solder exclusion voids are shown in Figure 3.

Motion Induced Voids: Hot Tearing and Ductile Rupture

Hot tearing is a well known solidification phenomenon in the field of metal casting [10]. As the solidification front in a mass of molten metal propagates through the melt, the front must always have access to a stable pool of liquid metal to supply the solidification process and form a defect-free solid. If that liquid supply is disrupted, the solidifying metal is starved for material and leaves void or space in the final casting. In metal casting, the most common reason for disrupting the supply of liquid is solidification nucleating on opposing fixed external surfaces.

In the case of SMT gull wing component soldering, hot tearing occurs through motion and/or disturbance of the joint during solidification by outside environmental factors and/or internal material design issues with the component. Specifically, a thermally-induced dimensional instability in the component materials or the relative displacement of individual leads accumulates as solder solidification events propagate through a large array component. This displacement forces sufficient separation of liquid solder from solid to form a tear or void. If the solder joint has fully solidified prior to the disruptive displacement, ductile rupture may occur in the solder at some high homologous temperature just below the melting point.

Either mechanism produces a solder defect beneath the lead foot. One should note that often the solder fillets are still visually maintained during such tearing or rupture events. Examples of motion induced voids are shown in Figure 4.

Other types of solder joint voiding not observed in the present array connector application, and hence not discussed here, include microvia induced voids and interfacial microvoiding phenomena such as planar microvoiding from surface finish reactions [2] and Kirkendall-like solid state voiding in the Cu3Sn intermetallic [4].

Gull Wing Solder Process Void Experience

The high-density area array gull wing SMT connector of interest is used in a range of enterprise server class products assembled at various manufacturing sites. While the bulk of assembly production to date has used SnPb eutectic solder, several lead-free solder applications have recently been qualified [11]. Depending on the thermal masses involved, some are reflowed with conventional forced convection reflow while others must use a vapor phase reflow process to accommodate the very high thermal mass of the connector assembly. Despite this manufacturing variety, occurrences of solder inclusion (or process) voids have been observed in all cases.

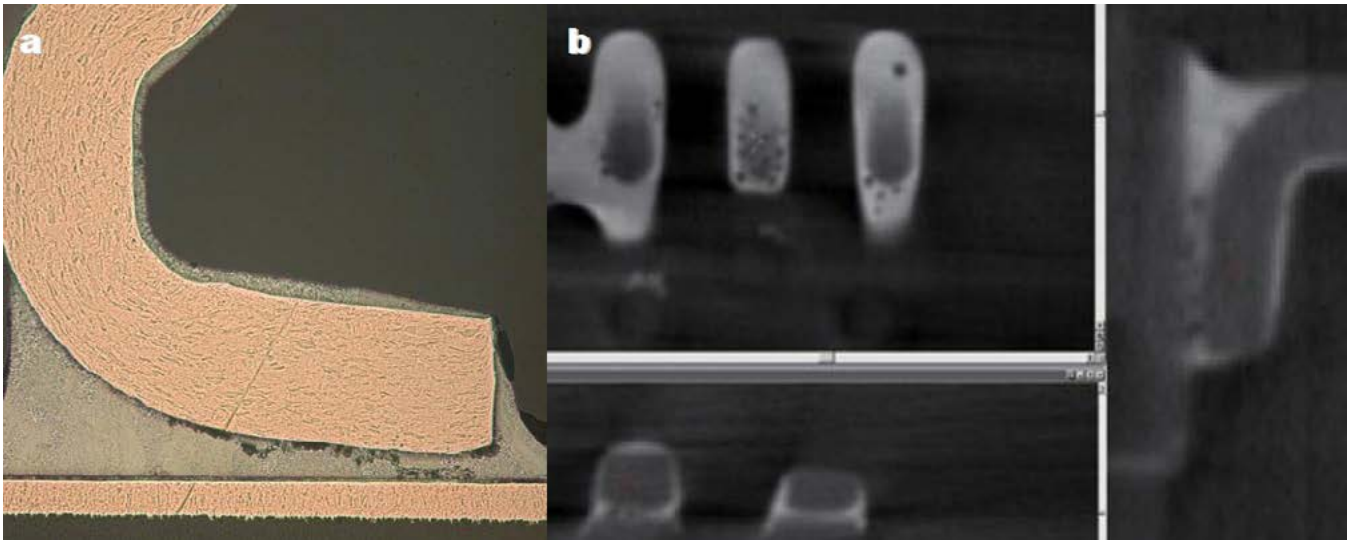


Figure 4: Motion-induced (ductile rupture) voids found in SMT gull wing solder joints using a) cross-section and b) 3D X-ray scans.

Solder inclusion voids are found in both header and receptacle backplane connectors, each of which use fundamentally similar copper lead geometries. Because of the obscuring mass of the receptacle connector body, voids tend to be more readily observed in X-ray inspection of the header connectors. It may also be that the receptacle wafers can exhibit more temperature induced movement (distortion) during reflow and may thus be less likely to capture stagnant voids of process gasses under the leads.

Solder Joint Mechanics

The importance of a well-formed solder fillet to the structural integrity of a solder connection has long been recognized. The IPC-A-610 workmanship criteria for gull wing solder joints require a wetted fillet along the full length of the lead and a minimum height heel fillet.

Figure 5 shows the solder joint stress distribution from a simulated thermal excursion (low-temperature shipping cycle) to illustrate the perimeter nature of temperature induced stresses. The lead depicted resides near one end of large array connector. Starting from a relaxed solder joint state at room temperature and cooling to -15°C, the simulation reveals that substantial tensile stresses accrue in the heel fillet only. In the general case for thermal cycle loading, much of the load applied to any individual gull wing lead will be borne by at least one of the solder fillets. The specific fillet bearing the

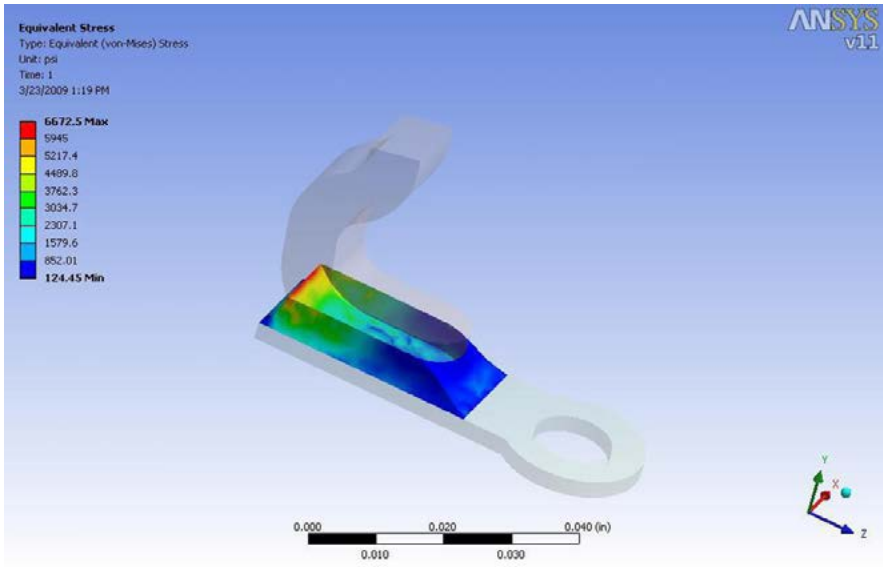


Figure 5: Stress simulation of an SMT array connector gull wing solder joint during a low-temperature excursion (shipping). Tensile stress is concentrated in heel fillet. (A. Sinha, [12])

peak load will of course depend on the sense of the temperature excursion, the position of the lead in the SMT attachment array and the construction of the connector body. In all cases though, the central region directly under the gull wing foot bears only a minor fraction of the applied load.

Similarly, lateral shock or vibration loading of the connector assembly will apply bending moments to the gull wing lead joints and again primarily load the perimeter solder fillets. For all anticipated operating and product usage loads, barring perhaps the abnormal case of a direct tensile load on the connector housing, the load bearing requirements of the solder bond line beneath the gull wing lead foot will be minimal.

Local voided solder regions directly under the gull wing lead foot will therefore have negligible impact on the ability of an otherwise well formed solder joint to withstand operational loads and thermally induced stresses. Solder joint structural integrity arises substantially from the perimeter solder fillet.

Eutectic SnPb solder inclusion voids in connector gull wing solder joints have been found to nearly always coalesce into a single, large cigar-shaped void directly under the central region of the lead foot. The stress concentration associated with a smooth walled void, located away from the high stress fillet regions, was found to be small and thus have minimal impact on the thermal fatigue mechanisms operating in the solder fillet regions. The primary objective of the solder joint quality specification strategy should therefore be to assure the structural integrity of the load bearing solder fillet regions.

Gull Wing Inclusion Void Specification Strategy

Given the limited structural impact of inclusion voids directly under the gull wing lead foot, the industry recognized IPC specification limit for BGA solder void acceptability was deemed inappropriate for SMT array connectors. An internal specification was instead defined that considers the structural, load bearing characteristics of the gull wing solder joint.

Rather than using the radiographic projection—the maximum solder area—as a reference basis for void size (as is done for BGA joints in IPC-A-610), the recommended gull wing inspection strategy would instead reference the void area to the minimum load bearing area, a discrete slice of solder just beneath the lead foot. This minimum load bearing solder area will be defined as a critical reference area for judging acceptable void size. Since the solder fillet extends outward from the lead to the perimeter of the PCB pad at its base, this plane of minimum load bearing area will most commonly occur just beneath the gull wing lead and have an area smaller than the PCB pad area.

The proposed inclusion void specification strategy is illustrated schematically in Figure 6:

- A critical solder joint area is defined as that area of the solder joint subtended by a plane parallel to the surface of the PCB just beneath the gull wing lead.
- Allowable inclusion voids are defined by the projected area of the void(s) relative to the critical area reference plane.
- The total area of inclusion voids in any solder joint shall not exceed 50% of the critical solder joint area.

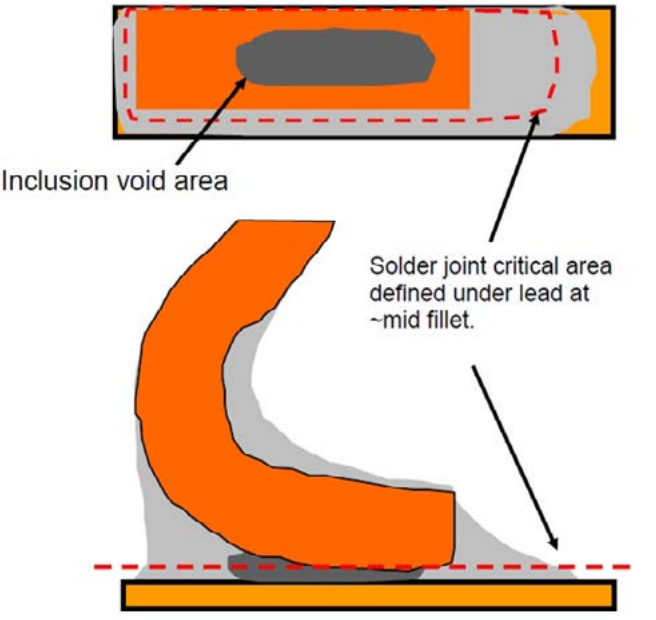
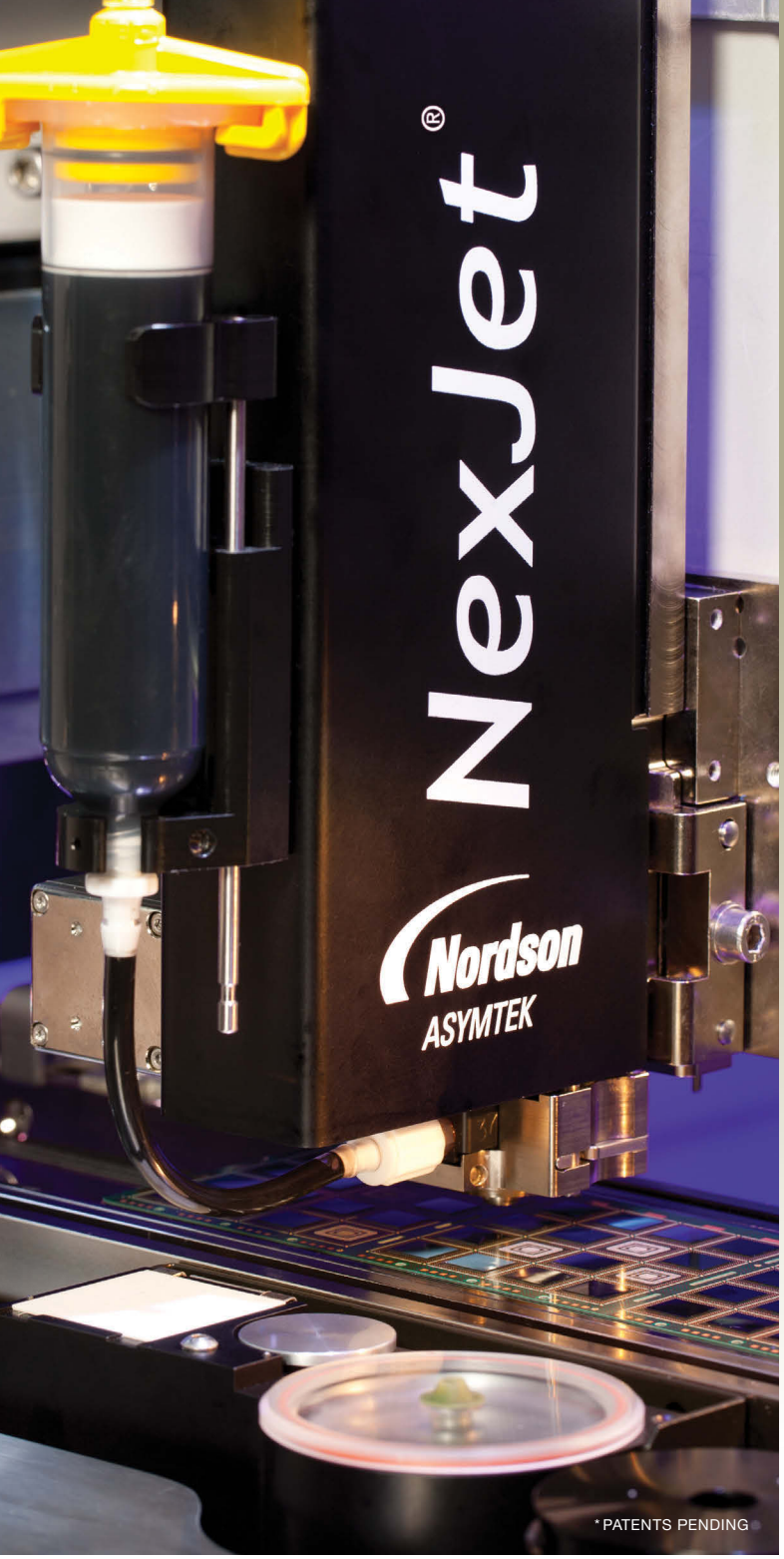


Figure 6: Schematic illustration (top and side X-ray view) of void area measurement in a gull wing solder joint relative to the solder joint critical load bearing area.



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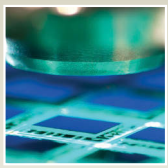

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INCLUSION VOIDING IN GULL WING SOLDER JOINTS *continues*

Instances of solder void area between 25 and 50% of the critical area are deemed solder process indicators.

This specification strategy does require a computed tomography or laminography X-ray inspection tool to capture both the void area and the critical solder joint cross-section area beneath the gull wing lead. Such tools are now commonly used in the production of complex server board assemblies. They can be programmed to produce an X-ray image slice under the gull wing lead and calculate relative void areas in real-time for 100% coverage of production solder joints if desired.

Note that it is not necessary to explicitly specify the allowable inclusion void location. Process voids forming in the lead fillets readily escape to the free surface before solidification, leaving only those voids directly under the lead foot. Inclusion voids in the structurally important side or toe fillets are rare and always small. Instances of small spherical inclusion voids in the heel fillet are not uncommon, but generally they occur above the plane of the defined critical load bearing area. If they are found to intersect the critical reference plane there are should be summed and factored into the acceptability decision.

Figure 7 illustrates void area measurements for successfully qualified product with large SMT array connectors. The void area fraction is indicated relative to the outlined critical load bearing area of the solder connection. Conveniently, a dye-and-pry inspection will most often fracture the solder bond line at approximately the minimum solder cross-section under the lead, therefore exposing essentially the same critical solder bond area defined to be the void fraction reference area. The failure surface can be readily used to measure the relative void size in individual solder joints. Since eutectic SnP inclusion voids are not normally open to the free surface, nor even extend into the solder fillet regions, they would not be expected to exhibit any dye penetration into inclusion voids. Exaggerated shrinkage voids from the fillet regions of SnAgCu solder joints have however been seen to allow some dye ingress into lead-free solder inclusion voids.

Recognizing that X-ray inspection test efficiency in a manufacturing environment is always something less than 100%, the production control limit for process void area in SMT array connectors is maintained well below the specification limit to assure that the shipped product population is safely controlled within the tested range. A process control limit of 25% void area has been established for current production.

A critical point to understand about the proposed void area specification limit for gull wing joints is that it applies only to process induced, smooth walled, inclusion voids—not internal hot tearing voids. Motion induced solder defects in the solder joint are not allowed. They

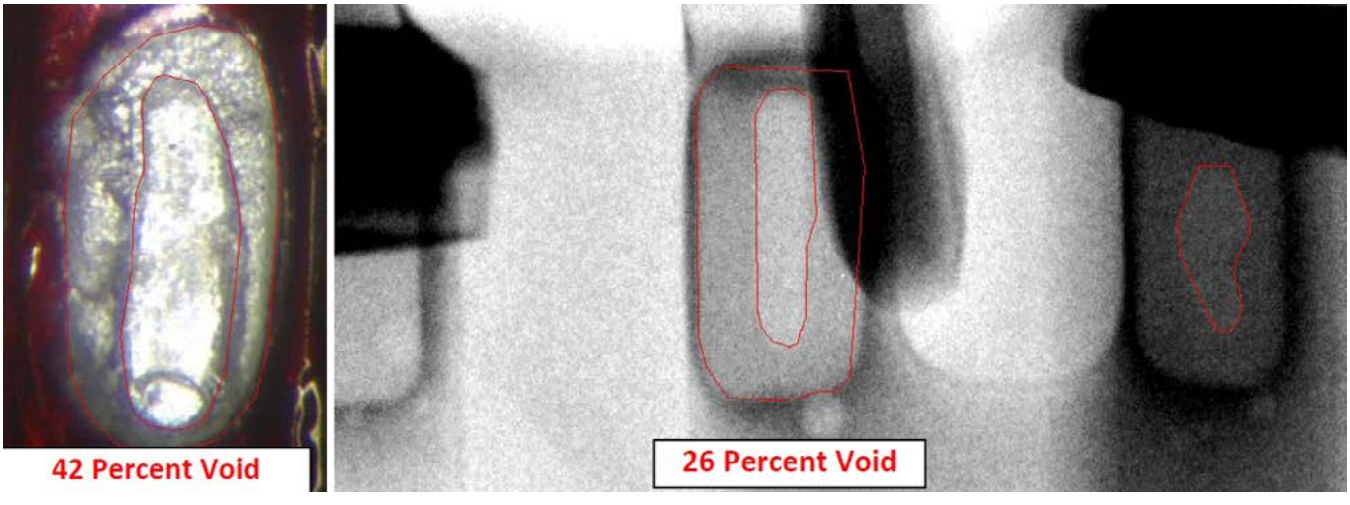

Figure 7: Quantitative void assessment examples from two different array connector product applications: a) Dye-and-pry; and, (b) X-ray tomographic measurement.

must be eliminated through process and fixturing optimization.

Reliability Verification

While the justification for a revised gull wing solder joint void specification was argued heuristically above, experimental confirmation of the resulting interconnect reliability to enterprise server standards is an absolute requirement. This was accomplished in conjunction with eight different board assembly qualifications, each involving SMT array connectors. These qualifications included representative product boards with gull wing connector attachments of varying array sizes, header and receptacle configurations, as well as vapor-phase and convection reflow processes practiced at four different assembly sites. Some boards included multiple array connector types. Candidate product qualification boards were inspected to ensure that instances of solder inclusion voids were explicitly included in the qualification reliability testing.

Solder inclusion voids were confirmed in the various connector gull wing joints of each product qualification sample with void areas measuring up to 50% of the critical reference area. Most of were of the elongated cigar shape morphology. All were in SnPb eutectic solder.

Board assembly qualification for server class product includes a suite of reliability tests on representative product boards. The primary test for establishing wear out characteristics of solder joints is the accelerated thermal cycle (ATC) test. ATC was therefore the primary means of validation for the gull wing solder inclusion void specification.

Translating ATC test results to acceptable field life is generally done with an equation of the form proposed by Norris and Landzberg [13]. Solder fatigue life is expressed in the form of a stress test acceleration factor (AF); the ratio of field life to laboratory test life. The equation is comprised of three terms, each a ratio of laboratory conditions to field conditions: A temperature induced strain term, a cyclic frequency term, and a thermal activation term. Writing the thermal activation term in the classic Arrehenius form, where k ≡ Boltzmann's constant, the Norris-Landzberg equation becomes:

$$AF = \left(\frac{\Delta T_t}{\Delta T_o}\right)^{1.9} \left(\frac{f_0}{f_t}\right)^{\frac{1}{3}} \exp\left(E_a\left(\frac{1}{T_o} - \frac{1}{T_t}\right)\right)$$

ΔT refers to the cyclic temperature range (maximum – minimum), f is the cyclic frequency, and T is the peak cyclic dwell temperature. The subscripts t and 0 indicate laboratory test conditions and field conditions, respectively.

This simplified form assumes isothermal temperature distribution in the assembly, i.e., no temperature differences between components and board. This would generally be the case for assembled boards thermal cycling in a laboratory chamber. The ratio of approximate interconnect strains then simplifies to a ratio of cyclic temperature ranges.

The activation energy for thermal cycle fatigue damage of solder joints, Ea, has been experimentally observed to depend on solder alloy and perhaps package structure. For SnPb eutectic solder, the activation energy has been shown to be 0.12 eV [14]. The SMT array connectors of interest are used exclusively in enterprise server applications where the target field life for product qualifications is 1,250 power-on/off cycles. In a typical server installation, the power-on cycle may drive a 35°C board temperature increase above 25°C ambient (ΔT_0=35°C, T_0=60°C). These parameters are used to calculate the minimum laboratory cycling exposure to assure the required field reliability.

Table 1 lists two examples qualification cases to illustrate the method. In each case, at least 30% of the SMT lead population was confirmed to have some level of inclusion solder voiding in the gull wing solder joints. Key qualification attributes are listed. In Case 1, for instance, five functional boards were subjected ATC test with a temperature cycle of 10 to 70°C at 1 cycle per hour. Each board contained multiple SMT array connectors for a total of 20,160 tested leads per board. Using the modified Norris-Landzberg equation above, the minimum number stress cycles to meet server reliability requirements was calculated to be 561 cycles. All five boards completed 1,000 cycles of ATC testing and remained electrically functional as tested through the SMT connectors.

Case	Number of Functional Boards	Number of SMT Leads per Board	T_t (°C)	ΔT_t (°C)	Acceleration Factor	Cycles per Hour	Minimum ATC Cycles Required	Cycles Tested (PASS)
1	5	20,160	70	60	2.2	1	561	1,000
2	6	1,968	100	100	11	1	112	1,000

Table 1: Two cases of array connector gull wing joints with solder inclusion voids subjected to ATC reliability testing.

In Case 2, six functional boards completed an ATC test with a temperature cycle of 0 to 100°C at 1 cycle per hour. Each board contained two SMT connectors with total of 1,968 SMT leads per board. The minimum number of stress cycles to meet server reliability requirements was calculated to be 112 cycles. All six boards completed 1,000 cycles of ATC testing and again tested to be electrically functional through the connectors. The proposed specification criterion for gull wing inclusion voids was therefore confirmed with a comfortable level of conservatism; from ~2X to 9X the required ATC testing lifetimes without detectable reliability consequences.

Destructive analysis (dye-and-pry and/or cross-section) of solder joints was performed in all qualifications after completion of ATC testing. No solder joint cracks or opens were observed. Figure 8 shows examples of the destructive analyses from the example cases above. No cracks or separations were found in the solder fillets despite the extensive thermal cycle history and obvious solder inclusion voids. Note that ground leads and signal leads of these SMT array connectors have different designs and thus slightly different mechanics and so are identified here as separate cases.

Other forms of reliability stress testing also performed on these same qualification board populations include:

- Thermal ship shock (-40 to 65°C, 5 cycles, 1 CPH);
- High-temperature soak (1,000 hours at 100°C);
- Shock loading (1 meter drop); and
- Vibration (random and sinusoidal loading with full mechanicals attached).

In all of these alternate forms of qualification stress testing, the known solder inclusion voiding in the gull wing solder joints posed no reliability issues.

Conclusions

While solder voiding in BGA solder joints has been extensively investigated and characterized, solder voiding phenomena in other SMT soldering configurations and their reliability impact have not been as clearly identified. In SMT gull wing lead solder joints similar void-

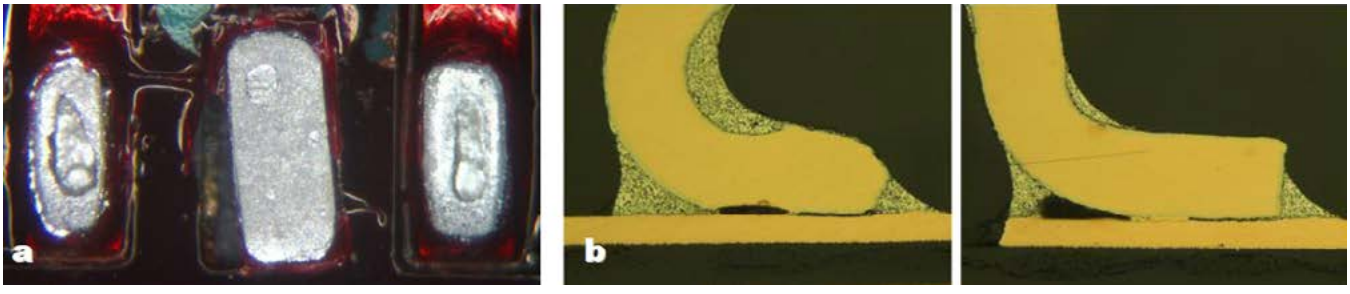

Figure 8: Destructive analysis of voided solder joints on SMT array connectors after 1,000 cycles ATC stress testing without failure: a) Case 1 - dye-and-pry analysis (GND, SIG, and GND); b) Case 2 - cross-section analysis of ground and signal leads.

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ing to that reported in BGA joints has been observed, but gull wing joints also include other void types not characteristic of BGA joints. Solder voids types most commonly observed in the gull wing lead solder joints of SMT array connectors are:

- Inclusion voids;
- Solder exclusion voids; and
- Hot tear voids through mechanical disturbances.

Similar to process-induced macrovoids common in BGA joints, acceptable levels of solder process inclusion voids in SMT gull wing lead solder joints exist below which minimal reliability impact is detected. That allowable void level can be defined according to the projected area of the voids onto the plane of minimum load-bearing area in the solder bond line beneath the lead. The criteria established in this document, confirmed through various ATC and other reliability tests, require that the total projected area of inclusion voids in any solder joint not exceed 50% of the critical solder joint area.

Acknowledgements

The authors are grateful to IBM colleagues Jim Bielick, David Braun, Wai-Mon Ma, Nandu Ranadive, and Mitch Ferrill for the contribution of supporting data to this study from various product qualification exercises. The stress simulations provided by Dr. Arvind Sinha were helpful in the interpretation of experimental results. We also appreciate the reviews and insightful comments on this manuscript provided by Marie Cole and Jim Bielick. **SMT**

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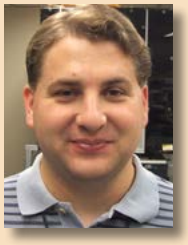

Theron Lewis, IBM ECAT qualification and assembly development engineer, has worked at IBM Corporation for 10 years. His main responsibility is the development and qualification of second-level attach processes for server computer cards. Specific second-level attach processes include initial attachment and rework of a wide variety of components, including high-temperature solder, press fit, and mechanical attachment. A majority of the development work at IBM engages in new connector and area array interconnect technologies with second-level attach processes. Lewis can be reached at theron@us.ibm.com.

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Get More (Products) Out of Your Day

by Sjef van Gastel
ASSEMBLÉON NETHERLANDS B.V.

SUMMARY: A PCB assembly plant invests in SMT flow lines and intends to produce as many quality boards of the required product mix as possible. But, in reality, there will be a big difference in performance over different SMT lines. Why?

It seems the most common response to a request for help is, "Sorry, I just don't have the time." However, a former teacher of mine once said, "We all have the same amount of time to spend (24 hours a day), but it is what you do with it that matters." The same applies to manufacturing equipment and especially to pick-and-place machines. The owner of a PCB assembly plant has invested in SMT flow lines and intends to produce as many quality boards of the required product mix as possible. But, in reality, there will be a big difference in performance over different SMT lines. Why?

The total available time for a manufacturing line is 365 days per year at 24 hours a day, providing 8,760 hours of manufacturing opportunity. But not all available hours will be used: Holidays, breaks, lack of orders, lack of personnel or electricity, and planned maintenance take up some of those hours. In a planned shutdown the unscheduled time is not influenced by the manufacturing equipment installed.

After subtracting these hours for planned shutdown, a facility is left with planned production time.

Overall Equipment Efficiency

To compare the influence of production equipment characteristics on effective line output (the true number of good products per hour) SEMI has defined overall equipment efficiency (OEE) metric in its SEMI-E79 standard. OEE is divided into three main categories of efficiency losses: downtime loss, speed loss, and quality loss.

Downtime loss relates to availability—a metric indicating the percentage of planned production time available for the intended manufacturing process (in our case the pick-and-place process). Downtime can be caused by machine breakdown/failure, repair, lack of materials or operator, product changeover, machine setup/adjustments, and unplanned maintenance. In practice, an availability of approximately 90% is considered world class.

Speed loss relates to performance—a metric indicating the percentage of oper-

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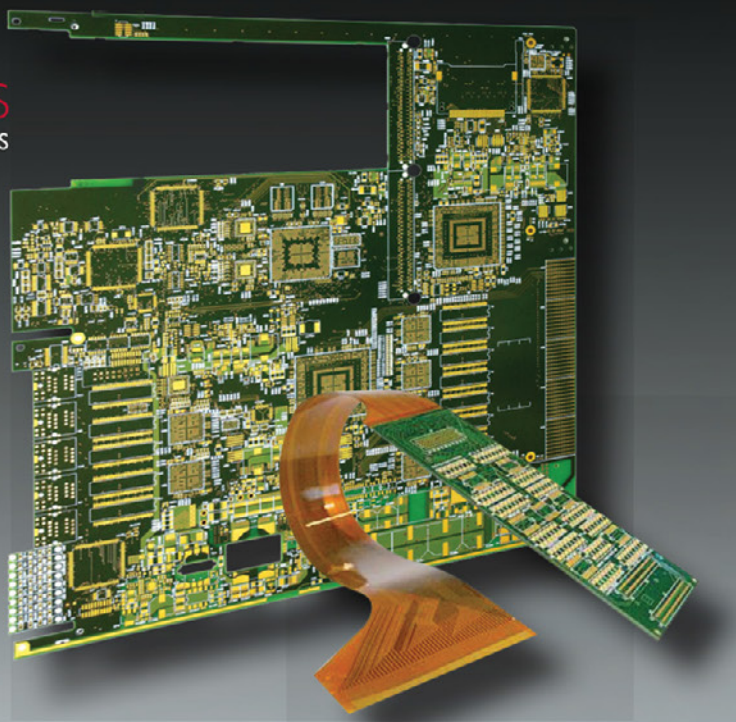

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ating time available for uninterrupted production. Speed loss can be caused by small stops (flow line not balanced, re-pick ppm, cleaning/checking) or by operating below specified capacity (equipment deterioration, operator inefficiency). In practice, a performance of approximately 95% is considered world class.

Quality loss relates to quality—a metric indicating the percentage of net operating time in which the manufacturing system is making good quality products. Quality loss can be caused by incorrect assembly, defective components, or component termination errors (e.g., loose contacts, short circuiting caused by solder bridging). In practice, a quality (first-pass yield) of approximately 99.9% is considered world class.

The overall OEE metric is the product of its three contributing factors: OEE = Availability x Performance x Quality. As a result, world-class OEE levels will be approximately 85%.

The challenge for every production engineer is to maximize the number of good products in relation to operating time, thus maximizing OEE. This can be done by reducing all the time losses as much as possible. Production time loss is always a combination of organizational losses (production planning, factory organization, logistics), line operator losses (operator skills, operator alertness) and equipment losses (equipment failures, underperformance, and errors).

I'll now limit the discussion to the influence of manufacturing equipment on OEE, focusing on pick-and-place machine performance.

Pick-and-Place Machine Performance

Table 1 provides an overview of the most important pick-and-place machine performance characteristics relating to production time losses for machines showing excellent, average, and poor performance. All data are typical for a machine with an average output of 50,000 components per hour.

We can now calculate production time losses for all three of the defined categories (downtime loss, speed loss, and quality loss). This is shown in the following three tables:

- Downtime loss —> Availability;
- Speed loss —> Performance;
- Quality loss —> First pass yield.

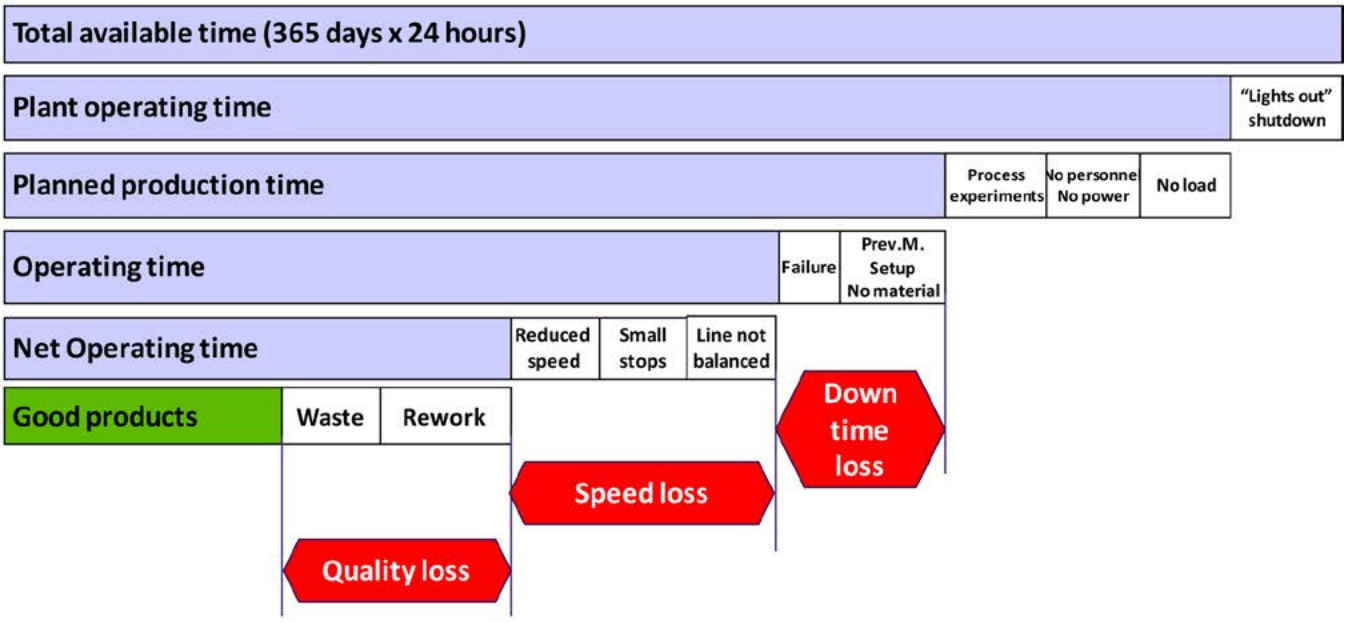

Figure 1: The relationship between different production time loss categories (SEMI-E79 standard).

Table 2 shows the considerable influence of maintenance and changeover on availability. By selecting pick-and-place machines needing little maintenance (lifetime greasing, auto calibration, closed-loop maintenance) and fast changeover (independent dual lane substrate transport, fast feeder exchange, multi-placement programs) the availability of the flow line can be greatly increased.

Pick-and-place machine characteristics	Best	Average	Worst
Output pick & place machine [kcph]	50	50	50
Planned maintenance [min/week]	30	120	280
Placement quality [DPM]	1	30	75
Automatic repicks [ppm]	400	1000	1500
Manual repicks [ppm]	50	100	150
Manual error recovery time [s] (excl. operator waiting time)	30	30	40
MTBF [hrs]	5000	2500	600
MTTR [min]	12	30	180
Typical COT (1 operator) [min]	5	10	20

Table 1: Typical pick-and-place machine characteristics.

Availability calculation table	Best	Average	Worst
Planned production time [hrs/year]	7800	7800	7800
Weeks / year	50	50	50
Days / week	7	7	7
Planned production hours per day	22.29	22.29	22.29
Maintenance per day [min]	4.286	17.143	40
Repair per day [min]	0.022	0.24	5.143
Changeover (COT) time per day (@4 C/O)	20	40	80
Down time loss (per day) [min]	24.308	57.383	125.14
Availability	**98.2%**	**95.7%**	**90.6%**

Table 2: Pick-and-place machine availability overview (excluding organizational and operator influences).

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Performance calculation table	Best	Average	Worst
Operating time [hrs/year]	7658	7465	7070
Weeks / year	50	50	50
Days / week	7	7	7
Planned production hours per day	21.88	21.33	20.20
Line unbalance loss [%]	0	5	10
Line unbalance loss [min]	0	63.99	121.20
Loss due to auto repick actions [min]	2.1	27.42	32.52
Loss due to manual repick actions [min]	27.35	47.6	56.46
Down time loss (per day) [min]	29.45	139.008	210.18
Performance	**97.8%**	**89.1%**	**82.7%**

Table 3: Pick-and-place machine performance overview (excluding organizational and operator influences).

Quality calculation table	Best	Average	Worst
Net operating time [hrs/year]	7486	6654	5844
Weeks / year	50	50	50
Days / week	7	7	7
Planned production hours per day	21.4	19.0	16.7
Placement quality [DPM]	1	30	75
First Pass Yield	**100%**	**97%**	**92.5%**

Table 4: Pick-and-place machine quality overview (excluding rework and scrap cost influences).

Table 3 shows the considerable influence of line unbalance loss and re-pick actions on performance. The influence of line unbalance loss can be reduced by selecting pick-and-place machines with internal substrate buffering positions. These buffer positions act as a parking lot inside the pick-and-place machine for substrates before or after the component placing area. As a result there will be fewer obstructions inside the flow line, giving a better board flow. Time loss due to re-pick actions can be reduced by selecting reliable feeders, (pick) force control, component presence checks, and self-cleaning nozzles.

Placement quality can similarly be considerably improved by selecting the right pick-and-place concept. Here, machines based on parallel placement (with parallel operating placement robots each equipped with single nozzle heads) have the advantage. The reason

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Pick-and-place machine characteristics	Best	Average	Worst
Availability	98.2%	95.2%	87.8%
Performance	97.8%	88.4%	80.2%
First Pass Yield	99.9%	97.0%	92.5%
Overall Equipment Effectiveness (OEE)	95.9%	81.7%	65.1%
Net available hours (good products)	7479	6371	5079

Table 5: Pick-and-place machine OEE overview (excluding organizational and operator influences).

is that acceleration/deceleration forces acting on the vacuum pipettes are much lower than at multi-pipette revolver heads (sequential pick-and-place machines). Also, parallel pick-and-place machines can incorporate closed-loop process control which is impossible on sequential pick-and-place machines. This produces huge differences in placement quality. (And note that these calculations ignore the related rework and scrap costs, which will also make a large difference.)

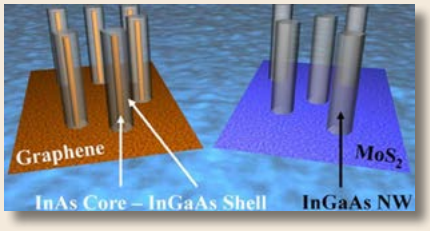
Finally, you multiply all three performance indicators (Table 5). The resulting differences in net available hours (bringing you good products) are remarkable. Just by selecting the right equipment you win valuable production time, enabling you to produce extra good products that will improve your margins.

With pick-and-place machines particularly, time is money. **SMT**

In addition to playing the clarinet in two bands, Assembléon's Sjef van Gastel has another passion: SMT. He has been with the company since its start-up as a Philips division in 1979. As the current Manager for Advanced Development, he combines his experience as systems architect and machine designer to explore technical and business opportunities from emerging technologies. van Gastel holds many patents and is a frequent speaker at international conferences related to SMT. He is also the author of "Fundamentals of SMD Assembly," which has become a standard piece of literature in the industry.

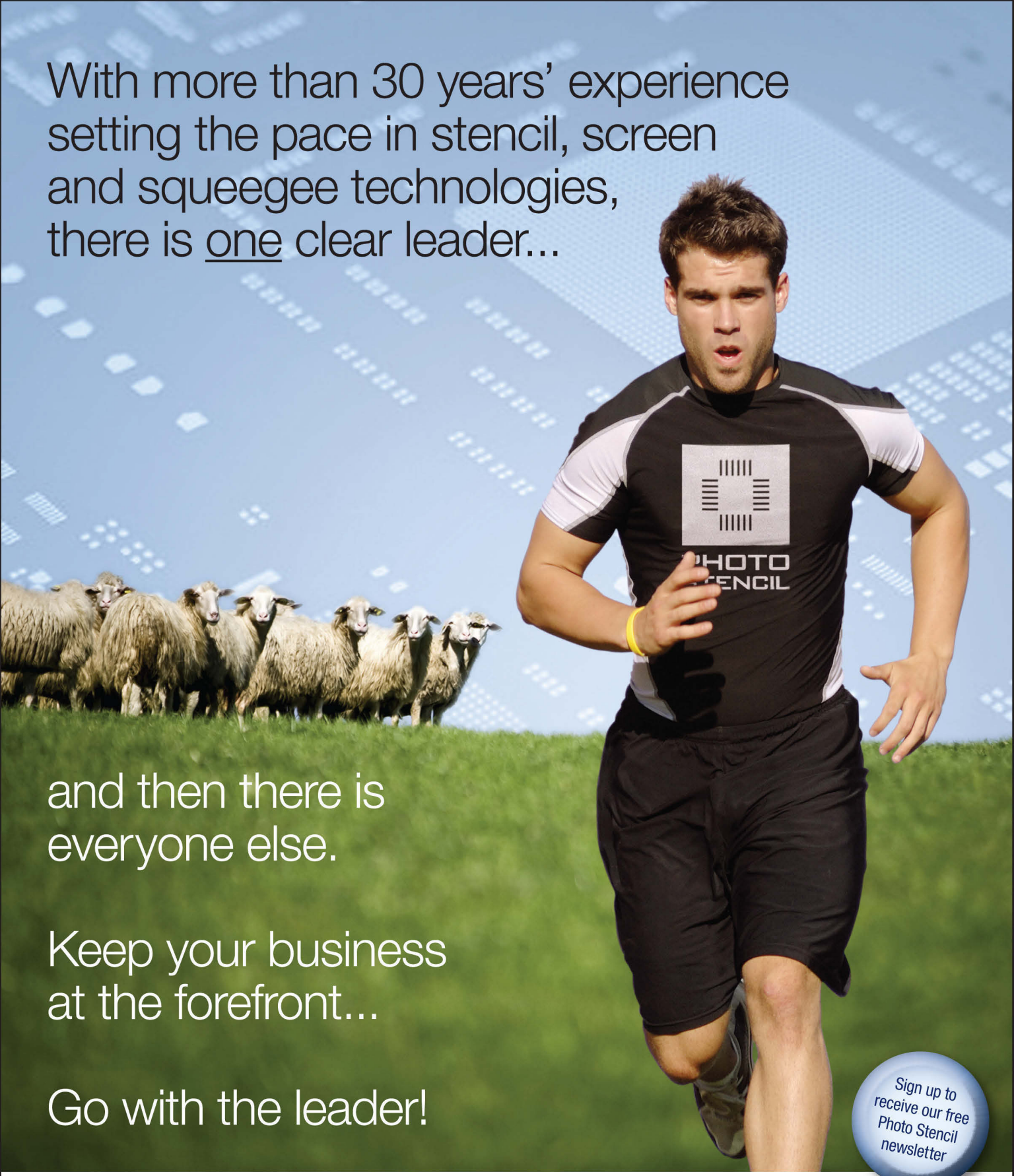
Nanowires Grown on Graphene: A New Paradigm of Epitaxy

When a team of University of Illinois engineers set out to grow nanowires of a compound semiconductor on top of a sheet of graphene, they did not expect to discover a new paradigm of epitaxy.



The self-assembled wires have a core of one composition and an outer layer of another, a desired trait for many advanced electronics applications. Led by professor Xiuling Li, in collaboration with professors Eric Pop and Joseph Lyding, all professors of electrical and computer engineering, the team published its findings in the journal Nano Letters.

Nanowires, tiny strings of semiconductor material, have great potential for applications in transistors, solar cells, lasers, sensors, and more.



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THE SHORT SCOOP

Introduction to Stencil Printing

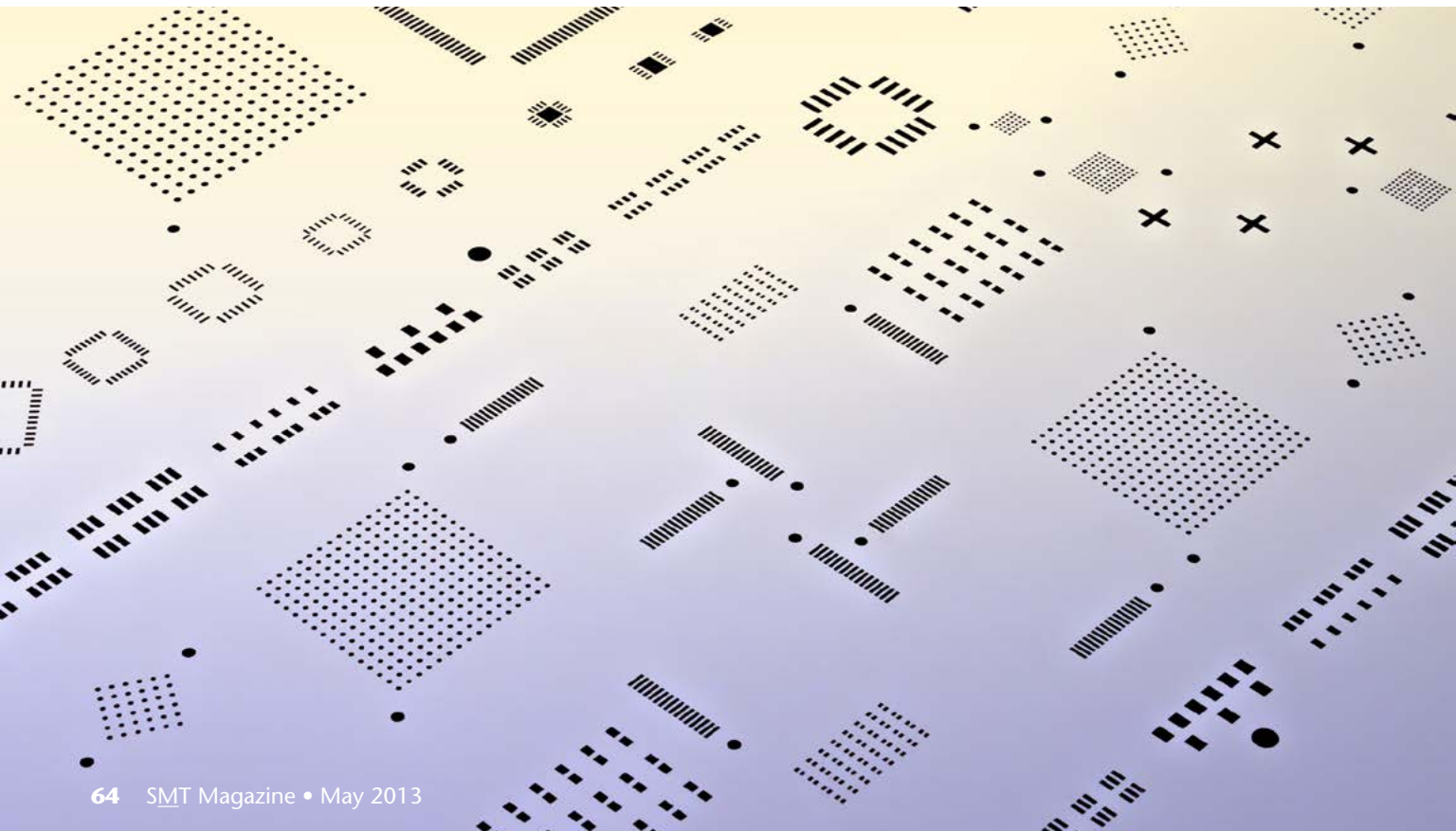
by Rachel Short
PHOTO STENCIL LLC

SUMMARY: Many different types of stencils are available today from many different suppliers, but not all stencils are created equal. And because the industry operates in a quick-turn, dynamic environment, industry lead-times for delivery, in many cases, are as important as the stencil's capabilities.

Approximately 50% of defects that occur on an SMT assembly line can be attributed to the printing process. Doesn't it seem odd, then, that instead of focusing on quality and experienced technical support, stencils have become a commodity and are being sold by a broad range of stencil suppliers, sometimes solely on the basis of price? At the same time, we continue to see more challenging requirements for stencil performance, driven by the continuous miniaturization of packages and components. Many different types of stencils are available today from many different suppliers, but not all stencils are created equal. And because the industry operates in a quick-turn, dynamic environment, industry lead-times for delivery, in many cases, are as important as the stencil's capabilities.

Stencils range from the fairly straight-forward technology of a laser-cut stencil manufactured on some form of stainless steel material, to the high-end full-nickel electroformed stencil, along with many versions and variations in between. Stencil selection depends on the specific technology required for an application. This is dependent on variables such as:

- The smallest pitch component to be printed;
- The mix of components being placed on the board; and
- The area ratio calculation of the smallest component.



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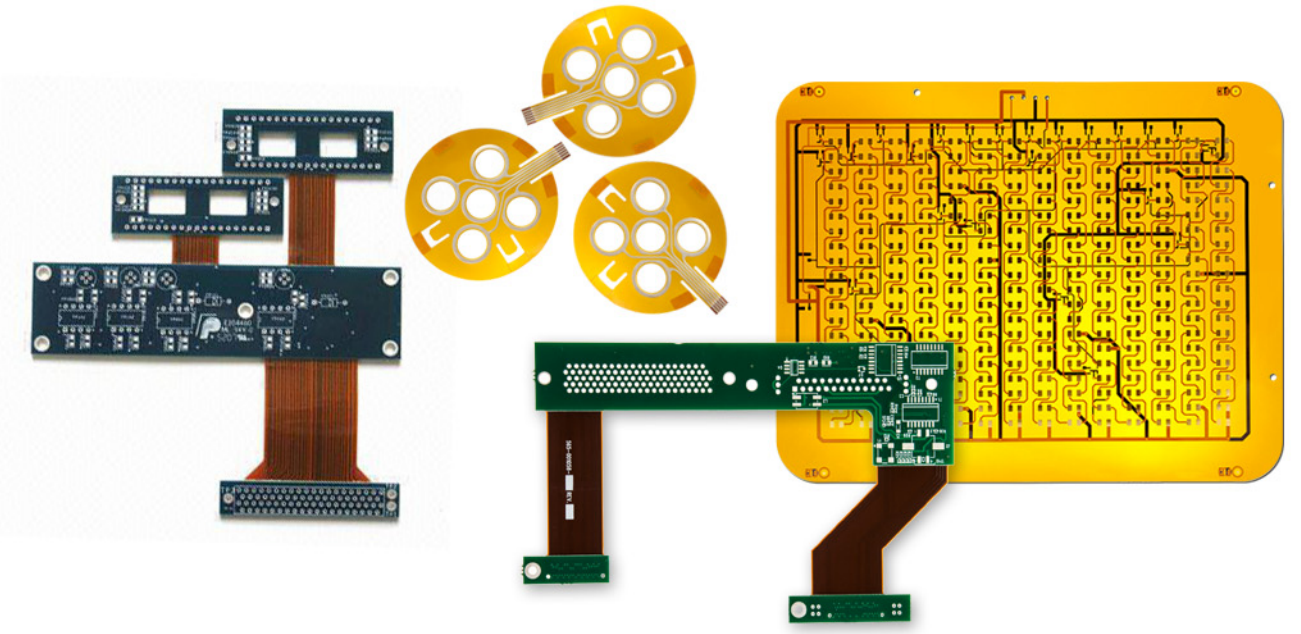

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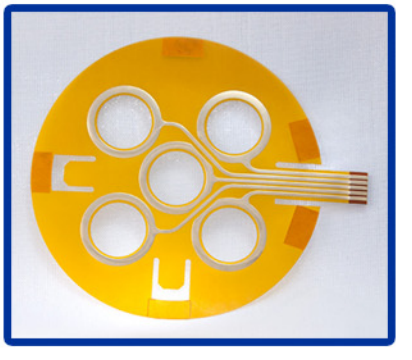

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INTRODUCTION TO STENCIL PRINTING *continues*

Currently, straight laser-cut stencils are the most common. The technology behind laser cutting equipment has continued to improve, coupled with keen improvements in core materials. This has driven straight laser-cut stencil capabilities to expand dramatically, leading to an increase in their popularity and an increase in the volume of straight laser-cut stencil providers. Every stencil performs differently and there are large variations in printing results. The age and capability of the laser used to cut the stencil can have an impact on the print process, and ultimately, on the effect of the area ratio (AR).

Area ratio has become a big factor in differentiating the type of stencil to use. The lower the AR, the more challenging paste release is, thus driving the need for perfect alignment and smoother aperture walls. AR is calculated as area of aperture wall/area of pad under aperture. Whereas ARs of 0.5 to 0.6 used to be considered low, solutions today look for area ratios down to 0.42.

One can improve the performance needed for lower ARs from laser-cut stencils through a means of electro-polishing, nickel-plating, or by stepping up to a 100% electroformed nickel blank. Electro-polishing and nickel-plating help smooth out the jagged aperture sidewalls created in the laser cutting process, but the extra time for these processes can have a negative impact on the delivery time of the stencil. On the other hand, by laser cutting a 100% nickel blank material, you can reach the lowest laser-cut ARs and still obtain the same delivery time as you'd have with a straight laser-cut stencil. Some of the best-performing laser-cut stencils are reaching ARs of 0.48 to 0.50. Again, laser-cut nickel blanks or post-processed laser-cut stencils can vary greatly from one supplier to another.

Speaking of area ratios, even ARs of 0.48 are not low enough for all of today's applications. In those cases, full electroformed stencils are the next step up in capabilities. Electroformed stencils are manufactured through a means of forming a 100% nickel stencil, and in the process, the apertures are formed simultaneously. This gives the smoothest aperture side-wall available. Like all types of stencils, electroforming capabilities and quality varies. The highest performing full electroformed stencils can offer ARs down to 0.42, whereas others might not perform successfully at ARs of 0.49.

> ***One can improve the performance needed for lower ARs from laser-cut stencils through a means of electro-polishing, nickel-plating, or by stepping up to a 100% electroformed nickel blank.***

As the miniaturization of electronics continues, the investment and testing to expand capabilities is in the forefront of many of today's stencil manufacturers. Clearly, many choices are available today for stencils. It becomes a project on its own to know and understand what stencils are required for what applications, all while trying to keep cost to a minimum and maintaining rapid deliveries.

In the coming months, I will continue examining various stencil technologies currently available, as well as coatings, the requirements for step-stencils, and the coupling of the correct blade type with the right stencil.

Do you have a question, comment, or topic you'd like to see discussed in this column? If so, e-mail me. **SMT**

Rachel Short is vice president of sales and marketing at Photo Stencil LLC. As a business school graduate of the University of Colorado, Short immediately stepped into technical sales in the electronics and pneumatics industry. Her last 10 years have been spent providing technical solutions and application support for key companies in the industry. She may be reached via email or 719-304-4224.

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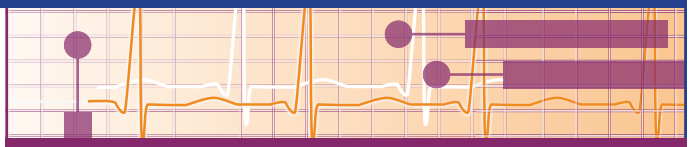

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Mil/Aero007 News Highlights

Hunter Wins Defense Award, Reacquires BBG Fab Facility

Hunter Technology has received an award for significant production quantities for mission critical RF Microwave systems from a major U.S. defense contractor. As a result of this award, Hunter has reacquired the BBG's PCB fabrication facility located in Santa Clara, California.

Probe Acquires EMS Provider Trident Manufacturing

Kam Mahdi, president and CEO of PMI, said, "This acquisition meets several of our long- and short-term strategic objectives, which ultimately reinforce our strategy to provide a low-cost, scalable model for small to mid-size OEMs that allows them to manufacture right here in the U.S. and avoid the myriad of problems and costs now being experienced with offshoring."

Ducommun Adds Baldridge, Churchill to Board of Directors

Ducommun Incorporated's board has appointed Richard A. Baldridge and Gregory S. Churchill as directors of the company, effective immediately, and, accordingly, they will stand for election at the company's annual shareholders' meeting May 1, 2013.

Axiom Earns Recognition from SELEX Elsag

David Davies, managing director of Axiom commented: "We are very honoured to receive this award from a company of Selex Elsag's international standing. Over the last three years we have continued our focus on adding real value to our customers supply chains. This award reflects the success of that focus. We look forward to further developing our relationship with SELEX in delivering innovative and technology driven solutions."

Ellsworth is New U.S. Distributor for Henkel Aerospace

"Ellsworth welcomes the opportunity to utilize our experienced team to market and sell Henkel Aerospace products throughout the United States," stated Mike McCourt, global president - Specialty Chemical Division. "This new distribution agreement allows us to better serve the growing needs of new and existing Ellsworth customers in this specialized industry."

Partnership Formed Between GPV and Danelec Marine

The cooperation between Danelec Marine a/s and GPV dates back to 2005, when the set-up for production of the so-called black box of the sea the Danelec DM400 VDR system, was established. Danelec supplied the PCB designed for the device while GPV designed the mechanics and helped to develop and manufacture the prototype for the system.

OSI Systems Secures $3M Assemblies Contract

OSI Systems, Inc. has announced that OSI Electronics, a business within its Optoelectronic and Manufacturing division, has received orders for approximately $3 million for electronic assemblies from an OEM of defense electronics. OSI Systems CEO Deepak Chopra stated, "OSI is proud to support this new customer with critical hardware to be used in shipboard communication systems."

PartnerTech Boosts Operational and Commercial Focus

To further strengthen competitiveness, PartnerTech is increasing operational and commercial focus by aligning the Electronics and Systems Integration & Enclosures operational areas and by developing supply chain function, covering the company's global sourcing and supply chain activities.

Global Soldier Modernization Market at $892.6M in 2013

"The Global Soldier Modernisation Market, 2013-2023," Visiongain's latest defence and security report, values the market for soldier modernisation spending to reach $892.6 million in 2013 as emerging national markets seek to develop all-encompassing soldier integration projects and mature national markets invest in advanced technology designed to increase operational effectiveness, capability, and flexibility.

Celestica Receives Global EMS Aero & Defense Award

"Celestica's position within the EMS market for Aerospace & Defense has been elevated by its ability to truly understand its customers' unique risks and requirements and help them overcome challenges in their marketplace," said Lavanya Rammohan, Analyst, Frost & Sullivan.

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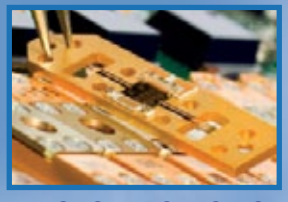

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EVOLUTIONARY SOLUTIONS

Why Reshore?

by Karla Osorno
EE TECHNOLOGIES, INC.

Summary: Bringing manufacturing, and jobs, back to the U.S. significantly impacts the nation's economic future and many industry leaders are taking on this initiative for the benefit of the nation. No matter which side of the fence you're on, there is benefit to considering important factors to ensure end-customer services and cost management.

A Google search on the term "reshoring" or "onshoring" produces 214,000 and 65,700 records, respectively. A "nearshoring" search produces 255,000 records. These terms are the opposite of offshoring which is the relocation by a company of a business process from one country to another. Typically, operational processes, such as manufacturing or supporting processes such as accounting or IT, were the business functions taken offshore. The economic logic was to reduce costs. If some people can use some of their skills more cheaply than others, those people have the comparative advantage.

The major idea was that countries should freely trade the items that cost the least for them to produce. And this seemed to work well until the economic environment changed and companies began to assess total cost rather than just product cost. Reshoring is offshoring that has been brought back onshore—back to the United States or, more broadly, North America. The trend is expected to continue with estimates that by 2014 at least 20% of companies who sent manufacturing offshore will be reshoring manufacturing.

For the United States, bringing manufacturing back, and thus jobs, significantly impacts our economic future. So many industry leaders are taking on this initiative for the benefit of

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WHY RESHORE? *continues*

our nation. No matter which side of the fence you're on, there is benefit to considering these factors to ensure you are able to serve the end-customer by managing costs.

Manufacturers are encouraged to understand and educate customers on the profit/loss impact of both offshoring and reshoring. A great place to start is by visiting www.reshorenow.org to learn the top reasons for companies to reshore:

- Reduces total cost of ownership (TCO);
- Improves quality and consistency of inputs;
- Reduces pipeline and surge inventory impact on just-in-time operations;
- Clusters manufacturing near R&D facilities, enhancing innovation;
- Reduces intellectual property and regulatory compliance risk;
- Eliminates the waste and instability caused by offshoring; and
- Strengthens companies' ability to respond quickly to customers' demands.

The reasons listed are not new. However, factors that have changed to get companies' attention include growing transportation and fuel costs, increased wages in other countries, exchange rate fluctuation, and the inability to provide needed responsiveness. Reshoring resolves these issues allowing many companies to maintain lower inventories, be more cost competitive, deliver products more rapidly, and meet demand for innovation.

A complimentary tool is provided at www.reshorenow.org to evaluate a sourcing decision. With this tool, you can account for all relevant factors of TCO. Here are a few factors to consider in your initial offshoring analysis:

• **Freight on board (FOB) price:** When comparing this level of pricing, the information is incomplete. FOB price ignores many other costs and risks that should be part of a decision. Many companies made decisions to offshore based solely on this price.

• **Packaging:** When shipping long distances packaging is more expensive. Plus there will undoubtedly be times when expediting services from overseas are required to meet customer deliveries. These unexpected and expensive services are often not considered in initial price comparisons and decisions.

• **Duty and freight:** For overseas manufacturing there are significant costs for duty and freight plus related fees. During initial pricing decisions this information is most often not available and when the costs are incurred they may or may not be attributed to the related product/job.

• **Inventory:** When the product takes longer to get to the end-customer, the inventory carrying costs are higher. Big dollars are associated with safety stock to compensate for long lead times and transportation time. Also, based on long lead times for offshore manufacturing, it is possible for companies to have significant inventory that becomes obsolete at the product end of life cycle.

• **Rework/quality:** Costs for incoming inspection, reworking substandard parts or products, and scrapping parts sourced from overseas are significant and seriously affect delivery to end customers.

• **Product liability:** If there are any issues, enforcing product liability in another country will be, at best, difficult and very expensive. Legal and travel fees alone could put many companies out of business.

• **IP risk:** Understand the measures taken to secure intellectual property on products and processes. The potential loss if breaches are made is significant.

• **Impact on innovation:** Separating manufacturing from engineering has a negative impact on innovation. When these two groups work together, improvements are made in product design and in manufacturing efficiencies.

• **Travel:** Many companies fail to include travel costs for sourcing new suppliers, conducting audits, and managing operations in the cost calculations for offshore products.

• **Prototypes:** Prototypes are generally small runs and need quick turn-around so companies choose local suppliers. And when these companies know they will also have production runs the prototype costs are significantly less. Choosing a local supplier for the prototype and production run can impact TCO dramatically. However, if the production is sourced overseas the prototype per unit cost will be significantly higher.

• **Wage inflation and currency appreciation:** Recent information is that wages in China increased 15% in one year. And exchange rate fluctuations can erode any perceived savings in a short period.

Many other costs should be considered, including costs related to language barriers, time zone gaps, communication, and cultural gaps. It is estimated that cost models proposing offshoring underestimated costs by 20 to 30%. This is significant for many, if not all, companies. And this is solely for quantifiable costs and not qualitative costs or consequences of service gaps.

Many other costs should be considered, including costs related to language barriers, time zone gaps, communication, and cultural gaps. It is estimated that cost models proposing offshoring underestimated costs by 20 to 30%. This is significant for many, if not all, companies. And this is solely for quantifiable costs and not qualitative costs or consequences of service gaps.

Reshoring allows companies to essentially eliminate many of the factors that contribute to instability for offshore manufacturing, including weather, port strikes, loss from mishandling, language problems, natural disasters, political instability, and pirates.

Here's an example: An EMS customer made a corporate decision to bring manufacturing back from overseas to North America. Several years ago, this company made a decision to transfer manufacturing of circuit boards overseas. A company in Asia was selected and the products were migrated there. It took a significant amount of time and resources for the migration, including much hand-holding. Subsequent to the migration, it took another nine months of onsite management to ensure products were transformed from raw materials to finished goods. It was certainly not a smooth transition. Issues included significant time differences, incompatible work methods, inability to source raw materials, and an inability to bond inventory to handle fluctuations in demand. Years later, this company is still experiencing the unintended consequences of problems stemming from the overseas transfer of manufacturing operations.

Companies are taking a closer look at the total costs for manufacturing products and making decisions, in many cases, to bring manufacturing back to North America, especially Mexico with its lower cost structure. Mexico plants have seen an increase in production from companies making such decisions. Customers are happy to reduce overall costs and logistic efforts and to have the products manufactured closer to the end-customer and home. **SMT**

Karla Osorno is business development officer for EE Technologies, Inc., an EMS provider delivering complete engineering and manufacturing services with locations in Nevada and Mexico. With education and more than 20 years' experience in finance and operations, Osorno drives completion of projects in marketing, business development, operations, and process improvement. Her passions are to educate and empower others to make changes and a daily difference in the world. Contact Osorno here.

ZULKI'S PCB NUGGETS

Proper Documentation Demands Dummy-Proof Instructions

by Zulki Khan
NEXLOGIC TECHNOLOGIES, INC.

SUMMARY: Why is proper documentation such a big deal? At the beginning of a project, a wide difference in meanings may exist between the OEM customer and manufacturing provider in virtually all aspects of PCB design, fabrication, and assembly. Clear and specific documentation can remove all doubt.

In this day and age, many people use acronyms, slang, abbreviated text, and poor English on social media and even in e-mail business correspondence. That's a red flag for our industry to take a step back and evaluate how we're going about writing PCB design, fabrication, and assembly documentation. In some cases, technical personnel can easily fall victim to, and duplicate the same level of, the type of social media communication they're using and easily transfer it to critical PCB documentation.

Now, at the other extreme, I'm not talking about using the King's English when it comes to defining and writing proper and exact documentation for PCB design, fabrication, and assembly operations. I'm not talking about using big words and fancy language—far from it. I'm saying that words and phrases need to be clearly understandable and to the point without embedding any ambiguity in the documentation.

Why is the proper documentation such a big deal? Here's why in a nutshell: The OEM customer creating the instructions and defining the scope of the work and the contract manufacturer (CM) or EMS provider who manufactures that OEM's product are different in a variety of ways. Those include having a different mindset, different skill sets, different interpretations, and so on.

So, at the outset of a project, it is safe to say that there can be a wide difference in meanings between the OEM customer and manufacturing in virtually all aspects of PCB design, fabrication, and assembly of that OEM product.

Consequently, for the PCB design, fabrication, and assembly house, it is of utmost importance that documentation must be correct and to the point so that it can be well understood. Instructions must be clear-cut, feature no ambiguity, and leave no room for interpretation. Precision must extend to the point where if a certain process cannot be accomplished a second, preferential method must be offered.

When writing the documentation and spec'ing out various aspects of a PCB project, the biggest rule of thumb is to create "dummy-proof" statements and "dumb down" the verbiage so that any reader can clearly understand

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PROPER DOCUMENTATION DEMANDS DUMMY-PROOF INSTRUCTIONS *continues*

it and comes to the desired conclusions. That's the ideal route to take.

More often than not, that's not the way documentation is written. Instructions are left wide open to interpretation, associated drawings are not clear, definitions are not exact, documentation is written to include shortcuts, technicians or engineers don't fully understand some aspect of the project and they guess at it, and, sometimes, sheer laziness or inattention creeps in and inaccurate information is written in the documentation.

Then there's the whole area of vagueness, at which many people excel in when communicating in their personal lives and at work. Being vague simply means not being clear or precise about something or hiding some aspects of the subject you're discussing or writing about. It's like talking about a subject all around its edges, but never really getting to the center of it.

Vagueness when writing documentation allows the verbiage to be left up to interpretation. Therefore, the reader is driven to an inaccurate conclusion and usually the reader relies on the easiest, most convenient method or process to get to that conclusion. The result is a product the OEM doesn't want and the manufacturer or EMS provider is stuck with it.

> ***"Proper documentation for PCB surface finish is critical, as well. Clearly specify the finish. Is it HASL, ENIG, OSP, immersion silver, or hard or soft gold?"***

Fabrication

Let's now examine a few examples in the areas of PCB fabrication, assembly, and box build designs. In a fabrication drawing, a number of callouts can be found: Type of material, thickness and surface finish of the PCB, warpage tolerance, impedance calculations and stack-up information, and IPC Class I, II, or III. When it comes to calling out the material, FR406 or FR408 with a Tg of 170°C or more is specified, for example. But if a specific material is not available, one should not write "or equivalent" because that phrase could be interpreted in different ways by different people. A better approach would be to write, "Either FR406, ISOLA 310 or Rogers 4030." Be specific in terms of what is being defined so that if material #1 is not available, spec out material #2 and include, "No deviation permitted."

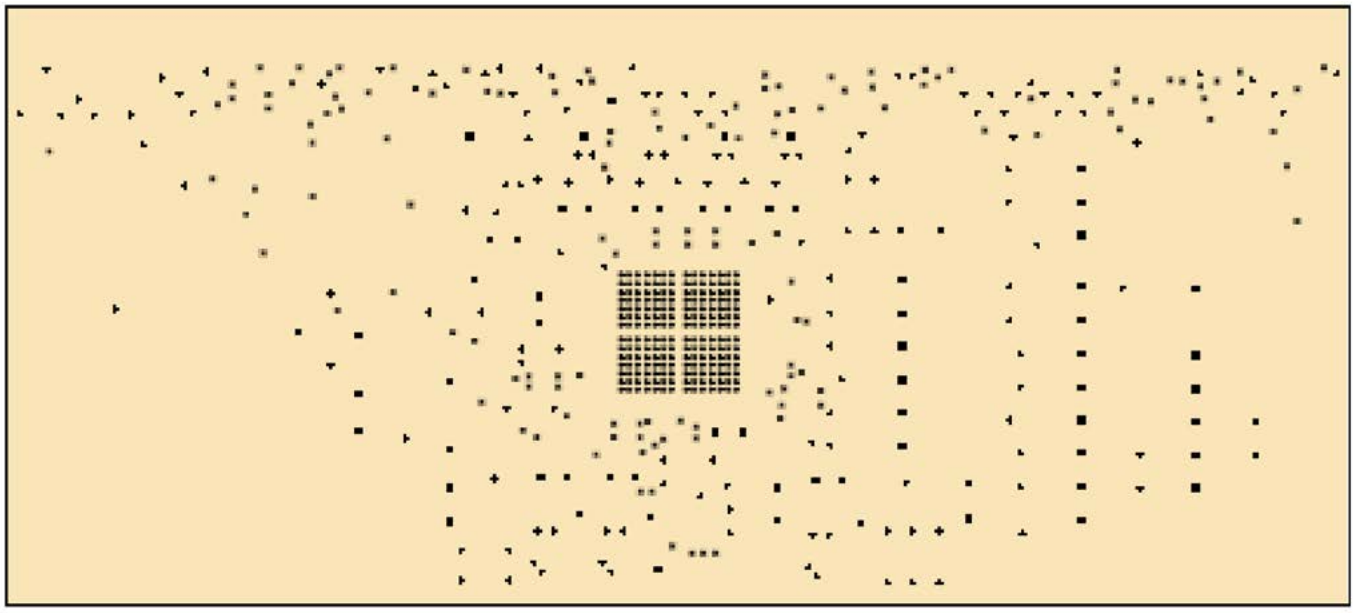
Proper documentation for PCB surface finish is critical, as well. Clearly specify the finish. Is it HASL, ENIG, OSP, immersion silver, or hard or soft gold? When it comes to gold plating, in some cases it's important to specify the deposition of gold per unit area, for instance "30 micro inches of gold per inch."

As for multilayer boards, it's highly important to clearly define the layer stack-up. If a multilayer board has impedance control, the documentation must define if it is a dual stripline or single-ended, the kind of impedance control required on certain traces, and whether the tolerance is 5% or 10% acceptable or more.

Also, the exact drill size with the tolerance must be a critical part of the drill drawing for fabrication (Figure 1). For instance, a 15-mil finished hole size should be clearly defined as to whether it is plated or non-plated with the tolerance being included, for example, +/-2 or +/-0. That comes in handy when it comes to special devices requiring insertion on the board with very tight tolerance requirements.

For example, the call out for a press-fit connector must be very specific; otherwise, if the finished hole is too loose or too tight, the press-fit connector cannot be inserted into the defined holes, creating a rework nightmare. In some cases, such boards must be discarded because the press-fit connectors don't fit because the drill holes are too small.

Meanwhile, via plating is yet another area demanding clear and specific wording. First, this call-out must describe if the via is to be plugged, plated, or plated shut. Then, the call-out should detail the via fill: Whether it is to be conductive via fill, non-conductive, silver, and so on because there are many variations and combinations, hence the need to be specific and ex-



SIZE	QTY	SYM	PLATED	TOL
20	145	+	YES	+/–0.003"
12	135	X	YES	+/–0.003"
41	68	□	YES	+/–0.003"
7.9	196	◇	YES	+/–0.003"

Figure 1: Drill drawing with different sizes, quantities, symbols, and tolerances for the drill holes used in this PCB.

ceedingly clear. Ambiguity results if the call out only states "plate the via" and no explanation is given as to whether it's plated with a mask or silver. This ambiguity leaves the door open for eventual adverse effects for the product.

Assembly

A savvy OEM customer should spell out first-pass SMT operations followed by a second operation of placement to be performed by hand because of moisture or temperature sensitivity, cleaning requirements, or other related factors. If the project comes to an EMS provider as a repeat run, there might be rework or touch-up instructions, like adding notes in the bill of materials (BOM) or assembly drawing for special devices like crystals or LCDs, cutting traces, or putting jumpers, and so on. These engineering change orders (ECOs) must be clearly defined and listed so that there is no room for ambiguity.

An experienced contract manufacturer or EMS company can review the BOM and scrub it to assure that whatever does not have to go through the first-pass SMT process can be held back and can create the manufacturing process instructions or MPI for a second operation. But an inexperienced EMS house might install an LCD using a surface-mount machine and wash it. As a result, the devices are ruined and must be thrown away due to contamination since these devices are especially sensitive to mois-

PROPER DOCUMENTATION DEMANDS DUMMY-PROOF INSTRUCTIONS *continues*

ture and are not hermetically sealed. A more knowledgeable OEM can better define such a process by specifying, "use water soluble" or "no-clean process," and the EMS provider must follow those instructions.

Sometimes OEM customers are overly specific, for example, when performing X-ray or automated optical inspection (AOI), they are particular about such things as sample size. Let's say the EMS provider is producing 500 boards. The OEM customer requests a sample size of 5%. That means that every fifth board undergoes X-ray and AOI. While it doesn't have to be that detailed, however, in some cases that detail comes in handy when a specialized mil/aero or space application board is involved. Moreover, it's particularly beneficial to include in a call out whether or not the board is a RoHS or non-RoHS build since a eutectic build is assembled differently and has a different temperature profile compared to a RoHS build.

If a mil/aero or medical OEM customer is involved, it's vital that boards are built per ISO 9000 or ISO 13485 standards, respectively, because those standards set forth rules and procedures on how to build, inspect, and test the product. If a medical PCB is assembled like a regular commercial board, and not based on ISO 13485, there will be considerable touch-up, rework, and hand-holding at the end—product quality and ship date may be jeopardized.

Controlling revision levels is yet another aspect of proper documentation for fabrication, assembly, and box build. Extremely stringent document control processes are required here. For example, if the call-out is for an E revision, and the product being built only follows Rev C or D, the actual Rev E version will miss special instructions coming after control level D. Consequently, the OEM customer may not accept the product or some rework might be required. To avoid such missteps, savvy EMS companies have assurances of airtight document control procedures, which can release and maintain an effective job throughout the flow with exact specifications and document control levels.

When it comes to flex boards, another set of instructions should come in the picture because flex or flex-rigid boards are a different beast. Not only do the regular aspects of a PCB have to be defined, like material type and thickness, but also associated elements like stiffeners. In the case of stiffeners, shapes, sizes, and tolerances must be specifically defined. If it's a rigid-flex board, the call out must specify how to attach the stiffener onto the board, using what kind of material. Also, the call out must define the amount of bow, twist, and how much bending is allowed.

"When it comes to flex boards, another set of instructions should come in the picture because flex or flex-rigid boards are a different beast. Not only do the regular aspects of a PCB have to be defined, like material type and thickness, but also associated elements like stiffeners."

Document Control for Box Build

Document control takes on special meaning for box build because building a PCB and performing a box build are completely different. Not only are PCBs included in a box build, but there's also a wide assortment of ancillary items like washers, screws, specialized papers, insulators, stand-offs, chassis, power supplies, and special connectors and cables—the list goes on.

So, rather than belaboring the subject, it is best to say that illustrations play a big role. I cannot emphasize enough the importance of step-by-step, color-coded figures and drawings. Combine these with dummy-proof instructions, and the EMS provider has a winning formula for proper documentation.

Then, there are the times the OEM customer isn't satisfied with the first version of their PCB for whatever reason and they want to make changes. That's when the ECO comes into the picture (Figure 2). Sometimes a jumper must be added; a capacitor must be added or removed; a resistor value must be changed; a component

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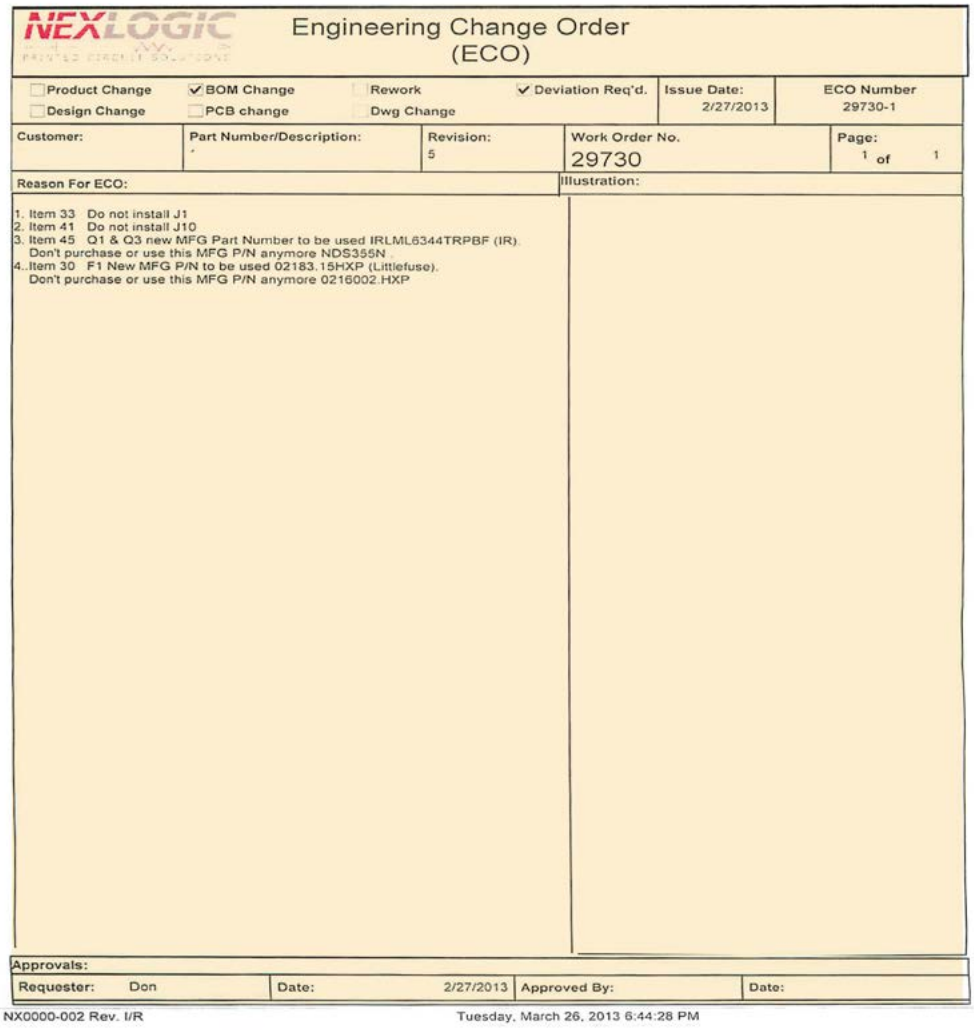

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Engineering Change Order (ECO)

☐ Product Change ☐ Design Change	☑ BOM Change ☐ PCB change	☐ Rework ☐ Dwg Change	☑ Deviation Req'd.	Issue Date: 2/27/2013	ECO Number 29730-1
Customer:	Part Number/Description:	Revision: 5	Work Order No. 29730	Page: 1 of 1	

Reason For ECO:

1. Item 33 Do not install J1
2. Item 41 Do not install J10
3. Item 45 Q1 & Q3 new MFG Part Number to be used IRLML6344TRPBF (IR). Don't purchase or use this MFG P/N anymore NDS355N
4. Item 30 F1 New MFG P/N to be used 02183.15HXP (Littlefuse). Don't purchase or use this MFG P/N anymore 0216002.HXP

Illustration:

Approvals:

Requester: Don	Date: 2/27/2013	Approved By:	Date:

NX0000-002 Rev. I/R Tuesday, March 26, 2013 6:44:28 PM

Figure 2: Example of ECO showing changes that need to be made in the final product, such as changing component, changing value, and other edits, such as cutting traces and adding jumper wires.

must be removed and replaced; and so on. Each and every change must be verified and quality controlled, so it's critical how it is listed and described in the documentation.

Finally, when it's all said and done, meaning the job is complete and shipped, it's a good idea to create and send to the OEM customer a DFM report post job with charts, figures, and drawings. In effect, it shows the OEM the challenges involved in building their product. It also explains the improvements they can perform, as well as parts of the product that are redundant, and the features that are show stoppers.

Also, in that OEM customer report, the EMS company can offer advice as to how they can change the component placements, orientation, or to make changes in the layout so that manufacturing and test are easier and perhaps more cost effective in the future. **SMT**

Zulki Khan is the founder and president of NexLogic Technologies, Inc., in San Jose, California, an ISO 9001:2008-certified company, ISO 13485-certified for manufacturing medical devices and a RoHS-compliant EMS provider. Prior to NexLogic, Khan was general manager for Imagineering, Inc. in Schaumburg, Illinois. He has also worked on high-speed PCB designs with signal integrity analysis. He holds a B.S. in EE from NED University in Karachi, Pakistan, and an M.B.A. from the University of Iowa. He is a frequent author of contributed articles to EMS industry publications.

CALL FOR PAPERS

Abstracts Deadline: 17 June 2013

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Interposer Assembly **Rao Tummala, Georgia Tech PRC**
3D/TSV & Heterogeneous Integration **Juergen Wolf, Fraunhofer IZM**
Power Electronics
Connection Taxonomy **Kyung Wook Paik, KAIST**
Embedded Assembly **Joseph Fjelstad, Verdant Electronics**
Green Electronics Materials & Processes **Tom Forsythe, Kyzen Corp.**
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News Highlights from SMTonline this Month

1 Cherry Named Director of IPC's Validation Business Unit

"The challenging regulatory environment and continued globalization of business practices make supply chain verification more important than ever," says Dave Torp, IPC VP of standards and technology. "With his background, Randy understands the needs of the electronics industry with respect to building trusted relationships within the supply chain."

2 IPC Issues Call for Participation for APEX EXPO 2014

The organization invites researchers, academics, technical experts, and industry leaders to submit abstracts for the IPC APEX EXPO 2014 at the Mandalay Bay Resort and Convention Center in Las Vegas, Nevada. To recognize exceptional achievement, awards will be presented for "Best U.S. Paper" for U.S. authors and "Best International Paper" for authors outside the U.S.

3 Sypris Reports Sales Growth in Q4, Full Year 2012

"Our Industrial Group responded well to the reduction in the production of commercial vehicles during the second half of 2012," said Jeffrey T. Gill, president and CEO. "We now expect the commercial vehicle market to remain stable at current levels in the short-term, as OEMs focus on the introduction of the new model year vehicles and engine technologies early in 2013."

4 Artaflex to Go Private

The company's board of directors has approved a going private transaction to be completed by consolidating the company's common shares on the basis of 1 post-consolidated common share for each 2,500,000 pre-consolidated common shares. The Consolidation is subject to the required shareholder approvals at the company's annual and special meeting of shareholders.

5 Standards Update to Ease Regulatory Compliance

IPC standards committee members recently completed updates on two documents that help the electronics industry keep up with regulatory changes. The revisions will help vendors comply with updates that went into effect at the start of the year and help document programs more efficiently.

6 OnCore Expands Presence with New Tijuana Facility

"We are increasing our existing Tijuana capacity in response to customer demand for a robust, low-cost supply-base that has a short and flexible supply-chain able to service the U.S. market," said Sajjad Malik, president and CEO. The new 88,000 square-foot facility, with the ability to expand to 175,000 square-feet, began volume production in April.

7 Enics to Provide Life Cycle Services to TOMRA

The company has signed an agreement with Tomra Systems ASA, a leading global creator of sensor-based solutions for optimal resource productivity. TOMRA provides cutting-edge solutions for optimal resource productivity in two main business areas: Collection solutions and sorting solutions. Enics was selected to become a global partner for TOMRA.

8 New Bob Willis eBook on PoP Assembly Now Available

Bob Willis has launched his latest eBook, "Package On Package Assembly Inspection & Quality Control," the first textbook covering every step in the process. This is the second publication written by Willis as a free download; his first, "Pin In Hole Intrusive Reflow," has already been read by over 3,000 engineers worldwide.

9 EMS Providers and ODMs Hurt by Cell Phone OEM's Realignment

Outsourced manufacturers previously making strong gains in the cell phone market now face a diminished growth outlook, as mobile communications brands increasingly opt to manufacture smartphones on their own, according to an IHS iSuppli "Global OEM Manufacturing & Design Market Tracker Report" from information and analytics provider IHS.

10 Nypro-Jabil Merger Plan Approved

Nypro's President and CEO Ted Lapres made the announcement, noting, "More than 98% of the outstanding voting shares of Nypro were cast in favor of the merger." Courtney Ryan, Jabil's senior vice president, Global Business Units, who will assume a leadership role in the combined Nypro-Jabil operations, said, "This is an exciting day for Jabil and we are thrilled at the overwhelmingly positive response from Nypro's employee shareholders."

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EVENTS

For the IPC's Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing of events, check out *SMT Magazine's* full events calendar here.

2013 AASRI Conference on Parallel and Distributed Computing and Systems
May 1-2, 2013
Singapore

EDS
May 6-9, 2013
Las Vegas, Nevada

Electronic Circuits World Convention 2013
May 7-9, 2013
Nuremberg, Germany

SEMICON Singapore
May 7-9, 2013
Singapore

IMAPS NE 40th Symposium & Expo
May 7, 2013
Boxborough, Massachusetts

Civil Aviation Manufacturing Conference
May 7-8, 2013
Charlotte, North Carolina

9th Suzhou PCB Show 2013
May 8-10, 2013
Suzhou, China

Japan IT Week
May 8-10, 2013
Tokyo, Japan

International Conference on Soldering & Reliability (ICSR)
May 14-17, 2013
Toronto, Ontario, Canada

SENSOR+TEST 2013
May 14-16, 2013
Nuremberg, Germany

PCIM 2013
May 14-16, 2013
Nuremberg, Germany

2013 International Conference on Materials for Renewable Energy & Environment
May 15-16, 2013
Nanjing, China

2013 Asia-Pacific International Symposium and Exhibition on EMC
May 20-23, 2013
Melbourne, Australia

IPC ESTC
May 20-23, 2013
Las Vegas, Nevada

The Eleventh Annual MEPTEC MEMS Technology Symposium
May 22, 2013
San Jose, California

Electronic Components and Technology Conference (ECTC) 2013
May 28-31, 2013
Las Vegas, Nevada

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INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**
COVER ART: **BRYSON MATTIES AND SHELLY STEIN**

SMT® (Surface Mount Technology) is published by BR Publishing, Inc., PO Box 50, Seaside, OR 97138

May 2013, Volume 28, Number 5 • SMT© (Surface Mount Technology©) is published monthly, by BR Publishing, Inc.

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Next Month in SMT Magazine

The focus of the June issue of *SMT Magazine* is high-reliability mil/aero, medical, and automotive sectors with a focus on standards and specifications; counterfeit components; certification; security, testing, and quality assurance issues; and CAF and SIR concerns.

Expect in-depth articles from the best in the industry: Ed Habtour, U.S. Army Materiel Systems Analysis Activity, and Cholmin Choi, Michael Osterman, and Abhijit Dasgupta, CALCE, present a novel approach to improve reliability in U.S. Army vehicles and Lavanya Rammohan, Frost & Sullivan, explains the EMS provider's role in combatting counterfeit components.

As always, the June issue will also include several columns from our industry experts, including Dr. Jennie Hwang, Zulki Khan, Chris Torrioni, and Karla Osorno.

If you're not yet a subscriber, don't miss out! Click here to receive *SMT Magazine* in your inbox each month.

See you in June!