

SMT

M A G A Z I N E

NOVEMBER 2017

Communication Still
the Best Tool p.12

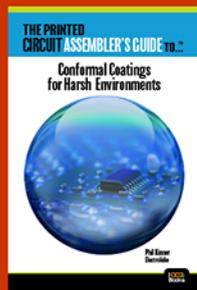
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Communication for Manufacturing Improvement

This month, *SMT Magazine* looks into the issues facing assemblers when dealing with HDI boards, and highlights why close collaboration and communication with the designers right from the very start will ensure assembly success.



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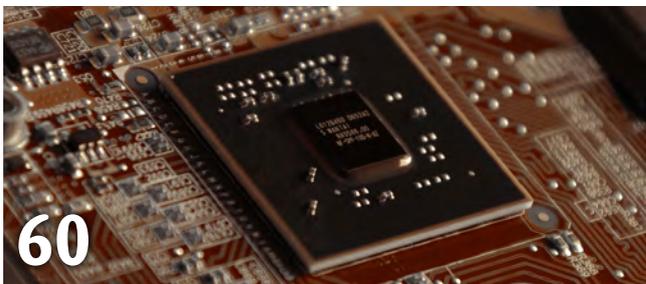
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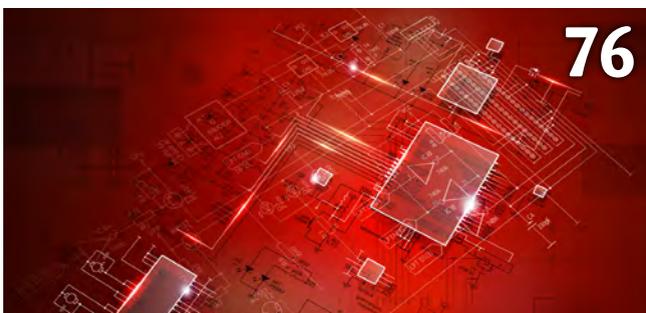
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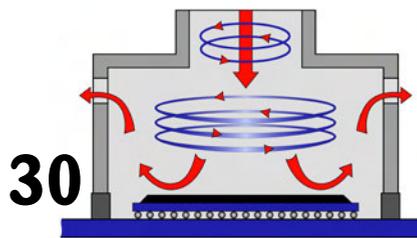
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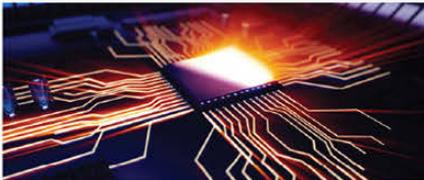
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What Matters Most is Communication

by Stephen Las Marias

I-CONNECT007

There is a growing trend towards the use of HDI in electronics manufacturing. A simple reason is that people want greater performance from their electronics, now more than ever. From an electronics design standpoint, greater performance means more switches or transistors. More transistors mean more power. Counterintuitively, more power requirements of a device means you need to lower the power of the whole system or subassembly. You also need to lower the power because then, you need to deal with thermal management.

To lower the power requirement, everything must be reduced. As such, the components keep getting smaller and smaller. Pin pitches are now down to 0.25 mm or around 10 mil. On top of that, the overall density of board assemblies continuously increases in line with the growing demand for more features and functions. Adding to that challenge is the shrinking PCB real estate on which to put this increasing number of components.

Our recent survey on HDI found that the three key factors driving HDI work are: overall density, fine pitch of components, and the high pin counts of ICs (Chart 1).

At present, majority of our surveyed respondents say up to 25% of PCBs they work with use HDI technology (Chart 2).

In three years, nearly half of the respondents answered that HDI technology will account for at

least 50% of their PCB work. This is across a variety of industries, top three of which are consumer electronics, telecommunications, and automotive electronics. In particular, the emergence of 5G and Internet of Things (IoT) are expected to bolster the use of HDI technology due to frequency and signaling requirements (Chart 3).

Assemblers have different areas of concern regarding HDI than fabricators and designers. When it comes down to having vias in the boards, especially vias in pads, issues will arise if the assembly is the not done properly. "When you put a via in a pad, you typically want to fill that via, with either a non-conductive or conductive epoxy, and use some sort of plating over the barrel of the via so that you get a smooth pad that you are assembling the part to without a whole lot of surface deviation. The flatter the pad, the easier it is to print solder on the board, and to assemble the part," said Garret Maxson of EMS firm ACDi.

This month's issue of *SMT Magazine* examines the challenges when dealing with HDI from an assembly perspective. We start with a roundtable between HDI experts Steve Bird of Finisar, Tony Torres of APCT, and technologists from EMS firm MC Assembly, including Vince Burns, Steve Jervey, Mike Smyth, and Paul Petty. The discussion covers the latest technology developments, manufacturing challenges, and HDI strategies, from the design, fabrication, and assembly perspectives. What we found out is that, while there may be new tech-

Q: What market trends are driving your HDI work?

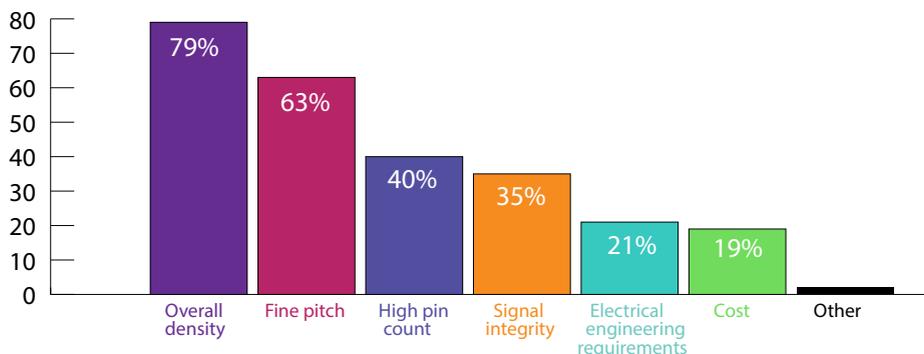


Chart 1.

Source: I-Connect007 Research

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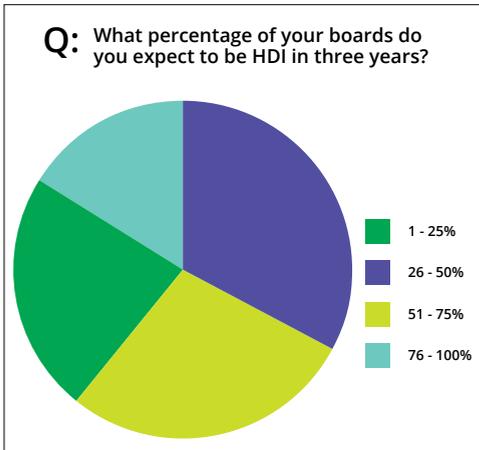


Chart 2: Source: I-Connect007 Research.

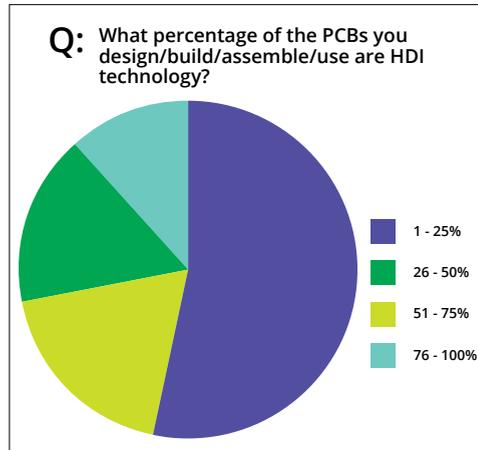


Chart 3: Source: I-Connect007 Research.

niques and strategies, technologies, equipment, tools, and materials to employ and utilize, there is always one thing that will ensure the manufacturing/assembly success of your product: communication.

Communication between the designer and the assembler will help improve the manufacturability and assembly of the final product—even before the board design gets fabricated. As Vince Burns of MC Assembly says, “It’s not just designing the perfect circuit, but it has to be manufacturable, and that’s where our input comes in.”

There is value to be added in collaborating with the designers in the very first stages of the design. Indeed, the goal is working together as a team and sharing the expertise of one another to make sure that the design is manufacturable, and the final product is of high quality and reliable.

We also have an interview with industry veteran Mike Creeden of San Diego PCB Designs, who explains the three perspectives for HDI design and manufacturing success.

Duane Benson of Screaming Circuits, meanwhile, delves into dealing with microvias and via-in-pad.

A technical article from Indium Corporation’s Jonas Sjoberg, Chris Nash, David Sbiroli, and Wisdom Qu, discusses DFX on high-density assemblies.

Another technical article, from Cisco Systems Inc. and Celestica Thailand, tackles via-in-pad plated over design considerations to mitigate solder separation failures.

This month, our resident columnist Tom Borkes of The Jefferson Project explains his take on voiding in solder joints. Bob Wettermann of BEST Inc., on the other hand, compares the two prevalent rework heating methods today, their advantages and disadvantages, and highlighted which among the two is the best process to use.

I was able to interview Dr. Ranko Vujosevic, CEO and CTO of Optimal Electronics, during the recent NEPCON South China event in Shenzhen, China, about the latest technology developments in his company and how he plans to further growth. He shared his ideas on lights-out electronics assembly and the technologies that would support this vision.

Finally, I had a chance to interview Chandran Nair, vice president for Asia Pacific at National Instruments, who explains how Industry 4.0 will revolutionize electronics manufacturing.

We at *SMT Magazine* are looking to expand our roster of columnists and contributing authors. If you have ideas—from industry trends to commentaries to technology developments in the SMT and EMS industries—we’d like to hear from you. Feel free to drop me an [e-mail](#) if you want to contribute to our magazine or online website, [SMT007](#).

Next month, we will focus on solder paste printing (screen printing or stencil printing) and the latest technologies that will help assemblers improve their yield on this front.

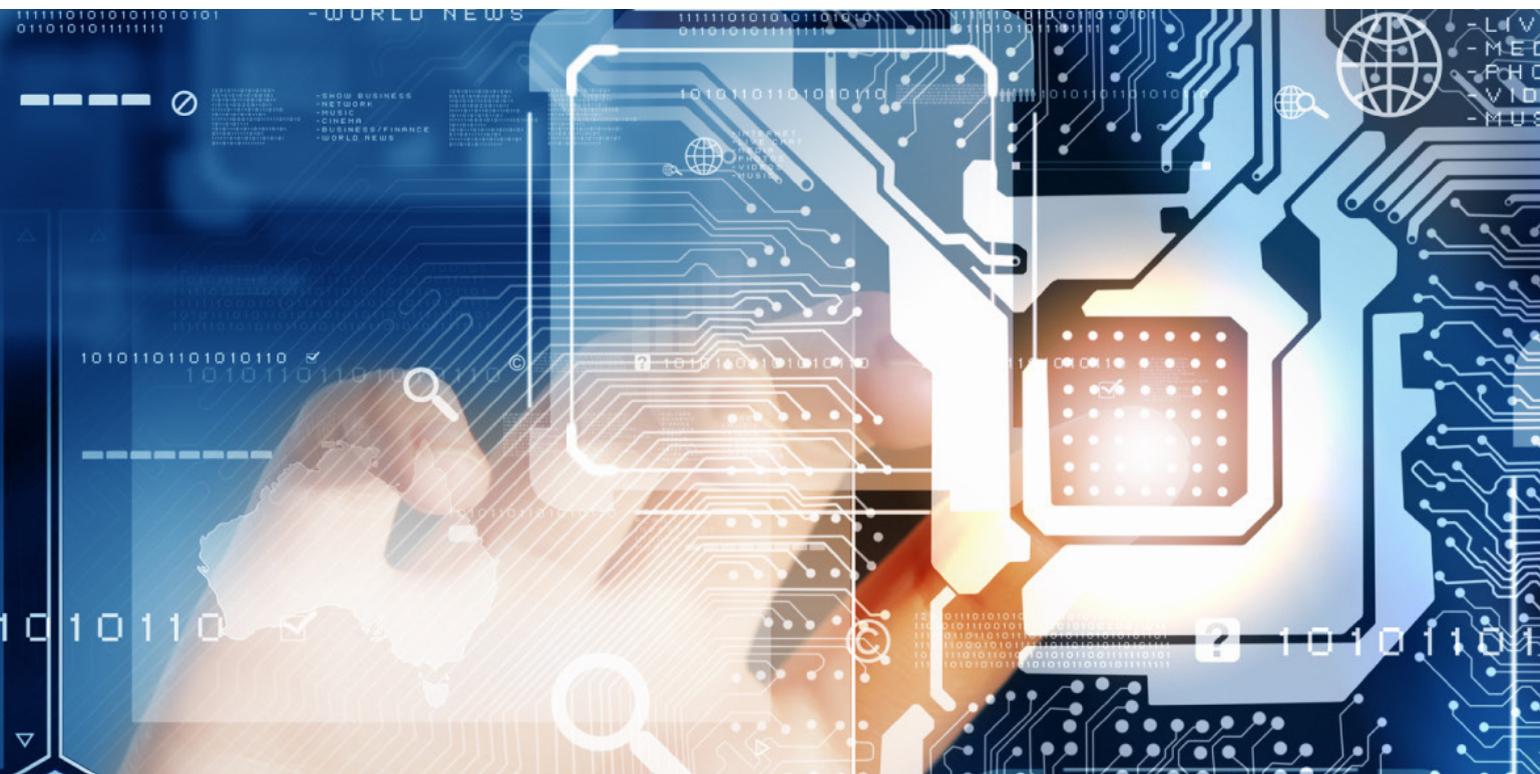
In the meantime, I hope you enjoy reading this issue! **SMT**



Stephen Las Marias is managing editor of *SMT Magazine*. He has been a technology editor for more than 14 years covering electronics, components, and industrial automation systems.

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by **Stephen Las Marias**

I-CONNECT007

For this month's issue of our magazines at I-Connect007, we interviewed some of the top HDI experts in the PCB supply chain to learn more about the latest technology developments, manufacturing challenges, and HDI strategies, from the design, fabrication, and assembly perspectives.

Joining us on the discussion were Steve Bird, PCB/Flex technology manager at Finisar; Tony Torres of APCT; and a group of technologists from the EMS firm MC Assembly: Vince Burns, quality engineer; Steve Jerve, director of Test Engineering; Mike Smyth, SMT engineer; and Paul Petty, product engineer. They all gave their expert insights, and provided tips and tricks as well key parameters that you should consider when it comes to dealing with HDI.

Despite the latest technologies, equipment and tools in design, fabrication and assembly, we found out that there is one very important factor that will determine the success or failure of your HDI assembly: communication. Com-

munication between the PCB assemblers, designers and fabricators will always guarantee the improvement of your design, process and products.

Increasing Adoption of HDI

There has been an increasing growth in the use of HDI boards in electronics manufacturing.

"It's unbelievable," said Torres. "Just two short years ago, in 2015, we were doing 20% HDI work. Our facility in Santa Clara now does 85–90% HDI work. We're a company whose mantra is to be able to say yes to the customer's needs, in technology and in delivery. We were forced to really learn how to build HDI work because that was their very first question: Can you build this product? Then they want to know how fast we can get it to them."

The growth is mainly driven by market demand, amid the continuing miniaturization trend in electronics, in addition to the need for more functionality and higher performance. According to Torres, the single-sided, double-sided and multilayer boards markets were all flat. "HDI technology was the only growth model,"



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he says. "Over the last three-year period, flex circuits and rigid-flex had a little bit of growth, but as far as percentage of the business, it was very, very low. The bulk of the business was HDI and so the writing on the wall was clear. That's why we made the shift in equipment and in up-front engineering, and it's paid off."

Does HDI technology lower the cost of boards? "It is a mixed bag," explains Torres. "Generally speaking, moving to HDI technology and keeping layer count down will ultimately wind up with a lower cost for our customer. However, there are times that, with standard through-hole technology and lower layer counts, simply adding two more layers may be more cost-effective than moving to an HDI design."

Material Matters

Besides the lines and spaces, annular ring, and holes to fill with copper, one the important issues that Torres's team review is the materials to be used. "I was very interested in listening to the discussion on what's coming. The first thing that we have to do in order to satisfy customer needs is to come through with quality and high-reliability product. So, we give a lot of feedback about what materials to use. We would be very, very open in that conversation," he explains. "If a customer has the design already in hand and wants us to use a certain type of material, if we think that the design will be better and go through easier with a different type of material, we'll certainly suggest that. We have partnered with different material suppliers and we often go out with our sales force, with our supply partner at our shoulder, and start the design discussion of HDI work with material. It's very important that the materials work for both the OEM and the PCB manufacturer. That's pretty critical."

Finisar's Bird wears two hats: one for being the technical lead for the EEs and the CAD designers at the company, and the second for leading their organic substrate roadmapping and development.

"Maybe 18 months or two years ago,



Steve Bird

we were working with a fabricator. We started cheating on the FR-4 design rules, and to their credit they built over 1,500 of these over a period of a year or so, and finally gave it up, and they said 'No bid.' Of course, the upper management team came to my group saying, 'You're violating the design rules.' And I said, 'Yes, but not without an engineer sitting next to the CAD designer. What we have here really is not a design rule violation, but a technology limitation," explains Bird. "That spun off an effort to find a substrate that could support the design rules that we're cheating to. Our PCB technology team was tasked with the effort. We got one new substrate developed and released, but now those new design rules are being violated; we have to continue development. For that previous generation, once we got off of FR-4 and onto alternate materials, we were still in the subtractive process. Now, we're looking very heavily at the semi-additive process. Our trace with normal FR-4 is going from 4 mil trace and space down to say, 3.5 mil, roughly, and that's what earned us the no-bid. Now, we're at 2 mil trace and 3 mil space, and that's still not good enough. So, we're continuing to increase the density, and for us, our whole game is no vias, no stubs, and no parasitics. Everything's predictable, no glass weave, etc., and so what we're looking at is thinner and thinner laminate, and hybrid stack-ups. We can certainly do all of our power delivery and control signal distribution on FR-4 layers, but what lies on that surface is really important to us. We can do small modules, system-type modules for our ICs and such, our chip-on-board and so on, but really what we need is a full system-level surface layer that can support those types of densities and mount chips. That's what we are working towards right now."

The Assemblers' Perspective

"We're listening to the designer and the fabricator talk about getting layers thinner and smaller," says Burns of MC Assembly. "But one

of the things that we're all discussing here is the temperature cycles. Just starting out, everything that we build here has to go through a reflow oven. It has to go through a reflow profile. We have to melt the solder so that we can get the parts to stick to the board, so the thinner the layers and material get, the more we're concerned about the adhesion of the layers, of the copper to the substrate, and the internal adhesion of the substrate layers.

"What I've seen in the past with boards that aren't HDI is you'll get issues with moisture in the boards and then you'll get issues with delamination as we run through the reflow process at the surface metal level and also at the wave solder and through-hole level. And that's not even mentioning the rework. Unfortunately, the way that the systems work is they go through the reflow or the SMT process, and parts don't always go where you want them to go, and so you end up with rework. When we rework these things, now we're applying a 700°F soldering iron to a pad and you're more likely to have that glue that's holding the boards together come apart on you, so a big concern that we have are our thermal profiles and how these things are going to stick together. Another concern is that the smaller these parts get, the more difficult it gets for us to put solder paste on the board and have things that we can see, like the bottom side underneath the BGA. When things flow in there, we have to look at it with X-ray. If we're talking about micro BGAs, we don't have a whole lot of clearance for the solder to reflow and hopefully not bridge."

To address those issues, Petty says they are starting to use a lot more nanocoating on their stencils, and they are focusing on different designs. "Instead of typical round BGA pads, we're doing the square with the rounded corners, and we have to have carriers. A lot of the times, we're running boards through the reflow oven or an exterior that gives it more rigidity. It goes through reflow so you don't have any warping of the board, which can also damage it."

"We also have an inline SPI, which we are definitely checking," says Smyth.

Is jetting the solution for the solder paste in this application? "It's something that we can definitely look at," says Smyth. "We do not have that capability at this time. We have looked at different equipment that could do that, but right now what we do is we rely on our SPI a lot. That monitors our height, volume, size. It keeps all the pads in check so that we can ensure that everything is meeting spec. I was also going to say we're sometimes constrained by our customers on which solders we can use. We have a variety of tin-lead solders and we have the RoHS-compliant solders, so we'll have a variety of the SAC solders and some others. For one customer, we use a low-temperature solder that has a high bismuth content, so we've got a huge variety of solders. Some of our customers don't allow high- or even medium-activity fluxes. We have to use ROL0 fluxes, which again creates other additional issues.

Testing

One of the problems HDI has is limited access for in-circuit tests. Are there solutions to help people that use HDI in terms of being able to use it for assemblies?

"That's a big concern of ours," says Jervey. "As a contract manufacturer, our in-circuit test traditionally has been a big part of our test solution. Over the last couple of years, I see that dying out very quickly. Our response to that in the immediate mode was to transition a lot of our work into flying probe with very small-pitch flying probe leads down to 3 mils on the point of the probe. We're doing a lot of flying probe work. The obvious extension to a physical test is to utilize boundary scans where we're capable of using vector-

less type tests or physical access isn't there to test things. It's going to be a challenge. As things get smaller and smaller, ultimately you have to touch it somewhere to test it in some fashion and it's a challenge every day."



Mike Smyth

Communication: Still the Best Tool in the Book

In any manufacturing environment, communication between the supplier, manufacturer, and customer is key to production success. In the PCB supply chain, it is no different, especially when dealing with HDI boards.

According to Burns, in his more than 12 years in the electronics contract manufacturing industry, there's only one company that came to them to talk actively about the design of the board prior to them bringing it for manufacturing. "That was an interesting journey. It ended up working really well," he says. "They went through a lot of iterations of the board design before we finally got one that would work, but the vast majority come to us with a product and say, 'Here, we're ready for you to start building this.'"

Burns notes that they have to convince customers that there's value to be added in collaborating with them in the very first stages of the design. "It's not just designing the perfect circuit, but it has to be manufacturable, and that's where our input comes in," Burns says.

"If I could put in my two cents from a fab standpoint, I would have the same comments as most everyone else: Suppliers very rarely get involved early," says Torres. "If I can be so bold, I see it as a comment on business in general that everybody is just concerned with their own responsibility, their own expertise. You've got to start acting like partners, not only with suppliers, but with your internal customers as well. If that designer understood the cost problems of the purchasing department, one phone call to the fab manufacturer before the design is completed could save a lot of time and money. If you design something for manufacturability, it's going to be more cost-effective for their

company, and obviously if you go one step further and design for automation, that's even better.

"I think the companies that embrace teamwork in all facets are going to win. When you start talking about the designers, do they know that the prototype is going to go into big production? In some cases, they do; but if they had a system to always call the fab house to have that relationship, why not call the assembly house and get all of the feedback before the design is completely made? Then you have a winner in all facets and you're not chasing your tail after the fact. You're saving time and money upfront. The goal is to work together as a team and share our expertise with one another. I think the niche in the market-

place is not to simply take the Gerber files and build it, but to really be a partner to the end-customer. Be a help to them and talk out the design and get something that is not only reliable, but manufacturable."

"I've been in this industry since '79, and the things that we care about now are so different from the things we cared about then," says Bird. "For instance, who cared about the height of a trace or a trapezoidal shape back then? Now we're trying to squeeze gaps down, and all of a sudden we get this metallic bathtub where we are hitting the spacing limits because we can't etch out the gaps cleanly. We use ENEPIG a lot. But now we're getting to a point where nickel, the thickest metal in the stack, is too lossy. It just goes against our density and performance goals. Therefore, we are going to be evaluating EPIG, actually more accurately EPAG (electroless palladium/autocatalytic gold). We're looking at metal thicknesses and trace features that I never thought we would see during my career. Also, as PCB technologists, we have to be willing to go out and scour the globe, not just within our approved vendor database,



Vince Burns



Steve Jervey

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for what's up to date, and then next year do it again and then do it again, because things are changing so quickly. The best thing we can deliver to the engineering community? Put together a package that is properly vetted, that you know is stable, all of the delamination and via micro-cracking, etc., address all of the reasons that people say why we shouldn't do it (challenge all paradigms). This means that we have to have DOEs going continually to make sure that we didn't just jump off the cliff. I'm always jumping off the cliff. You really need to own it, and owning it is doing the look-aheads that you talked about—talk to your assembler, talk to your fabricator, and talk to the guy on the plating line. Talk to the guy who's running the laser drill. So, this position two years ago did not exist and it does now, and the reason was because we were failing some of our substrates. Now, with proper vetting in place, we can explore just about anything that makes sense to us, as long as we qualify it before production. At this advanced level, PCB and flex technology roadmapping, PCB reliability, and the DFM process cannot be separated.”



Paul Petty

Burns concludes, “One of the best comments I've heard today was just more communication and better communication up front.

For the design and the fab end of it, the readers should consider contacting not just the OEMs but some EMS manufacturing facilities and ask them up front what their capabilities are. If we go smaller and smaller, what do we need to do as an industry to be able to manufacture things at that level? This also goes to the component manufacturers because now we're also looking at components that have to be mounted on these boards. We need the designers and the fab guys to understand the conditions that these boards are going to go through when they get to our end and a lot of it is heat. We're concerned about the number of heat cycles we can run a board through, and how we can keep from damaging things as we go through the heat cycles. From the material aspect, we need to make sure that the materials are robust enough to withstand the things that we're going to put them through at our end.” **SMT**

Joining Forces: SMTA and the SMART Group in Europe

At the recent SMTA International 2017 event in Rosemont, Illinois, I-Connect007 Managing Editor Patty Goldman sat down with Tanya Martin, SMTA



Keith Bryant



Tanya Martin

executive director, and Keith Bryant, global director of sales for YXLON International and Chairman of the SMART Group to discuss current events within the association, and to learn more about their upcoming merger.

They talked about the rationale behind this partnership, and their upcoming event, branded under SMTA Europe and titled “Electronics in Harsh Environments,” to be held in Amsterdam on April 2018.

[Read the full interview here.](#)

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Libra Industries Expands Design Team

EMS provider Libra Industries has expanded its design team with the hiring of Alan Vannasy as a Senior PCB Designer.

Fabrinet Names Seamus Grady Chief Executive Officer

Fabrinet has appointed Seamus Grady as chief executive officer and a member of Fabrinet's Board of Directors.

Huizenga Amendment on Conflict Minerals Approved by the U.S. House of Representatives

The U.S. House of Representatives has adopted an amendment by Rep. Bill Huizenga (R-MI) that would prohibit the use of funds for any action on rules issued by the U.S. Securities and Exchange Commission related to conflict minerals.

Sanmina Surpasses 25,000 Pieces of Manufacturing Equipment Connected in the Cloud

Sanmina Corp. has reached the milestone of connecting more than 25,000 pieces of manufacturing equipment to the 42Q cloud solution.

Cirtronics Chosen as Tour Site by The Association for Manufacturing Excellence

Cirtronics has been chosen as a featured tour site by The Association for Manufacturing Excellence (AME), for the recent AME International Conference in Boston, Massachusetts.

Celestica Honors Avnet with Best Aerospace and Defense Partner Award

Avnet has been awarded a 2016 Total Cost of Ownership (TCOO) Supplier Award from Celestica.

Syrma Technology Receives Top Prize for Quality at ELCINA-EFY Group Awards

Syrma Technology has received the First Prize for Quality in the SME category at the annual ELCINA-EFY Group Awards, at a gala presentation at The Lalit Hotel in New Delhi, India.

Jabil Posts Strong Q4 & FY 2017 Results

Jabil Inc. has reported preliminary, unaudited financial results for its fourth quarter and full fiscal year ended August 31, 2017, including fourth quarter net revenue of \$5 billion and fiscal year net revenue of \$19.1 billion.

ACDi to Exhibit at PCB Carolina 2017

EMS provider ACDi will be exhibiting at the PCB Carolina show to be held November 8, 2017 at the McKimmon Center in Raleigh, North Carolina.

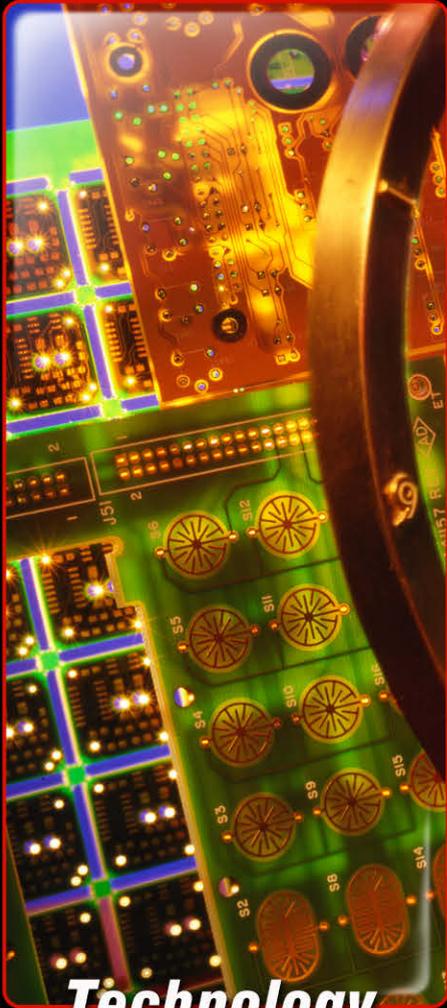
Microart Boosts Capabilities with Two More High-Speed Lines

Microart Services Inc., a contract manufacturer located in Ontario, Canada, has strengthened its capabilities by adding two more high-speed lines.

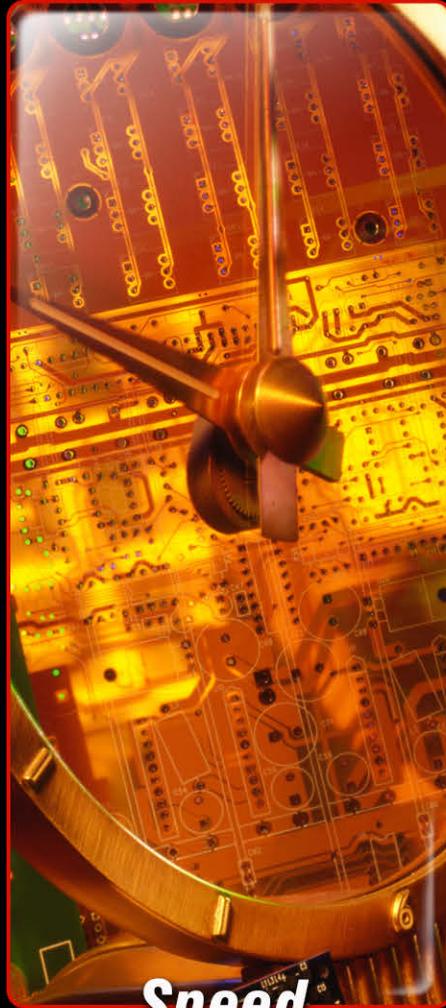


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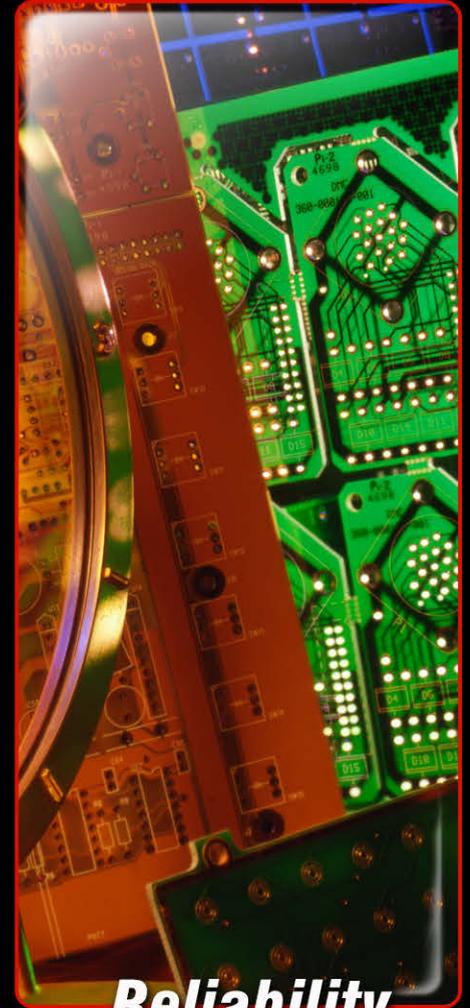
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Three Perspectives on HDI Design and Manufacturing Success

by Andy Shaughnessy, Happy Holden, and Stephen Las Marias

I-CONNECT007

Mike Creeden has been in the PCB design industry for more than 40 years. In June 2003, he founded San Diego PCB Inc., a design bureau serving a variety of industries, including industrial, automotive electronics, medical diagnostics, defense, aerospace, and communications markets. The company was acquired by EMS firm Milwaukee Electronics in November of 2016. Currently, Creeden is the vice president of layout services for San Diego PCB Design LLC, which has about 18 designers and supports four CAD platforms. He is also a master instructor at EPTAC, where he teaches CID+ certification classes across the country.

San Diego PCB has designed a variety of HDI circuit boards over the years. So, for this month's issue of our magazines, we interviewed Creeden to get his insights on the challenges when it comes to HDI and how designers and manufacturers can address those issues.

Typically, HDI can improve the performance

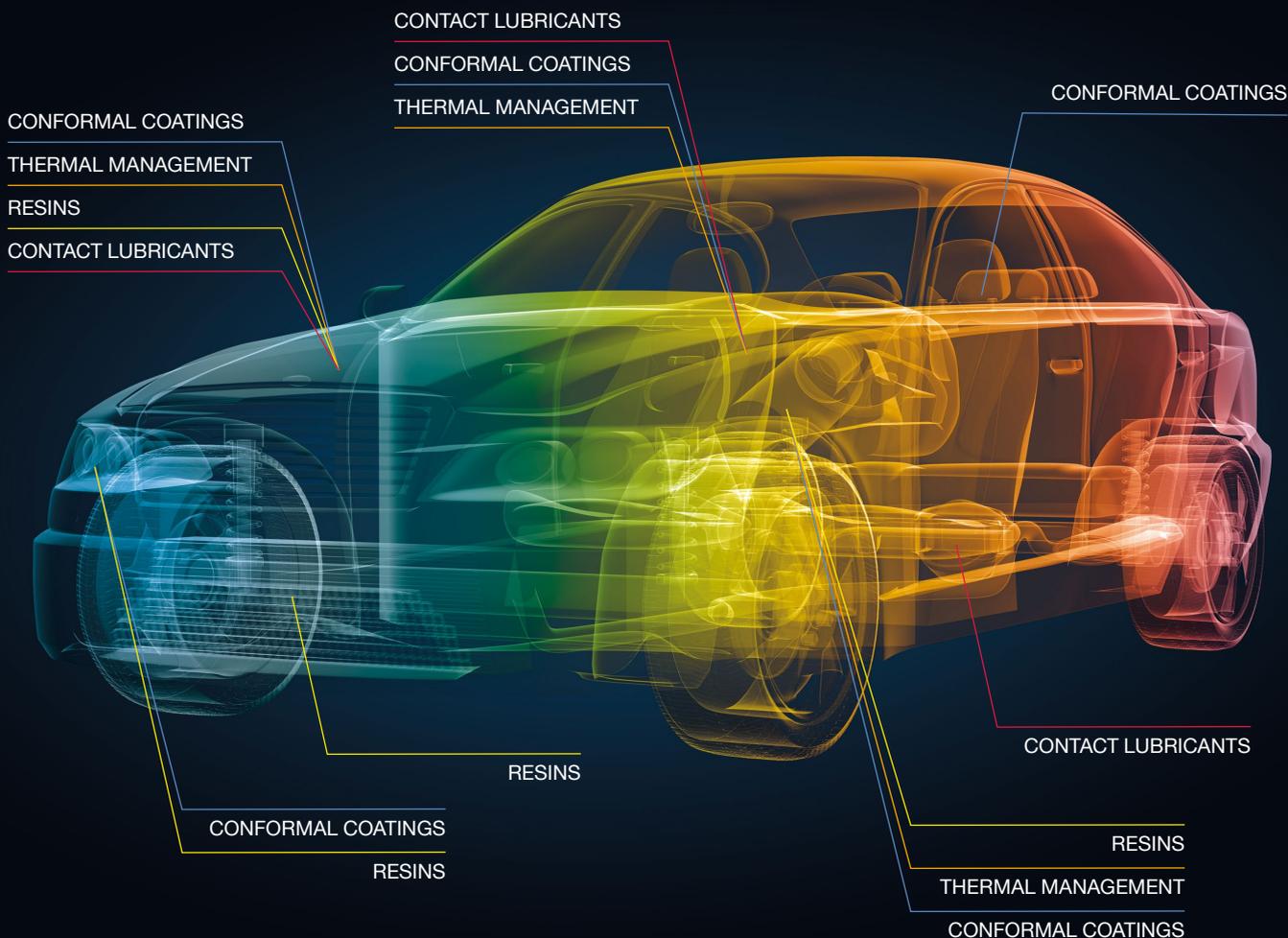


for dense, high-speed signals. HDI may have little or no effect on design cycle time. However, HDI is usually a cost adder to the fabrication cycle, with some exceptions, such as layer reduction. Most HDI issues are negligible to the PCB assembly process.

"HDI, along with almost any aspect of PCB design layout, in my opinion, should consider three perspectives for success: layout solvability, whereby oftentimes there's a complex packaging challenge involving dense BGAs or fine-pitched BGAs that need pin-escapes; electrical integrity—including all signal and power integrity considerations; and DFX manufacturability," explains Creeden. "A designer must approach HDI and any portion of PCB design layout with all three of those perspectives in mind.

"The solvability is a skillset that a designer would have to essentially understand and be competent to truly satisfy the placement and connectivity of the board with their CAD tool. HDI exists in many different forms. For example, via-in-pad. It would require half the geometry to pin-escape a board if you can put the via right in the pad. Therefore, you must consider

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Figure 1: Per IPC-2200 series: three perspectives for PCB design layout success.

the manufacturability of that because now, you have potentially a via filling and a planarization and a plating aspect. From an electrical integrity standpoint, when doing via-in-pad, you essentially are reducing some of the parasitics, by having an extra piece of metal there to perhaps impede or affect the circuitry. Via-in-pad is a form of HDI. We're seeing BGA pin counts routinely now in the 1,500 to 2,000 range; there are some BGAs that are way beyond that, but many are in that neighborhood. With the dense pin-count of the BGA, it presents a challenge to supply power, pin-escape and completing all the routes while maintaining electrical performance. It really becomes a geometric solve whereby you may seek to utilize—even if the pin pitch is 1.0 mm—an HDI solution to pin-escape in the dense board without adding extra layers. Sometimes, you cannot add so many layers in a standard board thickness, therefore HDI is a solution to increasing layer count. However, designers must be careful because they must always respect high-speed issues, such as the return path, whereby the electromagnetic (EM) field is resident in the dielectric material between a signal and GND and a voltage and GND. You must be observant that it's not just the physical pin-escape; you must consider the electrical integrity. And again, if you are using

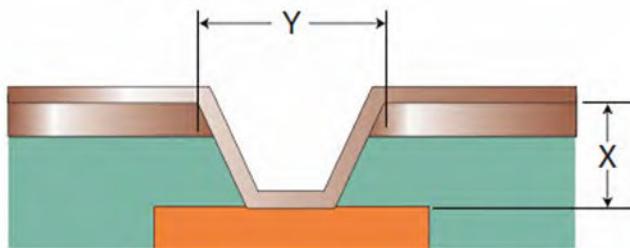


Figure 2: IPC 2221, microvia aspect ratio.

HDI, you've brought many extra process steps to the fabricator, such as considerations of FR-4 material and plating issues, to name a few."

Microvias

According to IPC 2221, a microvia has an aspect ratio of 1:1 or less. For example, with a 4-mil dielectric, you would have a 4-mil drill diameter. Creeden points out, "The reliability of microvias is high. And the reason it's high, when done right, is because of this low-aspect ratio. The plating is typically more robust and there's less chances for a coefficient of thermal expansion (CTE) mismatch, so the HDI laser via is robust, in my opinion. In design layout of finer pitch uBGAs, you can't fit a normal size via within the ball pattern and you can't pin-escape because on the surface, it is very difficult to pin-escape between two uBGA balls because you have to utilize a very thin trace. When you start considering the outer layer plating, it's difficult for the fabricator to produce a reliable thin trace on the outer surface. It's just not a robust manufacturable feature, especially if you're attempting to maintain a consistent impedance. So, you will typically have to use HDI microvias when you get into the 0.65 mm, 0.5 mm, and smaller pin-pitch uBGAs. Oftentimes, you might save money if you can find a similar functioning device and can live with a larger package size with the larger pin pitch."

Because microvias can only go down one or two levels at a time, they can be very good on signal integrity, or from a power delivery standpoint, according to Creeden. "If you have a very thin dielectric, even a buried capacitance material in layers two and three, it's very good power delivery to just tap down one to two layers to get a very low impedance delivery of your planar capacitance. To that end, it's very helpful for power delivery."

Creeden says that planar capacitance lends itself very well to HDI. "I am seeing that more on boards for mil/aerospace, as well as commercial boards with wall-to-wall components, which have BGAs on both sides of the board, and there's no room for decoupling capacitors. So, using buried planar capacitance is growing in acceptance within the industry. It is an incredibly thin dielectric, and it's a cost adder—

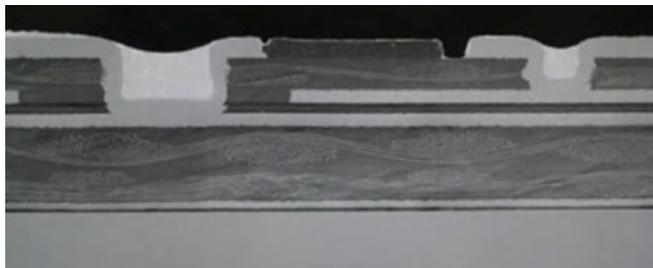


Figure 3: Example of HDI microvias accessing buried planar capacitance layers for robust power delivery.

don't kid yourselves. But it has very good performance. When you have no room for decoupling capacitors, then you may be forced to use it. Or if you work for someone like NASA or the military—maybe you're not as cost-sensitive—I recommend people consider it because it works well with HDI and improves performance."

However, there are sometimes tradeoffs when it comes to pin escape and power delivery. And therein lies the challenge brought by the number of pins in the BGA. "Whenever possible, in HDI, if you can bring your connectivity underground (layer 2), and I mean under 0.0V GND, you have EMI containment. Thus, it is easier to pass any kind of FCC or emissions testing that your product may encounter. Whenever a signal is encapsulated by ground layers, with adjacent return paths, you have good containment of its EM field, so they'll perform better, and you'll reduce noise emissions and susceptibility."

While there is a lot of signal integrity tools that try to help designers detect EMI noise, Creeden says he always encourages layout designers to "make the EMC correct by construction and not create noise, rather than detect it."

"Another caveat that I would always recommend from a manufacturing standpoint when dealing with microvias is the concept of stacked or staggered vias. It's a methodology by which when you're utilizing microvias to traverse multiple layers, you may stack them on top of each other or stagger them, offsetting them so they're not on top of one another. When you stack a laser via on top of a laser via, they will typically end up metal-filling that. It's okay because they have a thin dielectric, and there's less stress on

the via. But what you should never do is stack them on top of what's known as the "N" or the internal mechanical drilled via, because it is always best if the mechanical drilled via is non-conductive resin filled. There are thermal expansion issues at play that create via failures. You'd see that if you look at a lot of microsections; you can see that the non-conductive fill actually retracts a little bit because it has a thermal shield being inside the via wall. So, if you stack vias on top of it, essentially you have a much greater potential of having an open via failure.

"Typically, the limit of how many microvias can be stacked is a consideration of the number of lamination heat cycles the FR-4 material can withstand, and that number is debatably about four to five. I'm sure higher-end shops may be exceeding this at some point, but the limit is the material. Other methods of stacking vias on every layer is utilized in the telecom for tablets and cell phones that are typically thin boards. This method has been called by names like: full-stack-vias, every-layer-vias, or any-layer-via. They utilize a CU-sintered conductive paste as opposed to conventional plating methods. To this end, always keep an eye out for new methods coming around the bend."

While laser-drilled vias are reliable, they still present a lot of fabrication challenges. "Understanding some of the manufacturing process that your fabricator has to work with, I always encourage people that if you want to design a stack-up, the fabricator needs to weigh in. You don't create a stack-up, then route your board, and then after that, ask for the fabricator for a DFM review. You truly need to theorize your stack-up and all the feature sizes that you need for the layout solvability, such as pin-escapes, smallest features, and overall routing completion; you must ensure that you satisfy the electrical integrity such as impedance and implementing proper EM theory. Then, get your DFM review at the start of layout to make sure this can be built. You do not ask those questions after you routed the board. I repeat: Ask those questions at the start of the design. Considering manufacturability, it's much more of a fabrication issue than it is an assembly issue. Fabricators will provide conformance certificates, and

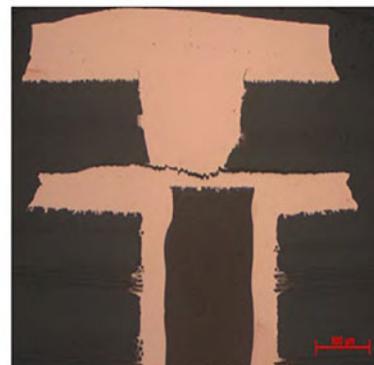
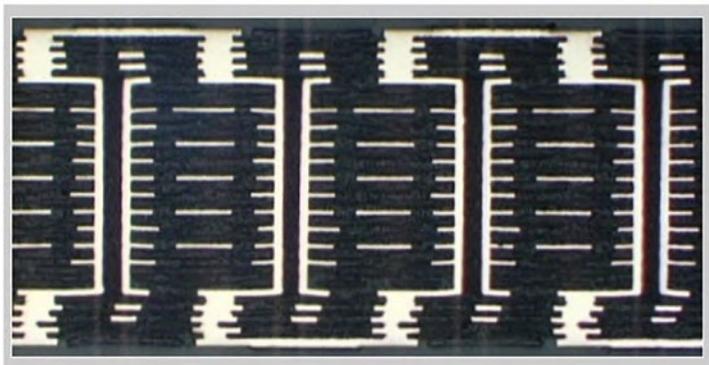


Figure 4: Never stack microvias on resin-filled vias.

they do a lot of testing; IST and HATS testing, are a couple of methods. However, if it's done on a coupon, you always have to ask if that coupon truly reflects the circuit as it's laid out. These designers can theorize the stack-up, but if they violate it, with the way they actually did the design, the coupons are really not representative. An asymmetrical stack-up is a good example of this occurrence, whereby the designer routes signals broadside coupled and not asymmetrical. The amount of cycles by which you test these vias in coupons—some people say 250 cycles at a certain temperature and some reports actually suggest 500 cycles—a person who wants to rely on these different testing methods should really investigate them to see where the sweet spot is, and if that fits with their budget and margin.”

Designers have always been asked to estimate the scope of schedule, performance probability and then provide technical feasibility for cost estimates and planning. On this, Creeden says, “I must do an estimation of this design; and typically, I can tell you early on if it's feasible and the scope. The first thing I want when estimating the scope is placement feasibility and assembly profile. I consider the placements of components to see if I can fit these components on the space provided—I do a component dispersant, where I just dump them all out on a board; at this point I don't care about the circuit flow—I just want to see wall-to-wall if I can put parts on the board. Because if I can, I could always do a via-in-pad, and I can go underground and solve the routing. The second thing I need to look at is the smallest pin pitch

of the BGA. This will dictate if any sort of via grid is required. If microvias are required, now I have taken myself into an HDI scenario. Finally, when you look at a large BGA, you often-times see how many signal pins that need to pin-escape. The amount of signal pins that may need to pin-escape a large BGA may constrain how many layers will go into a stack-up. Third, I will collaborate with my production fabricator to ensure complete high-yield buildability. With these three things, I can typically give you an estimation for feasibility at the beginning of the layout phase. Designers need to talk to their full development team and complete supply chain before they go and layout the boards. It's all about being proactive, not reactive.”

Testing Issues

Every circuit has different testing requirements or desires, depending on customer requirements, production plan, or end use. Several methods for testing in the should be given careful consideration depending on what best suits your situation. Different testing methodologies have varied strength and weaknesses.

“From a layout perspective JTAG testing can be one of the simplest to implement,” says Creeden. “Some companies would like to have ICT. It's expensive, but way more definitive as to the condition of the manufactured board. But you need full nodal access with ICT fixtures. When I have BGA pins that use microvias such as blind and buried, you do not have accessibility unless you can breach it to the outer surface. Then you might be violating the electrical integrity. And more than like-

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ly, if you are using the small-pin package, you don't have room for that. I design boards that have thousands of nets that would need to come out to the outer surface and often there is no room. HDI does not lend itself well to that. With these high-density challenges testing companies tend to go more into functional test or JTAG."

Assembly Front

HDI concerns are primarily a fabrication concern. However, one of the biggest issues when it comes to assembly is component placement feasibility, according to Creeden. "A via-in-pad, even if it's a through-hole via, is a form of HDI. Therefore, it's high-density from a placement perspective because now I can fit all the parts on the board with good DFA considerations. Because I can put a via in its pad, I can route that board. Assemblers typically don't know what it takes to route a board. They don't know what's internal. They see the outer layer—and that's mostly what the assembler will consider. Typically, what the assemblers would care about is the assembly profile. The assembler has three agents: the bare board, the components, and the bonding agent of solder. As-

semblers want to ensure that land pattern provides a robust solder connection to match the component, especially getting a good solder connection underneath any BGA," he explains.

"That's critical to them. One of the concerns they are seeing now is package types known as landless grid arrays (LGA), which are like BGA but without elevated solder balls on each contact pin. I see this utilized with a lot of power supply devices. The problem, because of its coplanar mating, they cannot disperse the solder flux residue, causing it to form a barrier on the edge of the device. It's not a normal perception of an HDI issue, but when you're talking about 100 amps coming from a power-supply device, that's a high-density power issue. People have this way of thinking that HDI means only microvias; now I put to you that HDI can be something with larger features such as a landless low-profile part, which may become an HDI assembly concern. So, what a good designer might do is to add vent holes in between the pins of the landless grid arrays so they can outgas the flux residue."

HDI is here to stay, and there are three key perspectives of concern: layout solvability for the geometry and density, the electrical integrity, and the manufacturability. **SMT**

Research Yields Significant Thermoelectric Performance

Scientists at the U.S. Department of Energy's National Renewable Energy Laboratory (NREL) have reported significant advances in the thermoelectric performance of organic semiconductors based on carbon nanotube thin films that could be integrated into fabrics to convert waste heat into electricity or serve as a small power source.

The research demonstrates significant potential for semiconducting single-walled carbon nanotubes (SWCNTs) as the primary material for efficient thermoelectric generators. The discovery is outlined in the new *Energy & Environmental Science* paper, "Large n- and p-type thermoelectric power factors from doped semiconducting single-walled carbon nanotube thin films".

Advantages of this research include the promise of solution-processed semiconductors that

are lightweight and flexible and inexpensive to manufacture. According to the researchers, the introduction of SWCNT into fabrics could serve an important function for "wearable" personal electronics. By capturing body heat and converting it into electricity, the semiconductor could power portable electronics or sensors embedded in clothing.

The paper was authored by Jeffrey Blackburn and Andrew Ferguson, both senior scientists in NREL's Chemical and Materials Science and Technology center. Other NREL authors are Bradley MacLeod, Rachele Ihly, Zbyslaw Owczarczyk, and Katherine Hurst. The NREL authors also teamed with collaborators from the University of Denver and partners at International Thermodyne Inc.



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Two Prevalent Rework Heating Methods—Which One is Best?

by Bob Wettermann
BEST INC.

Using IR Rework

There are two prevalent heating technologies in use throughout most electronic assembly operations for advanced component rework. The first method employs the use of hot air gas to heat up the component through the package—this may or may not include the injection of nitrogen. A second much-used heating technology relies on infrared energy. This electromagnetic radiation, safe to the operators, is absorbed by the package, thereby sending the solder into reflow.

Hot Air Rework

A typical hot air rework system employs a heat source and an air source that forces the heated air through a nozzle (Figure 1) configured to the area of interest, which heats up the component to be reworked. There are numerous levels of such a hot

air system, including a completely manual, a semi-automatic, and an automatic system, each with its own features.

Why Hot Air?

Hot air convection heating for PCB rework is advantageous for a variety of reasons. The absorption of heat by the component and circuit board is independent of a material's color or texture. Additionally, inducing nitrogen to the site during component reflow has the advantage of making sure the metallurgical structure of the solder joint is the most reliable. In air-atmosphere rework, an oxide layer forms around the solder sphere as it reflows. Inducing nitrogen during this step displaces the oxygen and limits the oxide layer forming around the molten solder. Finally, a hot air convection system quickly delivers heat energy into thermally massive boards.

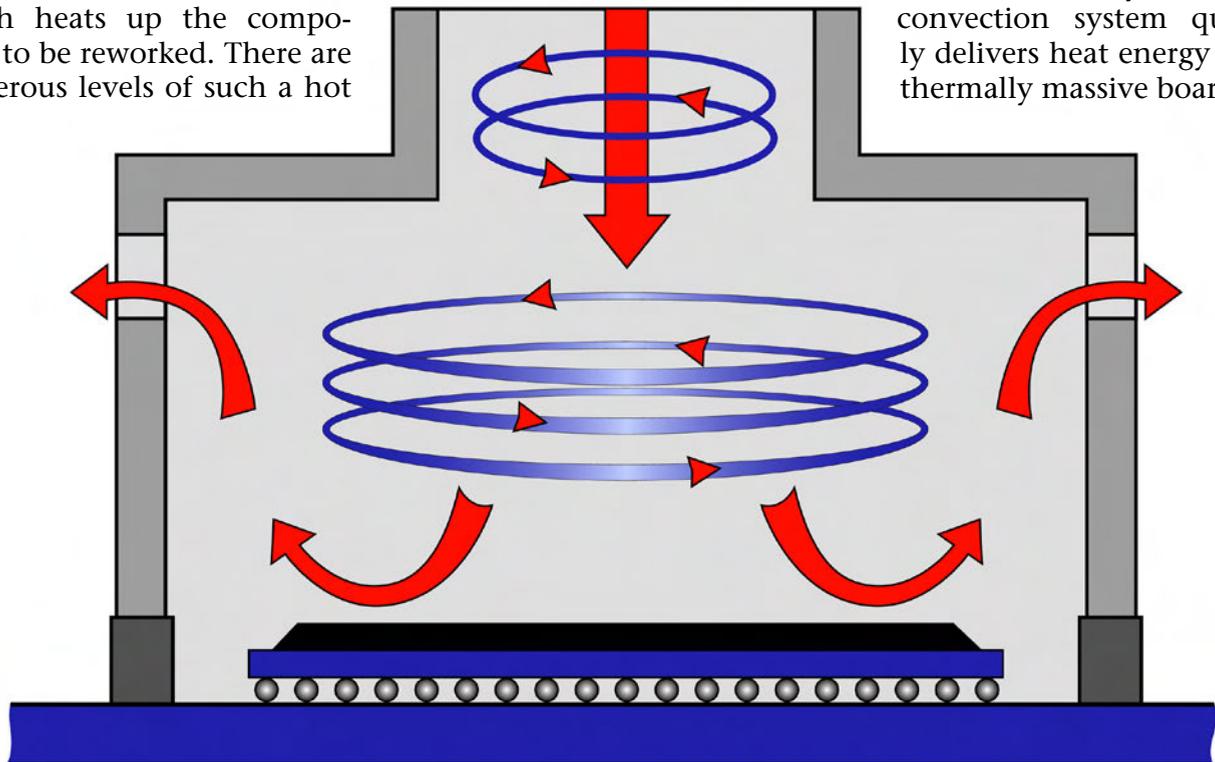


Figure 1: Nozzle delivers hot air in and around the package during rework cycle.

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While there are many advantages to using a hot air rework system, there are some drawbacks the user needs to be aware of when trying to decide which reflow source to use. First, due to the nature of the hot air source and the ever-decreasing mass of SMT components, solder joints can be disturbed or parts can be skewed during reflow. This is especially true for 0201, μ BGA and other micro packages. Secondly, to make sure the hot air blows effectively on the package and not onto the neighboring components, a customized nozzle is required. Too large a gap between the edge of the package and the nozzle and then the neighboring parts will tend to go in to reflow. A poorly-designed nozzle leaves a temperature gradient in the hot air source thereby leading to inconsistent results. In addition, customized nozzles take several weeks to fabricate and are not cost-effective for small quantities. Finally, in many cases the peak temperature will be higher for a hot air profile versus that of a similar IR reflow profile. This may cause parts in the neighboring vicinity to those being reworked to reach their softening point (like plastic-bodied relays and connectors), thereby causing damage to them.

What is IR?

Infrared (IR) technology, the other widely-used heating source for PCB rework, was

first introduced into SMT repair equipment in mid-1980s. An infrared heater is a body transferring energy to a body with a lower temperature through electromagnetic radiation in the infrared spectrum with wavelengths from 780 nm to 1 mm. There are two basic styles of IR technology. The first is medium range IR (Figure 2), which emits the energy and is “blocked” from some areas of the PCB by “shuttering.” The second is a focused IR heat source (Figure 3) in which IR radiation is collimated and directed through a lens system.

Advantage of IR

The IR heating source presents some advantages to the PCB rework process. It is important to realize how passive and gentle the method is and, in fact, at full power the heating effect is so slight that you can hold your hand in the beam for some considerable time before any effect is felt. This makes the technology advantageous for applications where heat-sensitive components found in rework may not be damaged.

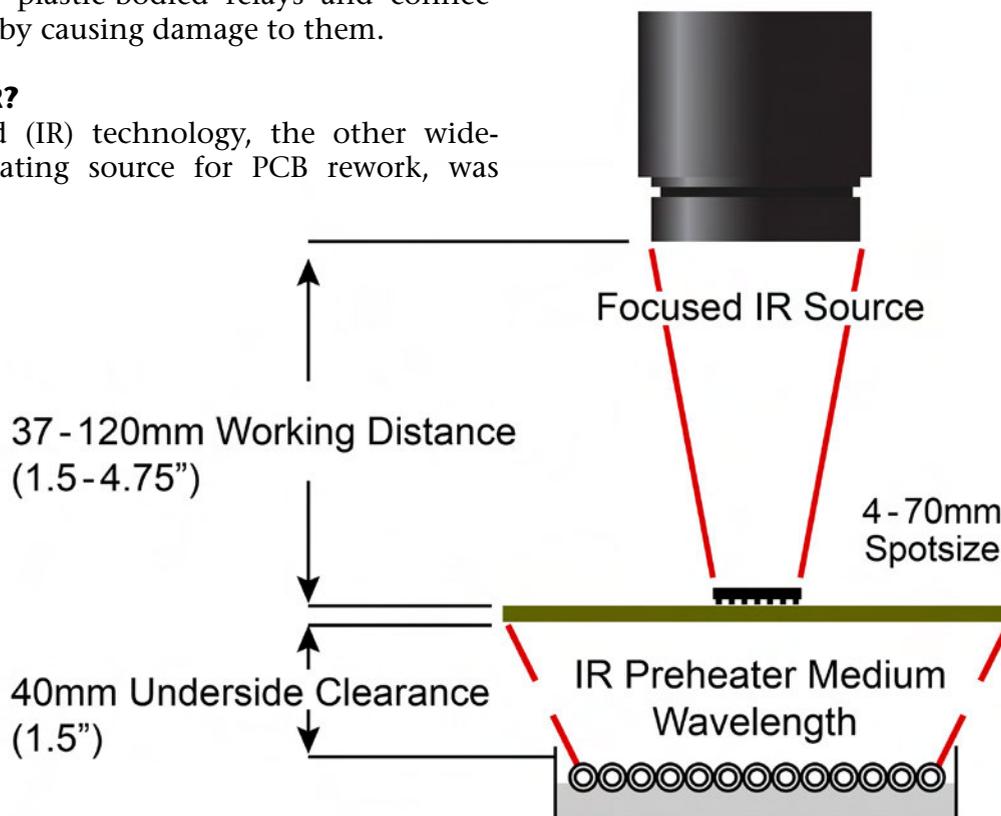


Figure 2: Medium IR heating technology for PCB rework.



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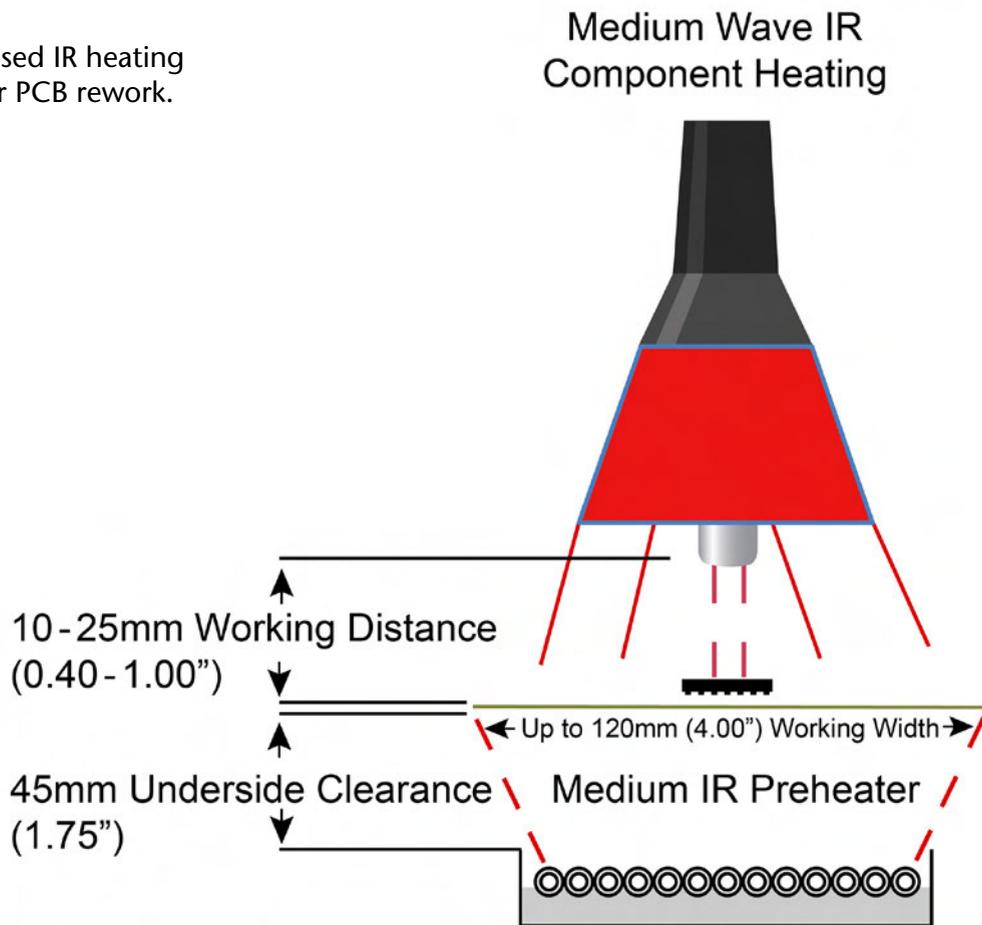
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Figure 3: Focused IR heating technology for PCB rework.



IR systems measure temperature empirically at the PCB or component, whereas hot air systems measure hot air temperature near the hot air exit source. This makes for a more-exacting profile based on achieved component temperature. In addition, IR heat sources require little tooling for specific BGA sizes. Another advantage is the ability to easily take in-process temperature data of the IC for each reflow operation. However, the primary advantage to the IR heating is the ability to not disturb very small components as no turbulent air flow exists along with the heating source.

While the infrared heating source has some distinct benefits over the hot air systems, it too has some shortcomings as a reflow source for BGA rework. There are still some underpowered IR heaters on the market which means that the rework process cycle time is much longer than a properly-designed nozzle and hot air system. This means that for very large boards such as servers, backplanes and other high current-carrying PCBs, the IR heat source may not be suf-

ficient. The user needs to be aware that IR systems using medium wavelength IR resulting in darker-colored components have a different absorption of heat energy than light-colored components. In some cases, this means that the user must employ an ESD-safe black tape to make sure the component heats up to the right heat energy levels. Process control can be difficult with infrared heating as the absorbency spectrum and therefore reproducibility from component to component and board to board results can be an issue.

Both hot air and IR heat sources have their place in PCB rework with specific choices of rework heat source dependent upon the application at hand. **SMT**



Bob Wettermann is the principal of contract rework and repair firm BEST Inc.



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DFx on High-Density Assemblies

**by Jonas Sjoberg, Chris Nash,
David Sbiroli, and Wisdom Qu**
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There are many ways to increase packaging density. Examples of technologies include fine-pitch connectors, package-on-package (PoP), fine pitch CSPs, 01005, 0201, and reduced component-to-component spacing.

Use of new technologies poses a number of challenges for solder paste selection, PCB design, assembly process, and reliability. The type of end product will have different challenges, concerns, and requirements in all aspects. The assembly line for many of these end products will look very similar, but specification limits would be different. Typical reliability tests are drop test, vibration, thermal cycling test (TCT), and SIR; even if the names of the tests are the same, the pass/fail criteria vary between different end products.

When it comes to material selection—and solder paste in particular—the type of end product plays a big role. An automotive, computing server, or router product would, in many cases, require an in-circuit test (ICT); thereby, the

solder paste residues must be easy to penetrate with a test probe. A consumer product, on the other hand, typically doesn't focus on ICT. The concern is more on throughput, thereby requiring a solder paste that is capable of fast screen printing. There are many more examples, but with the increased need for high-density assembly, most, if not all, solder pastes must be able to print well on stencil apertures with area ratios (AR) way below the typical industry standard of 0.66. The AR for some products could be as low as 0.5-.55.

With the above challenges, finer solder powder is increasingly being used, and the type of solder powder is moving from type 3 towards type 4-4.5, and even type 5 for a number of applications. This poses some new challenges. In addition, low-silver and low-temperature alloys are gaining traction, making the selection of solder pastes and alloys more complex.

Once the correct solder paste material is selected, a feasible and robust assembly process must be developed and sustained. The assembly process ranges from screen-printing, placement, and reflow soldering in air or nitrogen to electrical and functional testing. Many factors

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influence the quality of the assembly process. With the reduced pitch and component spacing, the capabilities for solder paste, assembly, and PCB fabrication will be tested to its limits and beyond, with the need for using statistical tools is becoming a requirement to develop and maintain good yields.

Even with the right solder paste selection, good assembly process, and high-quality PCB and components, failures still will occur, leading to yield losses and extra cost. Once these failures occur, it is very easy to jump to conclusions and start making changes without knowing the root cause of the failure. As engineers, we quite often tend to look for the most difficult solution, but in many cases, the simple solution is the right solution to solve the issue.

PCB and PCBA Design

When moving to high-density assembly, it is very important to understand PCB design and its limitations. With increasing density, the PCB fabrication becomes much more challenging. Some of the key PCB design requirements include:

- 50 μm copper/copper spacing (inner and outer layers)
- 50 μm solder mask slivers
- 25-40 μm solder mask registration tolerance
- 60 μm microvias
- 200 μm microvia capture pads in outer and inner layers

Understanding DfX and design is in many cases critical to be able to identify the root cause of the issues that occur on the production line. When it comes to PCB and PCBA design, there are many important aspects. In this paper, we have selected a few that have a critical impact on SPI and overall yields.

- PCB stretch and shrink
- Filled vs. unfilled microvias
- Silkscreen

PCB Stretch and Shrink

The maximum PCB stretch is 0.05 mm over the entire panel, and this must be clearly speci-



Figure 1: Typical PCBA panel layout for consumer products. It is important to ensure that the overall stretch/shrink tolerance is no more than 0.05 mm.

fied on the PCB fabrication drawing. This is very important for fine-pitch parts and high-density spacing products. The pads and apertures for 01005 passives and 0.3 mm pitch CSPs is 0.2 mm; a stretch or shrink of more than 0.05 mm leads to solder paste that will be 25% of the pad.

Microvia Issue

Excessive voids in some cases lead to solder bridging. This could be caused by oversized or “leaking” microvias in pad in combination with normal process variations. An issue on a smartphone can be seen below; failure rate for bridging was 6% in this case (Figure 2).

One primary issue today is that there are no clear specifications as to how big the microvias are allowed to be or where to measure the actual size of the microvia (Figure 4). Since there is no

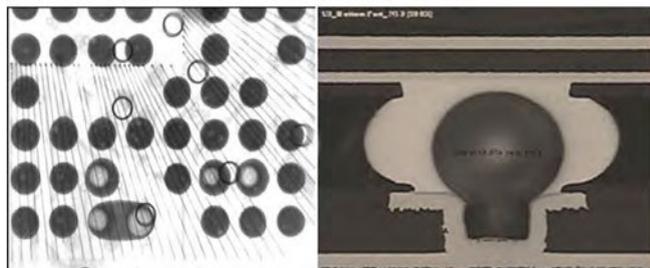


Figure 2: Solder bridge and excessive voids on a 0.4 mm pitch CSP due to microvia size issues.

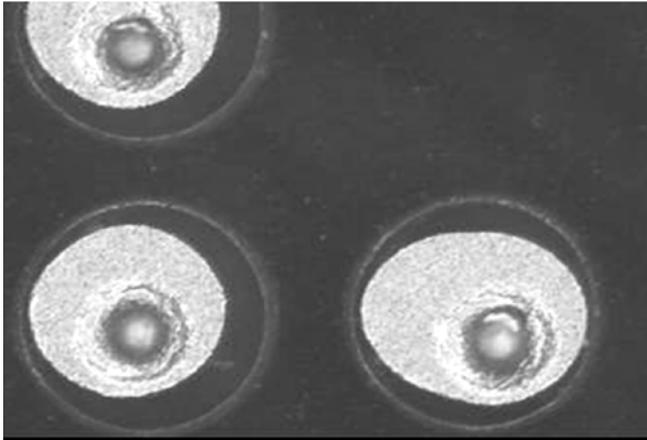


Figure 3: Typical unfilled microvia from top.

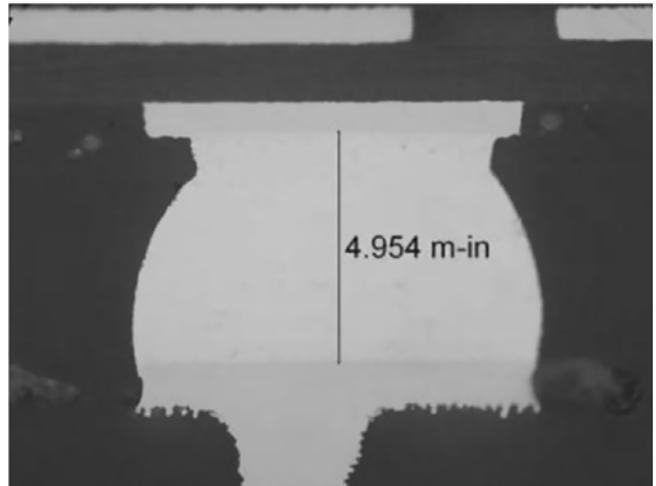


Figure 5: Bridge and void issue solved on a 0.4 mm pitch CSP by using a copper-filled microvia.

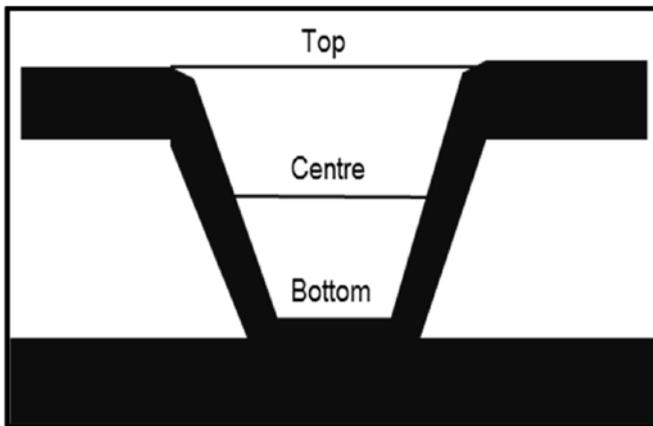


Figure 4. No clear specification if the microvia should be measured top, center, or bottom.

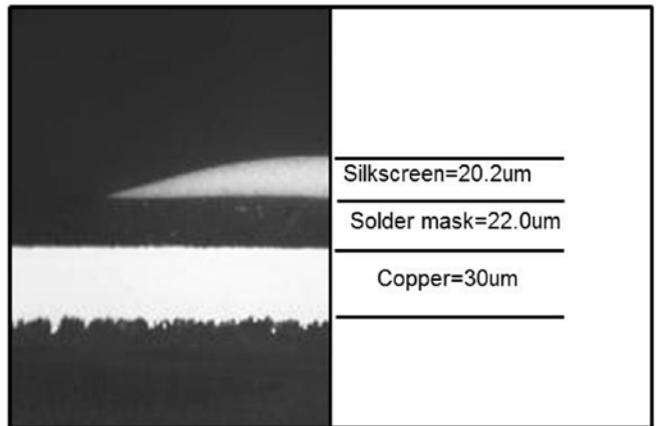


Figure 6: PCB silkscreen on top of solder mask and copper.

clear specification, the microvias can look different in size and shape between different suppliers and between batches of PCBs.

By filling the microvias with copper in the PCB fabrication process, the voids and bridging issues can be eliminated (Figure 5).

Silkscreen Issue

Depending on the quality of the silkscreen, the height on top of the solder mask could range from 15-40 μm (Figure 6). This can create a gap between the stencil and PCB of 15-40 μm , depending on the PCB design. The gap can create printing issues leading to both too little or too much solder paste height and volume. Depending on the design of a product, the solder mask can add 10-25 μm in addition to the silk-

screen, creating a gap of 15-65 μm from the bottom of the stencil to the pad.

In this case, the top of the solder mask is 422 μm on top of the copper pad.

When the stencil is placed on top of the PCB, the effect of the silkscreen becomes very visible graphically (Figure 7). By looking at the SPI data (Figures 8 and 9), it becomes very clear that it can have a big impact on SPI yields, and potentially overall yields.

Silkscreen is normally not needed on today's products and is an extra cost of approximately $\approx \$0.01/\text{square-inch}$. There is also a risk that parts of the silkscreen are placed onto the pads.

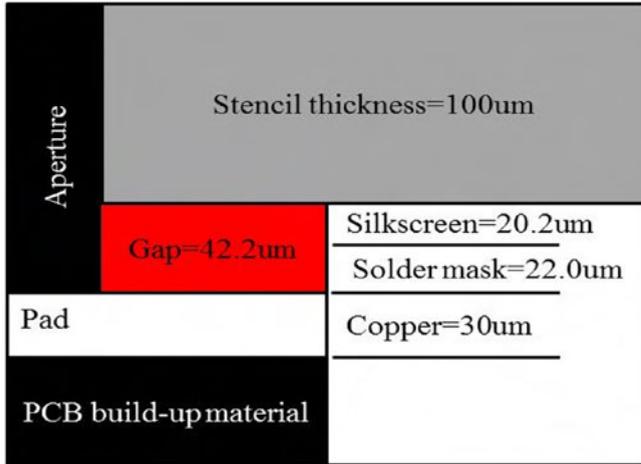


Figure 7: PCB silkscreen stack-up with stencil.

Copper markings should be used in the outer layers if the design can accommodate this. This applies to CSPs and other parts that have a critical placement tolerance. The effect of silkscreen on SPI performance can clearly be seen in Figure 8 and Figure 9.

Solder Paste and Alloy Selection

Today, the most common solder paste alloy is SAC 305 (Sn96.5/Ag3/Cu0.5) for high-densi-

ty assembly technologies. When increased thermal cycling performance is required, a higher silver-content alloy such as SAC 387 (Sn95.5/Ag3.8/Cu0.7) is typically used. However, using a higher silver (Ag) content alloy will increase price and could have a negative impact on mechanical reliability.

Before making the solder paste selection it is important to evaluate key material properties such as:

- Printability
- Voiding
- Cold and hot slump
- Solder balling and solder beading
- Wetting
- HIP resistance/oxidization barrier
- SIR (surface insulation resistance)

The selection of powder size varies between type 3, type 4, type 4.5, and type 5 (Table 1). With the correct flux formulation, a more expensive type 5 powder can in many cases be avoided but still meet an acceptable Cpk of 1.67 (Table 2). Besides a cost increase, type 5 powder also increases the risk of HIP and graping due to an increased surface area and oxide content.

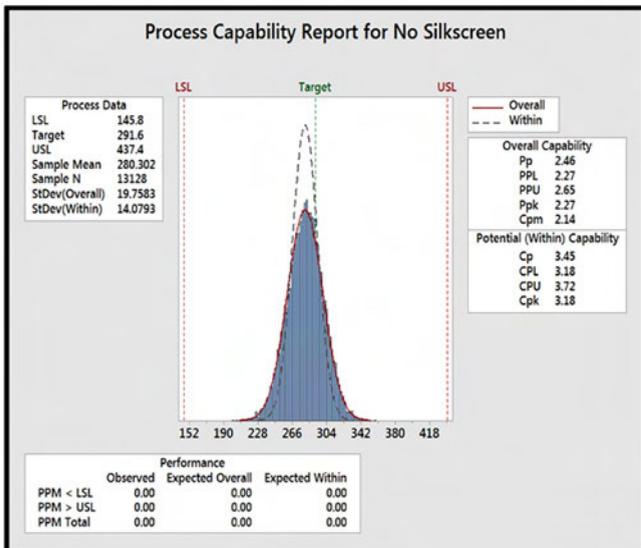


Figure 8: Process capability graph on a 0.4 mm pitch CSP without silkscreen on the PCB. Volume (mil³) specification limit is 50-150%. The mean value is very well-aligned to the target volume.

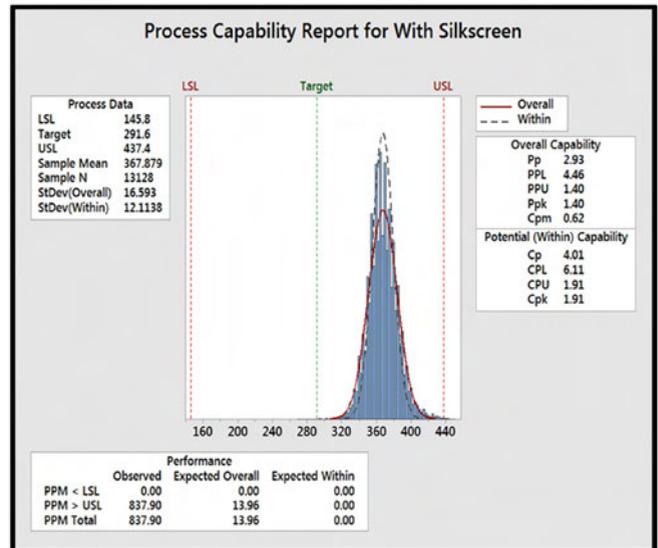


Figure 9: Process capability graph on a 0.4 mm pitch CSP with silkscreen on the PCB. Volume (mil³) specification limit of 50-150%. The mean value shifted to the upper specification limit due to the impact of silkscreen.



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Powder Type J-STD-005	Size Range (micron)	
3	25	45
4	20	38
4.5	20	32
5	15	25

Table 1: Powder types according to J-STD-005.

Even though reflow in air is possible, nitrogen reflow is most common in the market for type 5 powders.

Process

From a process point of view, screen printing has always been the major contributor of yield loss. Many investigations over the last few years have shown that printing can contribute to 60-70% of the overall process yield loss, followed by reflow soldering ranging between 10-20%.

Voiding, Graping, and HIP

Recently, QFN voiding has become a very hot topic. In some cases, reducing QFN voiding can be done with the help of a hot and long soak, burning off more flux residues that could lead to excessive voiding.

The drive for reduced QFN voiding can lead to an increase of graping on 0201 and 01005 passive parts and an increase of head-in-pillow (HIP) on fine-pitch CSPs and PoPs. Many studies show that graping does not have a negative impact on shear strength, but it is a clear process indicator for HIP. In both cases, flux exhaustion is caused by excessive heat and time before the solder joints are formed.

With regards to HIP, there are also other factors such as warpage and ball/bump contamination that impact the total amount of failures.

The head-in-pillow defect (Figure 10) is an open solder joint in a BGA or CSP where the solder paste deposit does not coalesce to the ball on the component. The result is an apparent solder joint with a gap between the solder reflowed to the PCB paste and the solder ball itself. This defect is particularly troublesome

FLUX	Powder	Cp	Cpk
A	Type 5	2.2	2.18
A	Type 4.5	1.82	1.81
B	Type 5	2.05	2.04

Table 2: Cp and Cpk comparing type 4.5 and type 5 powder on a 0.2 x 0.2 mm aperture and 0.08 mm thick stencil (AR=0.625).



Figure 10: Typical HIP issue when using too long of a soak time and too high of a soak temperature. This issue could pass a functional test and end up as a field return.

because it is very difficult to detect, even with X-ray inspection.

In addition, sometimes there is mechanical contact between the two solder deposits allows it to pass functional testing but it fails later in the assembly process or in worst case on the field.

Graping (Figures 11-12) is also in many cases referred to as cold solder. Not understanding the true root cause of the issue drives a different set of potential process solutions that in many cases magnifies the issue.

Graping typically happens on smaller solder paste deposits (Figure 13) due to fact that the smaller amount of solder pastes results in smaller amounts of flux to remove oxides.



Figure 11: Graping illustration.

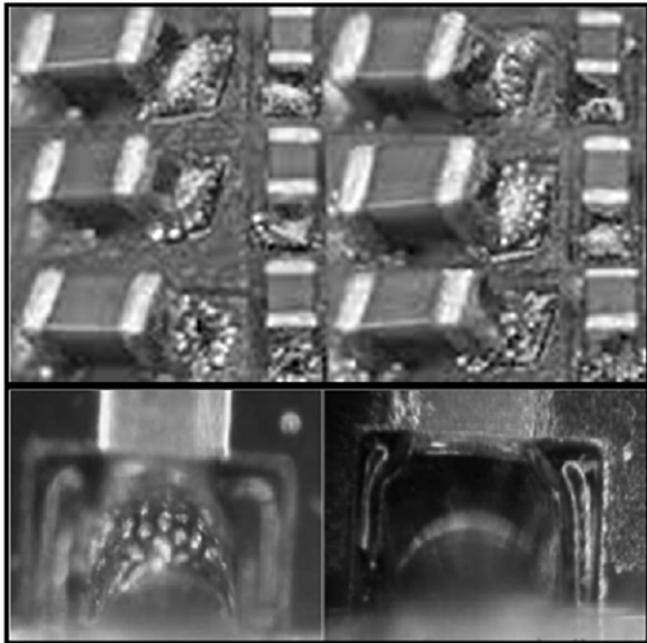


Figure 12: Actual images of graping of 01005 components (top and lower left), and a good solder joint on 01005 lower right).

In IPC 610 section 1.5.2, the following definition can be found:

“Cold Solder Connection: A solder connection that exhibits poor wetting and that is characterized by a grayish porous appearance. (This is due to excessive impurities in the solder, inadequate cleaning prior to soldering, and/or the insufficient application of heat during the soldering process.)”

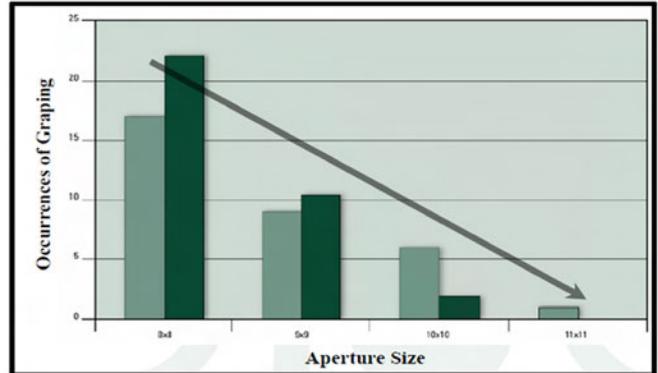


Figure 13: Impact of aperture size on amount of graping.

Ramp rate 180-220°C (°C/s)	Yield Loss (%)
0.7 (air reflow)	1.5
0.7 (Nitrogen reflow)	0
1.2 (air reflow)	0

Table 3: Yield loss on an actual product at different ramp rates and in air vs. nitrogen reflow for a 0.4 mm pitch CSP.

In section 5.2.5, this is further explained by including rosin connection. Cold and rosin connections are both classified as a defect for IPC Class 1-3.

In section 5.2.3 of IPC 610 Soldering Anomalies – Reflow of Solder Paste, incomplete wetting is classified as a defect for IPC Class 1-3.

Below is an example using a 0.4 mm pitch CSP with 0.25 mm round apertures and a 0.1 mm thick laser-cut stencil. This shows that, by increasing the ramp rate above 180°C from 0.7°C/s to 1.2°C/s, the HIP defect detected in functional testing is reduced from 1.5% to 0% (Table 3).

In this case, nitrogen (<1,000ppm of O₂) reflow (Table 3) has the same positive effect on the functional yields. One thing to keep in mind is that this is functional test yield loss, and many HIP defects might not be captured because there could be marginal mechanical and electrical connections.

Alloy	Temperature °C	
	Liquidus	Solidus
SAC 305	220	217
SAC 387	220	217

Table 4: Liquidus and solidus temperatures for SAC 305 and SAC 387.

Another common mistake is using 217°C as the liquidus temperature for SAC 305 and SAC 387. The liquidus temperature for SAC 305 and SAC 387 is 220°C and it is the solidus that is 217°C.

This can lead to some confusion when setting the specification limits for the reflow profile. If the plateau is between 219-220°C, this can lead to severe flux exhaustion resulting in graping and HIP in hip-scale packages (CSP) and package-on-package (PoP).

Inspection Tools for Voiding, Graping, and HIP

There is no set requirement for the QFN voiding limit, and each company has their own specification. The range can vary between 15-50% for standard applications and down to 5% for special applications.

X-ray is the most common way to verify the voiding levels, and most modern X-ray equipment will do an accurate void calculation.

The issue is that many production lines worldwide do not have adequate high-magnification microscopes to validate that the void reduction don't have a negative impact on solder joint quality.

IPC 610 clearly specifies that the minimum magnification required for solder joints <0.25 mm should be 20X, and in many cases, only a 2-4X magnification glass is available; a graping issue would easily be missed when using 2-4X magnification glass.

Conclusion

It is very important to understand design, materials, and process since they are very closely connected. There are many ways to achieve high-density assemblies, and it is crucial to have a "toolbox of technologies" to be able

to fulfill various requirements. It is also necessary to consider the interaction between multiple technologies in all areas during development and deployment since several advanced technologies will, in most cases, be used on the same product. Depending on the end product, several options can be considered and the selection should be based on data and not assumptions. **SMT**

Editor's Note: This article was originally published in the proceedings of SMTA International.

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[**RTW SMTAI: AIM's Dr. Mehran Maalekian Speaks on New Alloys for Harsh Environments**](#)

Dr. Mehran Maalekian, R&D manager at AIM Solder, speaks with I-Connect007 Managing Editor Andy Shaughnessy about new alloys that are targeted for high-temperature and demanding applications, particularly in harsh environments, where standard lead-free alloy such as SAC will not perform as well.

[**RTW SMTAI: Alpha Discusses Solder Dross Reclamation**](#)

At the recent SMTA International 2017 exhibition in Rosemont, Illinois, Mitch Holtzer, director of Americas Reclaim Business of Alpha Assembly Solutions, talks with Managing Editor Andy Shaughnessy about the solder dross reclamation process, and discusses his new role in leading Alpha's reclamation business.

[**Indium Expands Global Corporate Leadership Team**](#)

Indium Corporation has expanded the responsibilities of its global leadership team with the promotion of several top executives.

[**Seica to Exhibit at productronica**](#)

Seica S.p.A. will be showcasing its latest testing solutions at productronica 2017.

[**CyberOptics Launches Coordinate Measurement Software for High-Speed SQ3000 CMM System**](#)

CyberOptics Corporation has launched the new SQ3000 3D CMM system, powered by Multi-Reflection Suppression technology and CyberCM, a new comprehensive software suite for coordinate measurement.

[**Fuji America to Include Aegis' FactoryLogix NPI Software with Nexim**](#)

Fuji America Corp. will include Aegis Software's FactoryLogix software solution with their Nexim

Factory Control Software through an extended agreement between the two companies.

[**INTERFLUX Electronics Completes Testing on New Alloy at Ersu Demo Room**](#)

Kurtz Ersu North America recently completed tests with INTERFLUX Electronics on a new solder alloy.

[**Gen3 Systems Appointed Distributor for Nordson SELECT Selective Soldering Equipment**](#)

Gen3 Systems Ltd has been formally appointed as exclusive distributor in UK and Ireland for Nordson SELECT Selective Soldering Systems.

[**EU Commission Launches Stakeholder Consultation on RoHS Exemptions**](#)

IPC, in conjunction with an international industry stakeholder group, applied for more than a dozen exemption extension requests under the EU RoHS Directive.

[**BEST Releases Sustainable Version of J-STD-001 Soldering Kit**](#)

BEST Inc. has released an updated version of the Revision "F" IPC-JSTD-001 training kit.



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DEALING WITH VIAS IN PADS

by **Stephen Las Marias**

I-CONNECT007

Screaming Circuits, a division of EMS firm Milwaukee Electronics, specializes in short-run, one-off, and prototype PCB assembly. For instance, if you need two or three prototypes and you need them in just a couple of days—that's what the company does. Or if you need 500 or 5,000 production boards, for example, if you had a Kickstarter and you sold 500 and you don't know if you'll sell any more—most manufacturing companies don't want that business, but that's where Screaming Circuits comes in.

It's all about small volumes, unforecastable, uncertain volumes, according to Duane Benson, chief technology officer and marketing manager at Screaming Circuits. "That gives us a very large set of experience because we see so many different jobs; we see virtually any kind of component tree applications that you might possibly imagine."

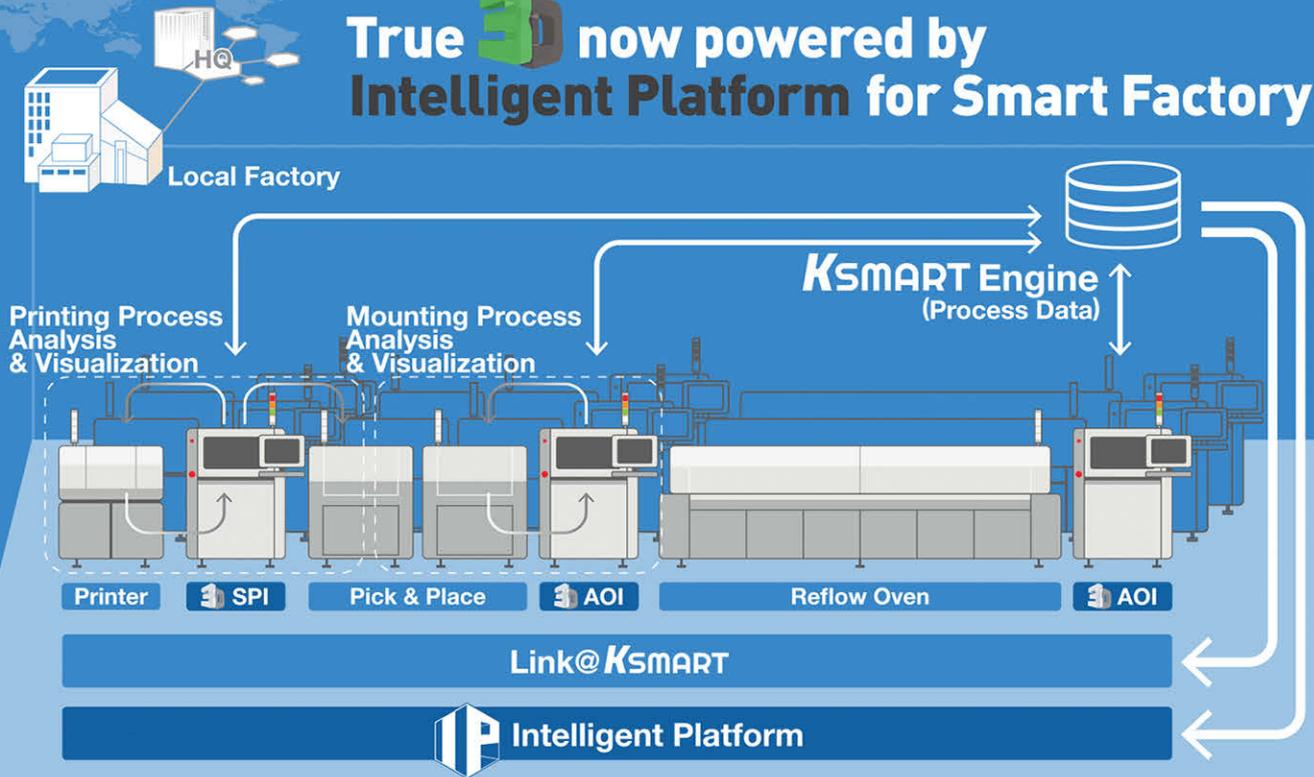
In another interview, Mike Creeden, vice president of layout services at sister company San Diego PCB Design LLC, said via-in-pad, even if it's a plated through-hole via, is a form of HDI.

With that in mind, I interviewed Benson about the challenges when dealing with microvias and vias-in-pads from an assembly standpoint, and how in-circuit test (ICT) issues, such as access to test points, can be addressed.

Generally, Benson said there's not that much issue for the assemblers when it comes to microvias or HDI. However, he notes that no matter how small the vias are, especially in via-in-pad, they have to be plugged and filled at the fabricator side, must be plated over, and has to have a very planar surface.

"That's the biggest challenge with the high-density vias—making sure that they're properly plugged and plated at the board house, and then that they leave a planar surface. If it's nice and flat like that, for assembly purposes, it doesn't matter—we don't really know that it's there really. Some people like to leave the microvias partially open—there would be a via open going from one layer to the next. With the tiny micro BGA, if you do that, you are going to end up with an air bubble inside the BGA ball, which might crack under stress, and it might not totally connect," said Benson. "Basically, the only thing for a super fine pitch BGAs and those types of vias, the only proper way to

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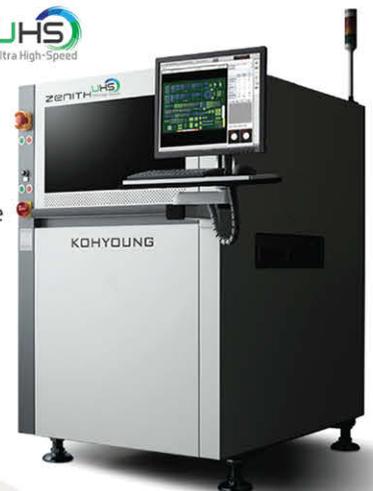


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avoid assembly problems is to have them filled and plated at the board house, and leaving a flat, planar surface. That's really the only option. Between the pads, you have to make sure that there is a complete and total solder mask dam between the pad and the via."

If vias are open, there's this possibility of solder flowing into them during the reflow process. "You can end up with outgassing—flux that didn't fully activate. It's just bad news," said Benson. "Really, with microvias, especially when it comes to BGA pads, you got to have them plugged and filled at the board house. You got to have a nice, flat, planar metal surface; there's really no other option for assembly with those tiny little parts. We would normally catch that before it goes to the board house. So, then we would go back to the designer, one of our manufacturing engineers would call them up, and let them know how to avoid that. If the via is in the pad, the two ways to avoid that are: (a) move it outside of the pad; or (b) connect with the board house and let them fill it and plate it over. We would give that advice to the designer."

Another issue with via-in-pads is the limited access for ICT. Screaming Circuits, however, typically doesn't do these tests because it is just dealing with prototypes. "What our volume production facility, Milwaukee Electronics,



Duane Benson

a more-traditional EMS, typically would do is our engineers would go back to the designer. If the test program is needed, we will have to say, 'We can't test without a test point here.' Quite often, you will end up with a hybrid of either bed of nails or flying probe, and a functional test. You can detect a lot of problems with a functional test, even if the pads are underneath the BGAs or hidden. But not everything. You will end up with some test

points added in and potentially use of software-based testing system," said Benson.

"In the prototype world, we make do with what we got. But when we are going to build hundreds or thousands, or tens of thousands of things, we will have to have our manufacturing engineers connected with the design engineers before those volume productions. Sometimes, what's going to happen is we'll get a prototype, we'll build it, and they will modify the design, then build it again, and then say, 'We're ready to go to volume production.'" Then, we'll go through an additional NPI process. If we found that it can't be tested, or it can't be reliably built because of some of those issues, whether they are HDI related or not, we would give them guidance on where or how to modify the designs so that they will be reliable and testable." **SMT**

Mentor Eases Programming in Viscom Inspection Systems

At the recent SMTA International 2017 exhibition, Jesper Lykke, engineering manager for USA of Viscom AG, and Zac Elliott, technical marketing engineer at Mentor, speak with I-Connect007 Managing Editor Andy Shaughnessy about Viscom's adoption of the Valor Process Preparation and how it is helping users with their inspection programming.

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The Proper Position to Take on Voids in Solder Joints, Part 1

by Tom Borkes, The Jefferson Institute

Component Cost Disparity Study Update

First, a quick update on the conclusion to our material pricing disparity study.^{1,2,3,4} Unfortunately, we have received “crickets” from the agencies that were contacted. In my opinion, this industry issue is too important to drop. So, we’ll keep digging for data. If any of you in our reading audience can contribute data or firsthand experiences concerning the price of assembly material in high labor rate regions, versus material pricing when the assembly is done remotely in low labor rate areas, please let me know. Of course, as suggested in a past column⁵ this issue becomes moot if the components begin to be manufactured in the same geographic location where they are assembled into products.

The many current reshoring efforts being undertaken in high labor rate regions make the issue crucial. This is especially true if the assembly activity is being done by a company which is of small or medium size, either an EMS (electronic manufacturing services) or an OPD (original product developer)—specifically, one that does not have multiple global assembly operations served by a central procurement capability.

On Solder Joint Voids—The Dilemma

In parallel to the continuing attempt to gather data that address the disparity in component cost between high- and low-labor rate assembly regions, in this column, we leap off the bandwagon into another thorny issue: solder joint voiding.

On the surface, it doesn’t seem to be an issue: “No voiding permitted.” That’s easy. However, not so fast says Inspector John J. Fadoodle, America’s #1 private eye. The number of variables involved in void creation is daunting and not as well understood as you might think, notwithstanding the hundreds of technical papers written on the subject. And, there will be voids.





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The void acceptance criterion is ill defined and strongly tied to void locations, volume and size. In addition, void acceptance is largely a function of a product's end use—Class 1, 2 or 3? And, to make it worse it's important to understand what type of component the solder joint in question is attaching to the circuit board (e.g. BGA, micro BGA, LGA, CSP, QFP, QFN, QFD, DCA, passive devices, etc.). What about stacked memory modules? Add to that, how are we measuring a solder joint's void population and character? 2D, 3D? And, of what can be thousands of solder joints on a circuit board, which ones do we inspect? All of them? No, that's time prohibitive. Then how many and which ones should we look at?

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“Now, if you think this is a knotty issue for an OPD who assembles the products they design, pity the poor EMS.”

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Now, if you think this is a knotty issue for an OPD who assembles the products they design, pity the poor EMS. They build other company's products. Does their ODP customer bring a void spec to the table? Is it a requirement of the purchase order? Do they invoke the requirements of joint standard IPC-STD-001, which in turn invokes the requirements of industry standards—IPC 610 and IPC 7095? Or, do they look to their EMS for guidance on voiding acceptability?

If the product fails in the field because of a solder joint that has fractured, who carries the liability? Who underwrites the cost of establishing root cause for the failure?

Void Reduction at SMTA International

This column is being written a few weeks after this year's SMTA International in Chicago. I hope many of you had the opportunity to attend the conference. In lieu of a more re-

sponsive and timely post-secondary educational system, this annual event brings leading edge issues and production equipment to the attention of our real world electronic product assembly community.

At the conference I chaired a technical session entitled “Void Reduction.” Here is the session description:

This session presents three papers that document the results of solder joint void studies. All three studies were performed to establish the causal relationships that exist between material selection and process environment variables and the reduction in solder joint voiding. The first paper addresses the effect of solder reflow environment, paste printing material and printing process variables. The second is the third part in a series of papers on voiding. It provides the results of a parametric study conducted to examine void reduction as a function of paste powder size, solder alloy and PCB surface finish when using QFN, BGA and LGA components. The third paper describes a new process technique that applies sinusoidal vibration to the circuit board during solder joint formation in order to reduce voiding.^{6,7,8}

I think it is significant that there were no papers that addressed what is an acceptable level of voiding based on empirical testing or analytical study. There was no session entitled “Acceptable Voiding.” However, I believe IPC has a working committee that is tasked with updating the current industry specs. The message in the “Void Reduction” session as it was described in last month's SMT Magazine, “Achieving the Perfect Solder Joint,” do everything possible to eliminate or at least minimize voiding.

“Acceptable” voiding is left to specification organizations and colleagues that have attempted to quantify the issue.^{9,10} Most of these have focused on voiding in BGA solder joints. So, let's eliminate voiding.

Cost Consequences

What is the cost? I remember the “zero defect” obsession. A zero-defect rate for products being shipped is certainly a justifiable and necessary production requirement. However, in-process zero defects? Even a 6-sigma defect pro-

cess translates to 3.4 DPMO (defects per million opportunities).

And, in the real world most electronic assembly operations aim for 5-sigma (233 DPMO) or even a 4-sigma (6,210 DPMO) defect rate. If there are 1000 solder joints (opportunities) per board, there will be about six board failures per 1000 at 4-sigma and less than one board failing per 1000 at 5-sigma—even less board failures if more than one defect is found per board considered.

How much money are you willing to spend to wring out all but 3.4 in-process DPMO to attain 6-sigma? Of course, if the defects are random and not in the assignable cause category, no amount of money will identify their root cause.

Since we began this Jumping Off the Bandwagon column, we have stressed the competitive importance of high assembly yields to reduce labor content in high labor rate regions of the globe. And, with a first-pass in-circuit test (ICT) yield of 99.6% coupled with passing a functional test as the board's final acceptance (4 failures per 1000 boards or 4,000 DPMB (defects per million boards—assuming 1 defect per failed board), it makes sense to eliminate the ICT. The functional test will identify the defective circuit boards. It doesn't pay back to subject 4000 boards to ICT to find the four with defects.

Let's start with this: The product team, whether they belong to an OPD or an EMS, should write a quality assurance plan (QAP) for each assembly. Unfortunately, today I find most people in the industry don't even know the difference between quality assurance (QA) and quality control (QC).

The QAP must clearly state what the acceptance criteria is for voiding and the inspection plan that will be used to ensure this acceptance level is met. The plan may invoke industry standards as well as company standard operating procedures (SOP) and any specific quality requirements such as inspection sampling plans, both automated and manual.

In most cases the student who moves through the looking glass from the academic side to the real-world side has most likely never even heard the phrase "solder joint void."

Is History Repeating Itself?

A couple of firsthand experiences from the graveyard of forgotten favorites:

1. Do you remember tweakers? Before circuit board labor content became an issue (pre-low labor rate competition, circa 1983) and when component placement accuracy had significantly more variation than we have today, many board assembly lines stationed a tweaker(s) between the exit of the pick and place machine and entrance of the reflow oven. With tweezers in hand their job was to gently center components that were not perfectly placed in the wet solder paste. So, if even one component was tweaked per board the true first pass yield was zero. This reactive process caused much unnecessary rework to be done. This is the risk with how we approach solder joint voids. However, the risk is much more serious and costly since it in post reflow rework.

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“ This is the risk with how we approach solder joint voids. However, the risk is much more serious and costly since it in post reflow rework. ”

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2. I remember the beginning of the commercial use of SMT. Assembly processes were being refined and there was significant process uncertainty accompanying the use of these components—components that weren't anchored to the PCB with a lead that went through the board with a plated-through barrel full of solder. This caused a cautious approach in permitting the use of this new technology in the military. The Air Force was seduced by the lighter weight. However, they needed to be persuaded that the use of SMT in their electronic equipment was at least as good as the traditional pin-in-hole (PIH) technology and did not reduce the reliability of the system.

When an aircraft testing the technology had its navigational system fail in flight, the flags

went up. Upon opening the failed electronic assembly, a number of SMT components were found loose, rattling around in the bottom of the chassis. Uh oh! Clearly the new component technology was not as robust as the tried and true through-hole technology. Or, was it? What was the root cause of the solder joint failures? It turns out it wasn't anything inherent about SMT technology. In fact, an objective comparative look at the technology suggests that all things being equal using SMT should result in a more reliable assembly—less mass and a lower center of gravity. These characteristics result in a component-to-board assembly with a higher natural frequency. Consequently, there is less chance of the attachment going into resonance and resulting in a solder joint failure from the mechanical stresses induced by vibration and fatigue. Performance in shock and temperature environments should be better as well. The thermal stress developed between two different materials is proportional to the change in temperature, difference in thermal coefficient of expansion between the two materials (TCE), and the initial length of the interface.

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“In politics, a favorite catch phrase is: “It’s the economy, stupid.” In this case, we say, “It’s the process, stupid.””

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So, what was it? In politics, a favorite catch phrase is: “It’s the economy, stupid.” In this case, we say, “It’s the process, stupid.” Many independent studies have linked solder joint mean-time-to-failure (MTTF) to the temperature the solder is exposed to during the assembly process. In this case the peak temperature and temperature duration caused the solder joint embrittlement. (Think of integrating the time/temperature reflow profile—effectively, summing the total thermal energy applied to solder during the reflow process.) The solder joints looked fine—nice, concave fillets. However, the

metallographic grain boundaries formed during overheating caused joint failure with very little applied force.

Like in these examples, we can be misled if we don't understand the science associated with the process. So, we try and minimize voids. What this has come down to in many cases is developing soldering materials and processes that minimize voids. However, there will be voids. If the voids are not acceptable, what then? Are you going to have a battery of rework operators “touching up” void-laden solder joints? Then, it's back to the X-ray machine.

Voids and Process Capability

Do we challenge the specifications? Should most voids be relegated to the “Process Indicator” category? Should a voiding baseline be established as part of a process capability study? Maybe some lap shear destructive testing should be done as a qualification test. And, if deemed acceptable, use the voiding baseline to compare production results in real time. Then, when a statistically significant negative change in voiding occurs use this to proactively highlight that an assignable cause is entering the process. Even better, if the root cause of the change in voiding can be identified by an automated statistical process control system, the system may be able to make the necessary corrective action in the process without engineering intervention—what we have called Meta Process Control—sometimes called Factory 4.0. The strategic key is to be able to identify voiding changes in production to the capability study baseline in real time, not after 100 boards have been assembled with unacceptable voids.

What We Should Want

The full first line in the song “A Must to Avoid,” by Herman's Hermits, is “She’s a must to avoid, a complete impossibility.”

So, should we require perfect solder joints?

Perfectly placed components off the pick and place machine? Zero voiding? Zero in-process defects? Variation in results will take place whether we like it or not. The time the bus arrives at the bus stop everyday will vary in accordance with a normal distribution (i.e., Bell or Gaussian curve). If the variation falls outside

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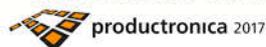


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the confines of normal distribution it is because a “non-natural” assignable cause has pushed or pulled it. If we require perfection, first know we will never achieve it. Second, we need to ask: At what cost? Does the cost justify the benefit? And, if we end up demanding perfection we need to make sure someone is designated to turn off the lights and close the door when our production business goes out of business.

At least that’s what I think. Hey, what do YOU say? I’d like to hear your thoughts, reactions and opinions. And, please, if you have knowledge and/or experiences concerning the material pricing disparity between products assembled in low and high labor rate regions of the world please contact me. **SMT**

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Tom Borkes is the founder of the Jefferson Project and the forthcoming Jefferson Institute of Technology. To read past columns or to contact Borkes, [click here](#).

EPTAC Discusses Manufacturing Training Trends

During SMTA International 2017, Leo Lambert, vice president and technical director of EPTAC, discusses with I-Connect007 Managing Editor Andy Shaughnessy, his company’s recent expansion and the trends he’s seeing in manufacturing training.

[Watch the interview here.](#)





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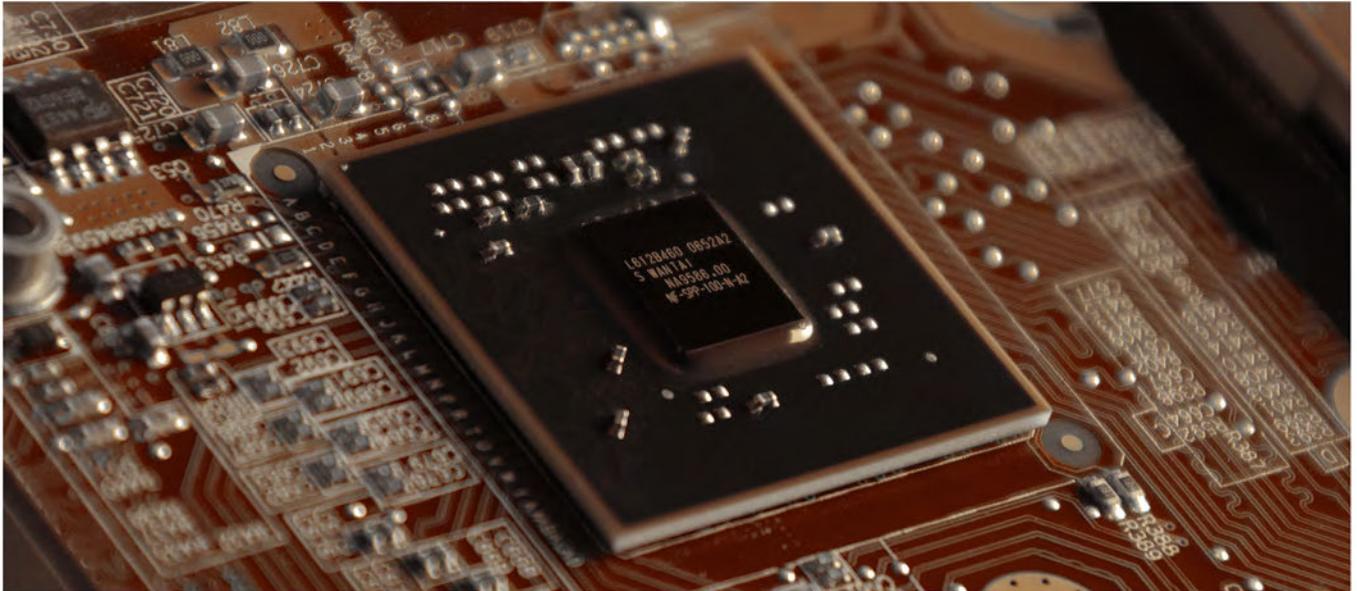
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Via-in-Pad Plated over Design Considerations to Mitigate Solder Separation Failure

by **S.Y. Teng, P. Peretta and P. Ton,**
 CISCO SYSTEMS INC.;
and V. Kome-ong and W. Kamanee,
 CELESTICA THAILAND

As signal speeds and performance requirements continue to rise, the use of advanced PCB technologies is becoming increasingly important. As a result, the via-in-pad plated over (VIPPO) structure has been adopted in many BGA footprint designs within the PCB. These VIPPO structures are preferred over the more traditional dog-bone pad structure in order to shrink signal path lengths, reducing two parasitic effects,

capacitance and inductance, for improved high-speed performance. Figure 1 illustrates how the VIPPO structure can influence those parasitic effects. The signal traces, which connect the BGA pads with the vias, act as inductors. Additionally, as high-speed designs typically have ground planes immediately below the outer layer, there is also a capacitive effect that is generated. With the VIPPO structure, the outer trace layer is eliminated, thereby cancelling both parasitic effects.

Figure 2 exhibits the VIPPO structure as compared with the VIPPO + backdrill (BD) structure. The use of backdrill with the VIPPO structure

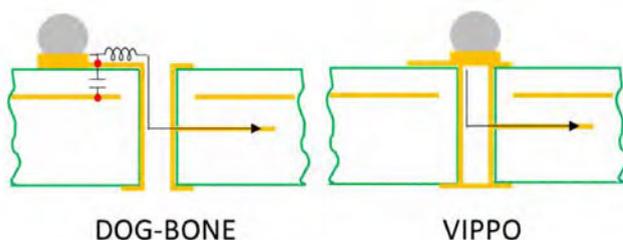


Figure 1: Dog-bone vs. VIPPO pad structure.

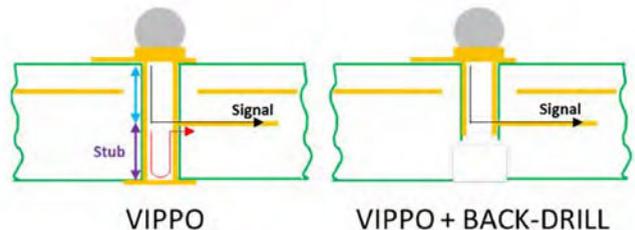


Figure 2: VIPPO vs. VIPPO + back-drill structure.

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can eliminate the reflections within the unused portion of the via, which acts as a stub. The portion of the via indicated by the purple arrow is not in series with the signal path, but instead acts as a stub. Therefore, a portion of the signal is reflected back, creating an interference, which will degrade the high-speed signal performance. Hence, the purpose of the back-drill is to remove this “unused” portion of the via in order to eliminate the reflections for a cleaner signal.

With increased complexity of PCB designs for high-end networking products, the boards thicknesses are typically >120 mils and signal speeds are reaching 25 GHz and beyond. For these types of designs, backdrilling of the VIPPO structures becomes imperative.

It is also a common practice to mix VIPPO and non-VIPPO pad structures within a single BGA footprint, as indicated in Figure 3. The green lines indicate a high-speed signal trace (e.g., for differential pairs) on the outer layer. It is preferable from a signal integrity perspective, to route these signal lines on the outer layers of the PCB to take advantage of microstrip routing which has faster propagation speeds than stripline routing. Hence, these BGA pads do not require the use of VIPPO. These non-VIPPO pads are highlighted in red. Without any VIPPO structure, a zero stub length can be achieved,

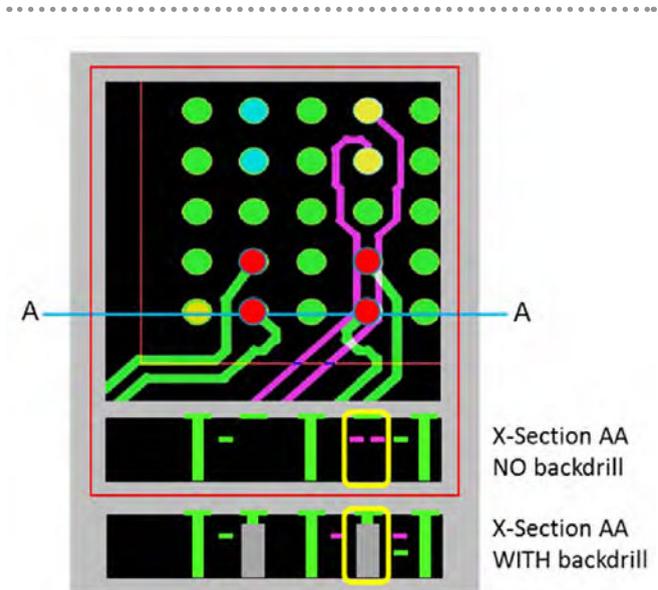


Figure 3: Mixed VIPPO/Non-VIPPO BGA Footprint.

which is an extremely attractive option for the signal integrity engineer. Moreover, additional routing space is gained underneath the non-VIPPO pad. Unfortunately, these types of mixed footprint designs have a propensity for manufacturing defects during SMT assembly of BGA packages and can potentially expose the PCBA to field reliability risks if these defects escape manufacturing tests.

Failure Mode and History

As a consequence of these advanced PCB technologies and complex board designs, a unique BGA solder joint failure mode has emerged during specific assembly conditions. This failure mode occurs when the bulk solder separates from the IMC during or just prior to reflow. This failure mode is of particular concern because the discontinuity is so small relative to the size of the solder joint itself that it cannot be detected via X-ray inspection methodologies. Furthermore, in many cases it is only a partial separation of the BGA solder joint and hence, it may not even be detected via ICT or functional test techniques. Without a robust methodology to screen for these defects, this presents an extremely high risk for potential escapes to the field.

Typically, this failure mode has been found on BGA packages with a 1 mm pitch or less BGA array and having a PCB footprint that includes a mixed VIPPO/non-VIPPO pad design. The solder separation occurs when the component is subjected to a secondary reflow, either during top-side SMT for bottom-side components or during rework of an adjacent, or mirrored, BGA component. Since the open occurs between the bulk solder and the IMC, it does not have the typical brittle solder joint fracture signature, which has a flat fracture interface through the IMC as shown in Figure 4. Instead, this failure mode exhibits more of a hot solder tear or separation type of failure mode, as the solder separates from the IMC leaving it intact. [1,2,3] Figures 5 and 6 illustrate examples of both partial and complete solder separations. For these failures, the solder separation only occurs on the solder joints that use a VIPPO BGA pad and is typically adjacent to a solder joint(s) with a non-VIPPO BGA pad. In some cases, this

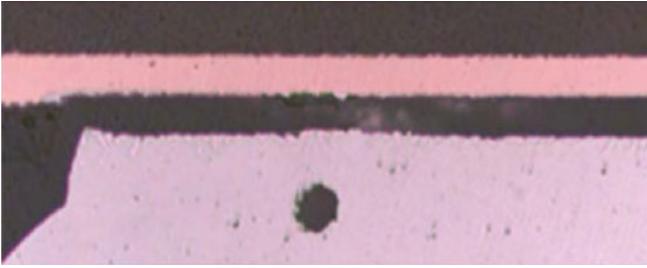


Figure 4: Example of brittle fracture.

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type of failure mode has also been identified on a component having a full VIPPO BGA pad pattern on the PCB when there is also a pattern of VIPPO with deep backdrill (BD) within the footprint. Hence, the deep-backdrill VIPPO structures seem to mimic the behavior of the non-VIPPO pads so that it becomes comparable to a mixed VIPPO/non-VIPPO BGA pad footprint and again, induces solder separation in the solder joints on a VIPPO pad when subjected to a secondary reflow.

Since the separated solder ball shape is rounded near the open or partially open interface, this indicates that the solder joint underwent reflow subsequent to the separation. Furthermore, since the separation is between the bulk solder and the IMC and does not reflect a brittle fracture, it is suspected that the separation occurred after the solder has softened and is nearly molten. Figure 6 illustrates a brittle solder joint failure in which the fracture occurs within the IMC itself and exhibits more of a flat surface indicative of crack propagation.

Failure Mechanism

There seem to be two primary effects that are occurring which contribute to this failure mechanism. First, there is a CTE mismatch between the VIPPO structure and the non-VIPPO, or deep-backdrill VIPPO, structure, that results in a greater expansion of the PCB beneath the non-VIPPO BGA pad, or the deep-backdrill VIPPO pad, as compared with the VIPPO BGA pad. Secondly, the higher thermal conductivity of the VIPPO structure as compared with the non-VIPPO, or deep-backdrill VIPPO structure, allows the VIPPO solder joints to reach liquidus before the adjacent solder joints having a non-



Figure 5: Partial solder separation.

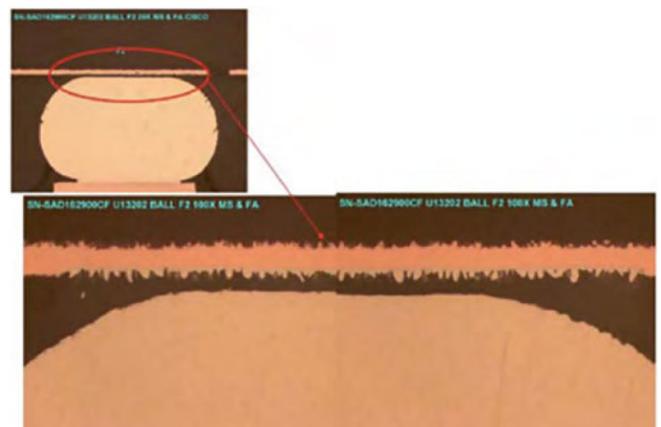
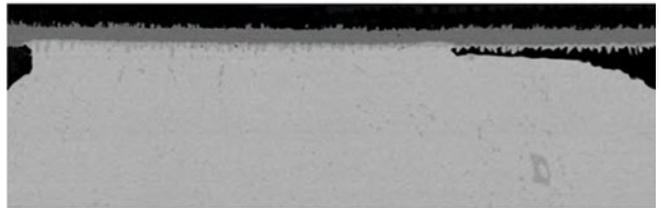


Figure 6: Complete solder separation.

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VIPPO, or deep-backdrill VIPPO pad. Therefore, during a secondary reflow process, when the adjacent non-VIPPO solder joints are still solid, tensile stresses are induced in the VIPPO solder joints as the adjacent non-VIPPO solder joints are pushed up due to the greater out-of-plane PCB expansion beneath those pads.

Subsequently, when the VIPPO solder joints become molten, these high stresses are relieved

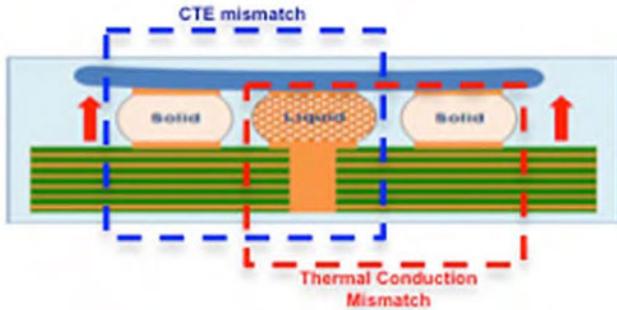


Figure 7: CTE mismatch between VIPPO and adjacent non-VIPPO structures.

as the bulk solder “tears” or separates from the IMC. This solder separation can occur at either the package interface or the PCB interface of the solder joint, depending on whichever is the weaker interface. Since the PCB pad design is generally a non-soldermask-defined pad (NSMD) and the BGA package typically uses soldermask-defined pads (SMD), the separation will more likely occur at the package interface.

Alternatively, a 100% VIPPO BGA footprint without deep backdrill does not introduce the additional stresses that are exhibited with the CTE mismatch between adjacent VIPPO and non-VIPPO pad designs. Additionally, a 100% VIPPO BGA footprint without deep backdrill does not create the high thermal gradients between adjacent solder joints that the mixed VIPPO/non-VIPPO BGA footprints achieve. Therefore, this type of failure mode has not been identified with 100% VIPPO BGA footprints with no deep backdrill.

Evaluation Plan

In order to better understand the influence of various PCB and packaging design parameters on this failure mode, three different test vehicles have been designed to assess the following:

1. Influence of drill hole size (DHS) for the VIPPO structures: 9.8 mils vs. 7.9 mils DHS
2. Influence of BGA package body size and BGA pitch
3. Influence of varying backdrill (BD) depths and BGA package body size

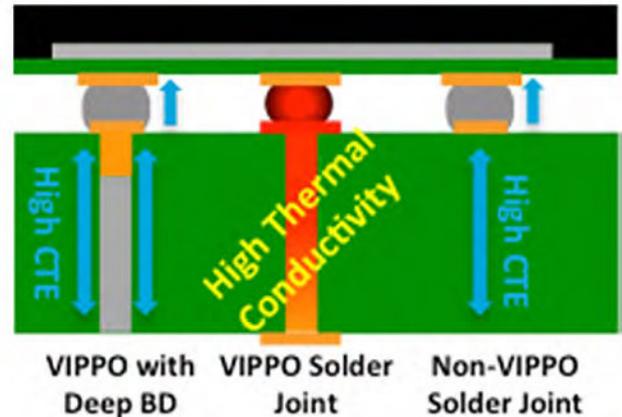


Figure 8: Thermal gradient between VIPPO and non-VIPPO structures.

Each test vehicle is assembled through a primary and secondary SMT attach process, followed by inspection and physical analysis to validate the solder joint integrity after each reflow. The printed circuit assembly equipment, process parameters, tooling (e.g., stencil design and technology), assembly materials (e.g., solder paste) and inspection equipment and methodologies utilized for these builds are consistent with Cisco’s standard production processes in order to minimize the number of variables introduced in this study.

Test Vehicles

The DDR4 VIPPO and non-VIPPO test vehicle (shown in Figure 9) is designed to investigate the influence of two different VIPPO drill hole sizes (DHS), 9.8 mils & 7.9 mils, on the solder joint integrity in a mixed VIPPO and non-VIPPO BGA footprint within the PCB. A set of controlled PCB factors such as PCB thickness (125 mils), material (Megtron 6) and number of stack-up layers (16) are used along with DDR4 daisy chain BGA components (13.3x7.5 mm sq., 0.8 mm pitch) for resistance measurement and failure analysis purposes. The DDR4 components are designed only for single-side PCB assembly. However, for this evaluation, the assembled PCB is subjected to a second SMT reflow excursion in order to simulate a secondary topside reflow process.

The fine pitch VIPPO and non-VIPPO test



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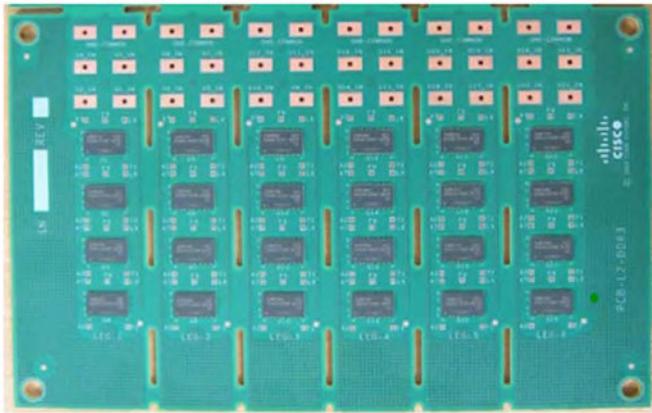


Figure 9: Mixed VIPPO and non-VIPPO test vehicle with multi-drill size.

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vehicle (shown in Figure 10) is used to study the impact of different BGA body sizes, ranging from 10x10 mm sq. up to 37x37 mm sq., in addition to BGA pitches, ranging from 0.7 mm to 1.0 mm, with respect to the solder joint integrity within a mixed VIPPO and non-VIPPO BGA footprint on the PCB. An advanced 7.9 mil DHS

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VIPPO was used in order to accommodate the DHS-to-pad size design rule for BGA pitches < 1.0 mm. The components are designed on both sides of the PCB and utilize the same set of controlled PCB factors as defined in the DDR4 test vehicle for thickness, material and stack-up.

Lastly, the VIPPO and VIPPO + backdrill test vehicle (shown in Figure 11) is designed to investigate the influence of a mixed VIPPO and VIPPO + backdrill BGA footprint on the solder joint integrity. Different backdrill depths (to layer 03, layer 05 and layer 07 on a 28-layer, 130 mil thick PCB design) are studied based on PCB backdrilling depth capability and tolerance. Different daisy chain component BGA body sizes ranging from 10x10 mm sq. to 37x37 mm sq. are again used for this test vehicle.

For all of these test vehicles, each board is subjected to pre- and post-assembly (i.e. after primary and secondary reflow processes) process resistance measurement followed by physical analysis verification with dye and pry and cross-section techniques.

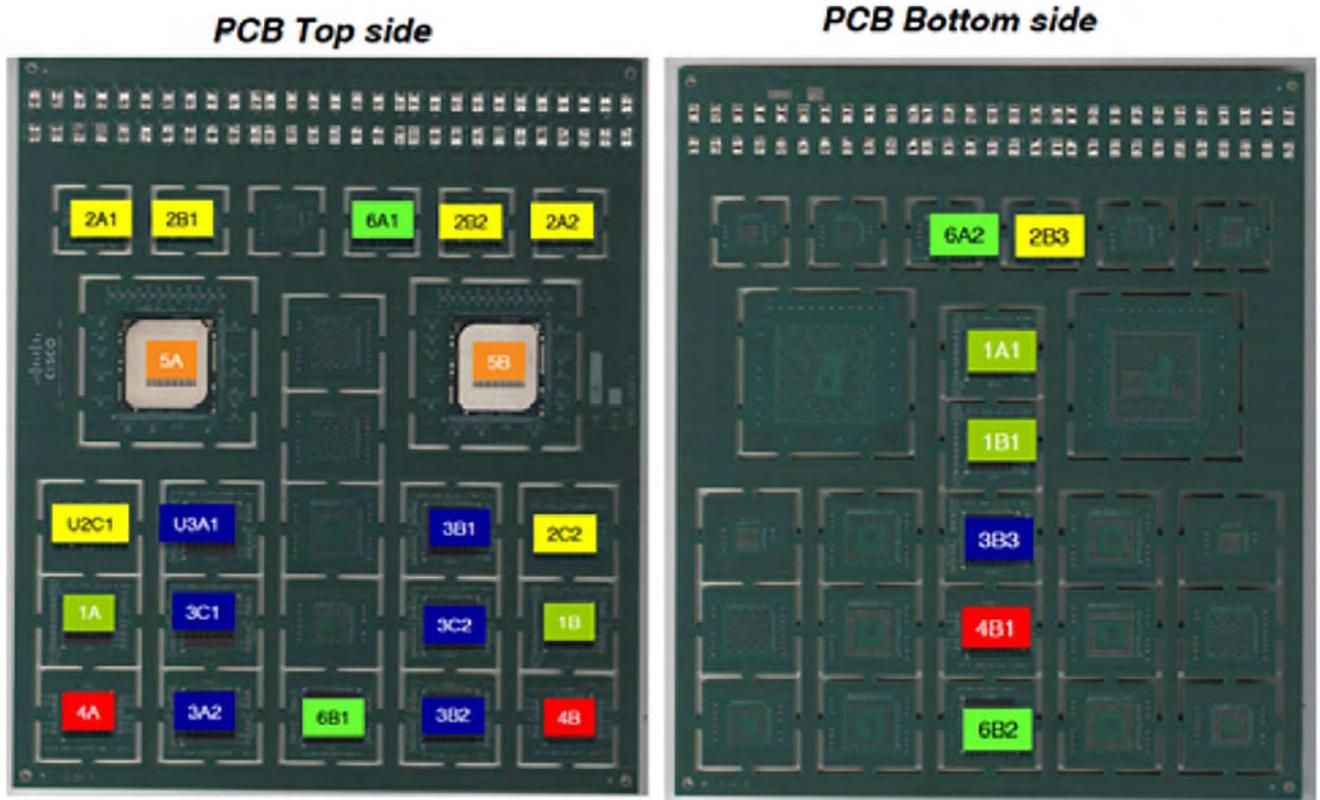


Figure 10: Mixed VIPPO and non-VIPPO test vehicle with multi-package types.

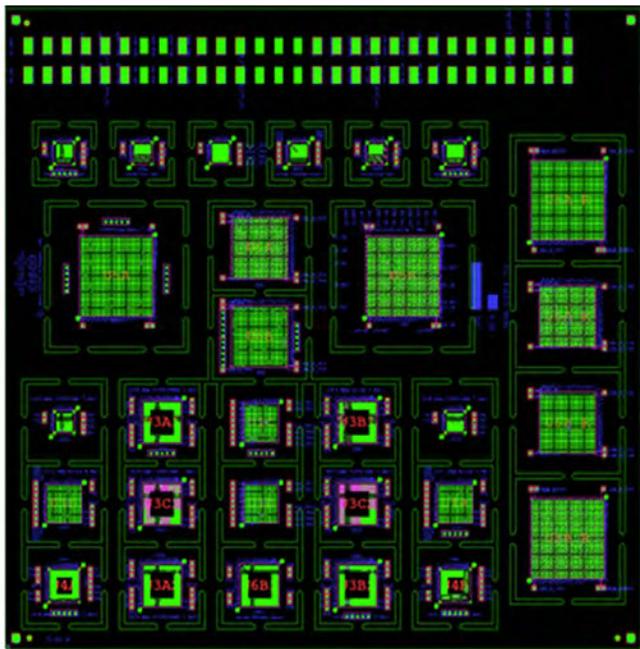


Figure 11: Mixed VIPPO and VIPPO with backdrill test vehicle with multi-package types.

Results and Discussion

DDR4 Test Vehicle

Mixed VIPPO and non-VIPPO BGA footprints with different drill hole sizes were directly compared for this DDR4 test vehicle study. Post-secondary SMT reflow electrical resistance measurements were taken and physical analysis via dye and pry was performed for solder separation failure verification. The experimental control test leg with an all VIPPO pad BGA footprint showed no solder cracks. On the oth-

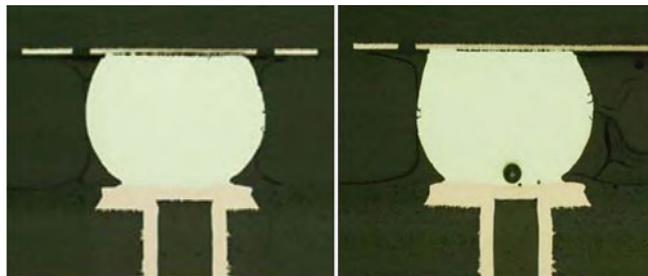


Figure 12: VIPPO pads with 9.8 mil and 7.9 mil DHS post second reflow.

er hand, as shown in Figure 12, all of the designs with mixed VIPPO and non-VIPPO pads within the BGA footprint showed solder separation at the component side of the VIPPO solder joint. The solder separation failure occurred with both 7.9 mil and 9.8 mil drill hole sizes, and hence, confirms that the failure mechanism is independent of drill hole size used in the VIPPO pad structure.

Fine Pitch VIPPO and non-VIPPO Test Vehicle

Employing the same analysis technique, the results obtained for the fine-pitch, mixed BGA VIPPO and non-VIPPO study further confirmed that mixed VIPPO and non-VIPPO pad designs within the same BGA array would result in solder separation at the component side and is independent of BGA pitch and VIPPO drill hole size. However, the data also indicates that BGA body size can influence the outcome of the solder joint integrity for this type of defect.

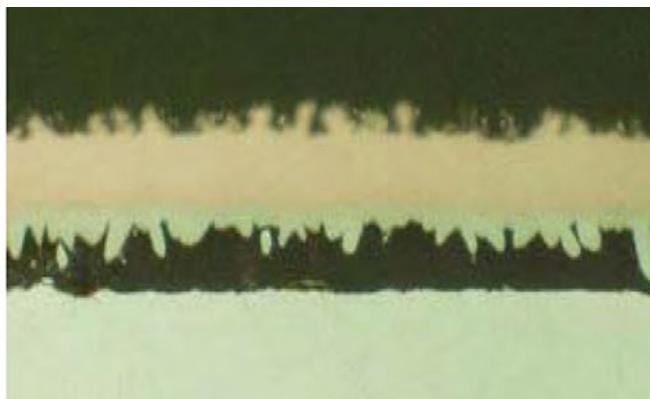
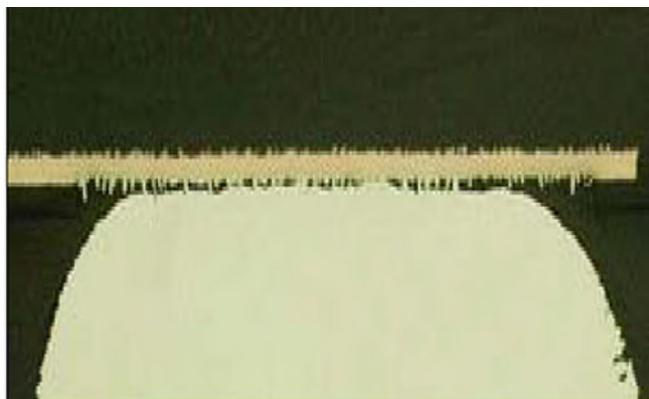


Figure 13: Solder separation interface observed on DDR4 VIPPO + non-VIPPO test vehicle.

This experiment studied 10x10 mm sq., 15x15 mm sq., 17x17 mm sq., 19x19 mm sq. and 37x37 mm sq. package body sizes, and only the 37x37 mm sq. package body size did not result in this solder separation failure mode with the mixed VIPPO and non-VIPPO BGA footprint. However, additional work will be needed to better understand the influence of the package body size on this defect and to determine where the cutoff, or threshold, body size should be defined. Although, the underlying root cause as to why the large body size tends to perform better is not clearly understood, it is hypothesized to be related to the package weight, BGA density and possibly the ratio and locations of the VIPPO-to-non-VIPPO solder joints within the BGA array. The larger 37 mm sq. FCBGA package is much heavier than the smaller overmolded BGA components included on this test vehicle and hence, may require more strain per solder joint to separate from the IMC. This 37 mm sq. package also has a higher BGA density due to its fine pitch (down to 0.7 mm pitch) and exhibits a lower ratio of VIPPO-to-non-VIPPO pads within the BGA footprint as compared with the smaller BGA packages studied.

Furthermore, the locations of the VIPPO pads are grouped together rather than being dispersed among the non-VIPPO pads as seen with the smaller BGA components. This is illustrated in Figure 14 below, showing the non-VIPPO pads connected to a plated through-hole (PTH) in green. Having fewer non-VIPPO pads surrounding the VIPPO pads may induce less strain within the VIPPO solder joints resulting in less likelihood for solder separation for the 37 mm sq. component. Further work in this area should be pursued in order to better understand the influence of these parameters.

VIPPO and VIPPO + Backdrill Test Vehicle

A VIPPO pad with a certain level of backdrilling depth is expected to behave similarly to a non-VIPPO pad. Currently, besides the floating pad with traces, non-VIPPO pads are also defined as pads with microvias (layer 1 to layer 2 via) or skip-vias (layer 1 to layer 3 via). BGA footprint designs combining VIPPO and any of these non-VIPPO pads have been demonstrat-

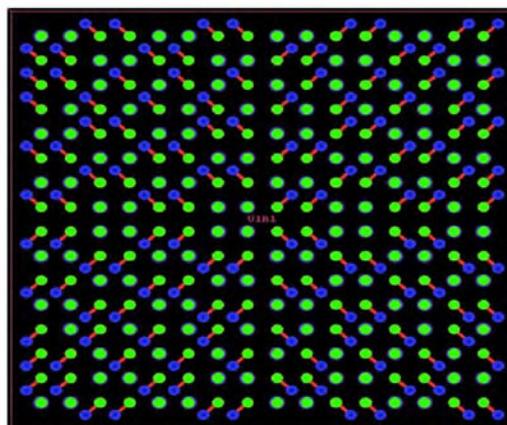
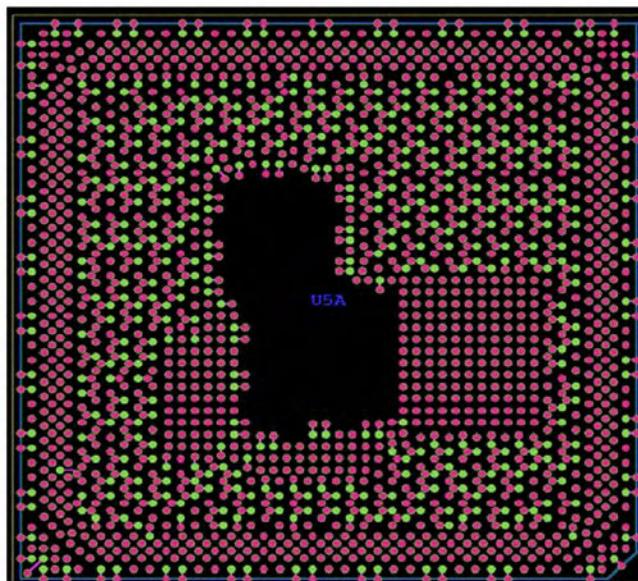


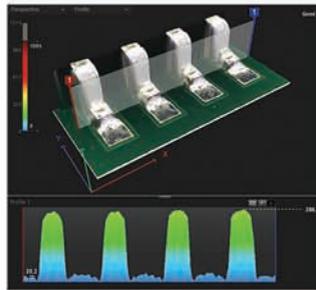
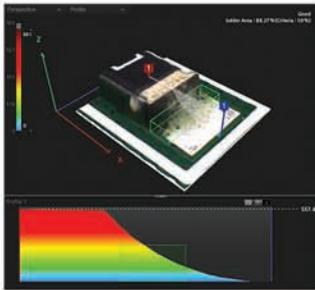
Figure 14: 37x37 mm sq. variable pitch BGA footprint vs. 17x17 mm sq. BGA footprint.

ed to exhibit the solder separation failure mechanism. Therefore, BGA footprint designs with mixed VIPPO and VIPPO + back drilling to some threshold depth would be expected to behave similarly, exhibiting the same solder separation mechanism as seen with these standard mixed VIPPO and non-VIPPO BGA footprint designs. Therefore, the objective of this test vehicle is to understand what this backdrill depth threshold should be within a VIPPO and VIPPO + backdrill BGA footprint in order to prevent the solder separation failure mechanism from occurring. Results from this test vehicle will be used to provide a guideline for future PCB designs with VIPPO and VIPPO + backdrill BGA patterns.



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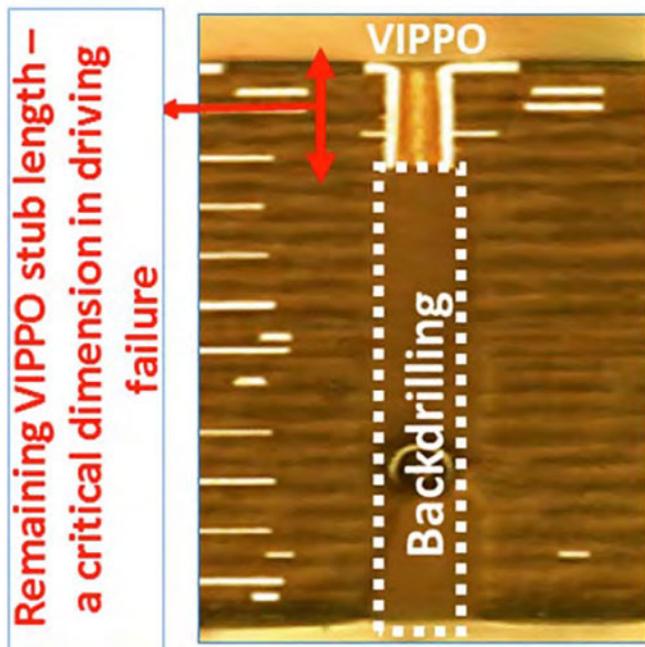


Figure 15: VIPPO stub length after backdrill.

However, the experimental results from this investigation are still pending as the data collection and interpretation is still on-going.

Design Guidelines

The test vehicle experimental data discussed previously has provided a good baseline understanding and insight into the parameters influencing this solder separation failure mode. Because this solder separation failure mode can result in an electrical failure either at manufacturing test or prematurely during field use, it poses a high risk for product launch in terms of solder joint quality and reliability. This establishes the need for specific design guidelines with the use of VIPPO pads. Based on the experimental data thus far, mixed VIPPO and non-VIPPO pad designs within a single BGA footprint are prohibited for applications having a secondary SMT process. For designs having only a single SMT reflow process, the rework process of an adjacent component can still pose a high-risk for solder separation of the adjacent non-reworked component having a mixed VIPPO and non-VIPPO BGA footprint. Therefore, a validated mitigation strategy is required for manufacturing production release of such designs. There is

also on-going work to establish more data with the VIPPO and VIPPO + backdrill pad designs within a single BGA footprint in order to define an acceptable backdrill depth limit which does not induce the solder joint separation failure mechanism.

Summary and Conclusions

This work has evaluated various BGA packaging and PCB design parameters in order to characterize their influence on this double-reflow solder separation failure mode for mixed VIPPO BGA pad footprints. It was observed that this failure mode is not dependent on the BGA pitch and can occur for ≤ 1.0 mm pitch components. It was also found to be independent of the VIPPO drill hole size, occurring with both 9.8 and 7.9 mil drill hole sizes. However, this failure mode has been shown to be sensitive to the BGA package body size, with the risk of occurrence decreasing for large package body sizes. It is also suspected that the package weight, BGA density and ratio and location of VIPPO-to-non-VIPPO pads within the BGA array may also play a role along with the package body size.

As previously noted, the current guidance recommends not to mix the VIPPO pad structures with non-VIPPO pads or deep-backdrill VIPPO structures within a single BGA footprint. Further investigations are still needed to establish more specific guidance regarding the usage of these VIPPO structures with non-VIPPO pad designs or deep-backdrill VIPPO structures. As performance requirements continue to advance, these types of PCB structures and designs will become a necessity for future generations of products.

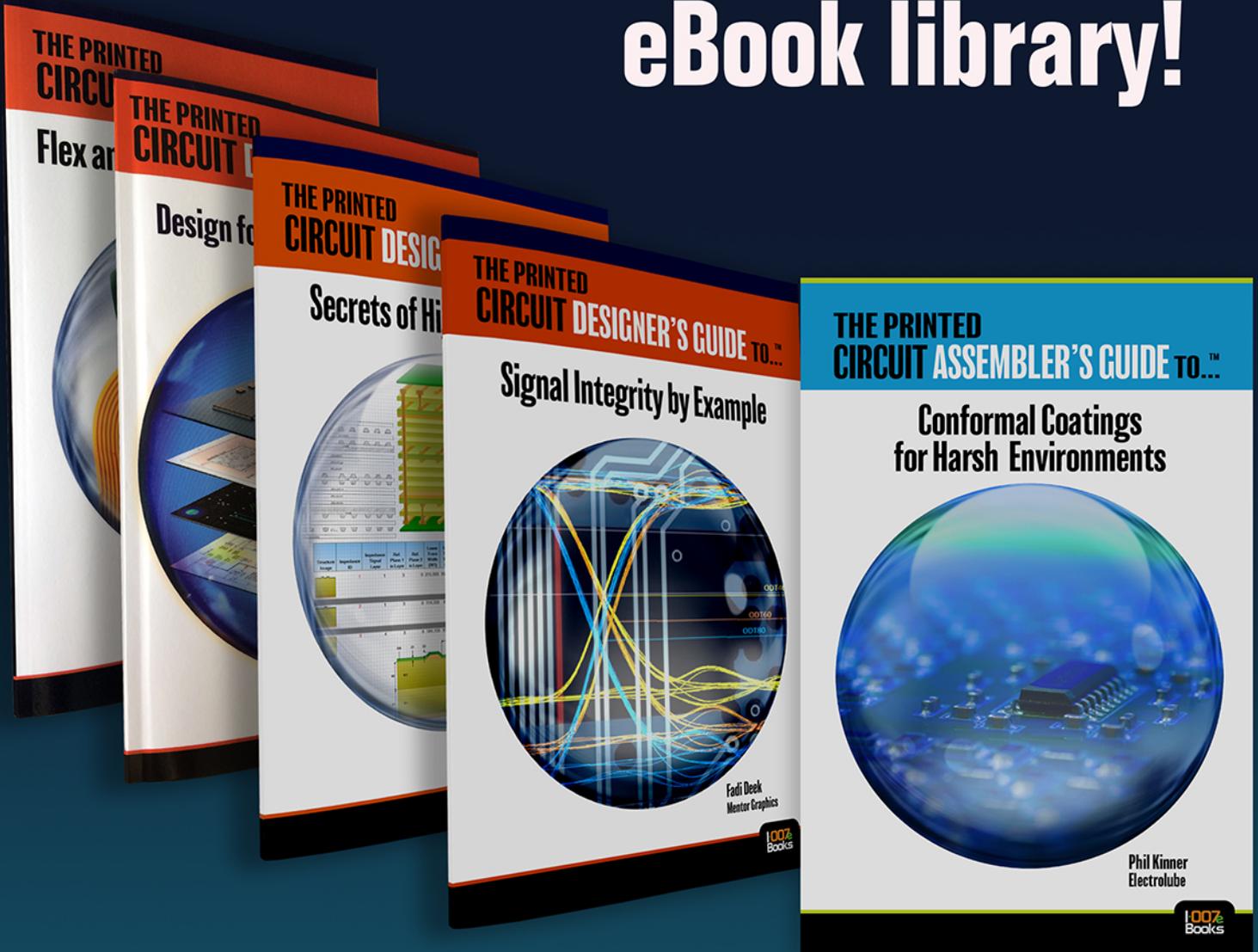
Hence, these design guidelines provide only a short-term solution to address this failure mode. More detailed understanding of the mechanisms driving this failure mode and how to control them are needed to develop a long-term solution that can allow implementation of these mixed VIPPO designs.

Future Work

As discussed in this paper, this work has helped to establish PCB design guidelines and best practices in order to prevent this defect



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from occurring in new product designs. However, there are also other approaches being investigated as potential mitigation strategies that directly address the theorized root cause by employing innovative assembly processes. Positive results have been demonstrated thus far, and more data is being generated before pursuing publication of this work.

Acknowledgements

The authors would like to thank our managers, Scott Priore, Sadanand Patil and Roberto Recca for their support of this work. We would also like to acknowledge Passawee Reaungart from Celestica Thailand for her collaboration and support of these investigations. **SMT**

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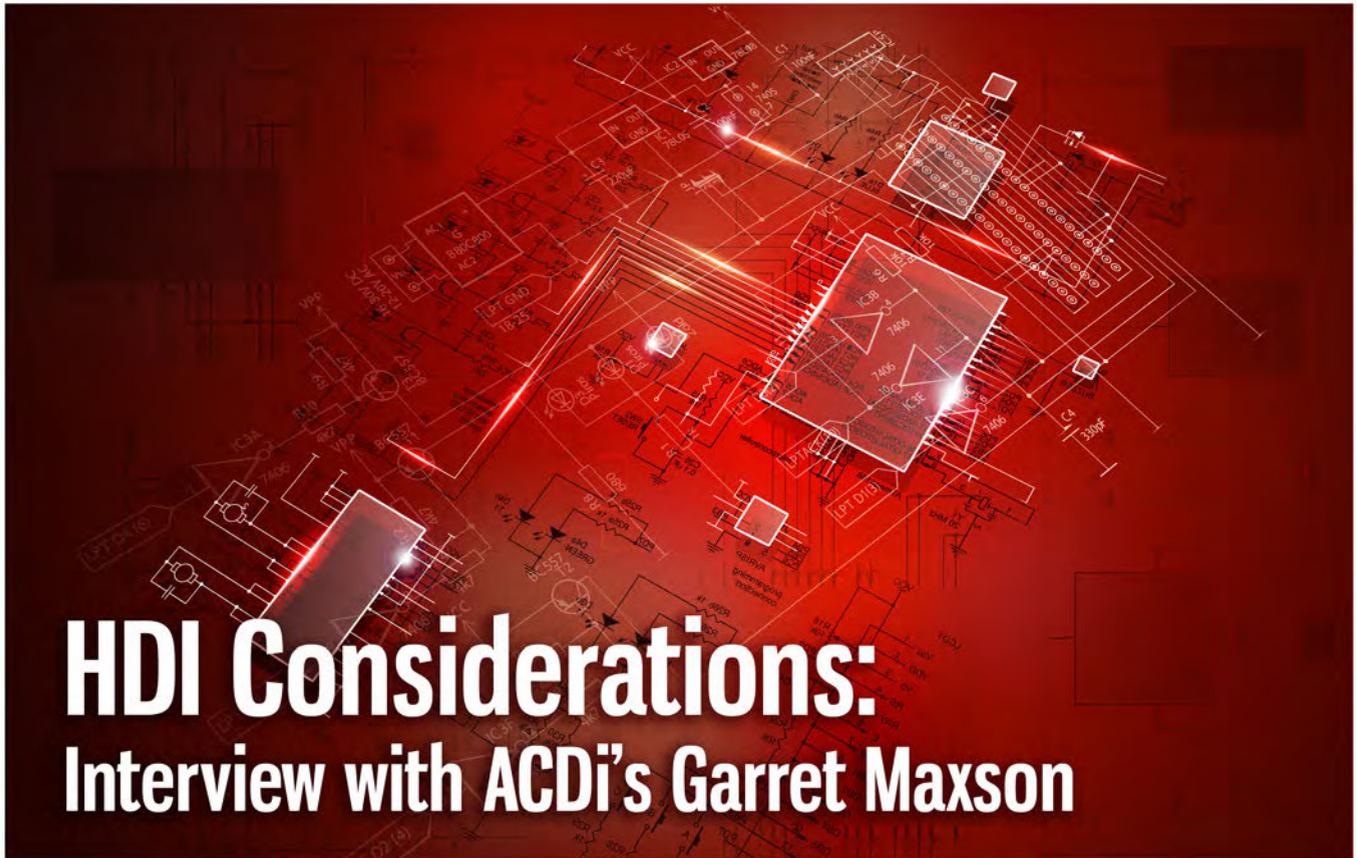


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HDI Considerations: Interview with ACDi's Garret Maxson

by **Stephen Las Marias**
I-CONNECT007

American Computer Development Inc. (ACDi) started approximately 30 years ago as a PCB design and layout service bureau. Today, the company does about 350 to 400 unique PCB layouts per year for a variety of customers across different industries, including medical and industrial fields.

Around 15 years ago, ACDi acquired a local manufacturing plant, enabling it to ramp up into design, layout, and prototype assembly. Five years ago, the company purchased another facility in North Carolina for production-type runs.

Garret Maxson is the manager of engineering services at ACDi. He currently oversees 11 direct reports, and most of them are PCB layout designers, AutoCAD drafters, and component librarians. In this interview Maxson discusses the PCB assembly challenges when dealing with high-density interconnect (HDI) boards, parameters to consider, and strategies to help facilitate a smooth assembly process when using HDI boards.

Stephen Las Marias: What are the challenges in PCB assembly when it comes to dealing with HDI boards?

Garret Maxson: As the boards get denser and denser, obviously we get into high-density interconnect boards. There are a variety of via structures due to the pitches of the parts, and how small the IC manufacturers are making them. What that often leads to is new via technologies, whether they're buried vias or blind vias, or microvias—a lot of companies will start putting them in the pad, which can lead to issues if the assembly is not done properly. When you put a via in a pad that is going to get soldered, you typically want to fill that via, with either a non-conductive or conductive epoxy, and use some sort of plating over the barrel of the via so that you get a smooth pad that you are assembling the part to without a whole lot of surface deviation. The flatter the pad, the easier it is to print solder on the board, and to assemble the part.

As it pertains to assembly, the via-in-pad is one of the larger concerns of the HDI. Other than that, you are mostly concerned with the

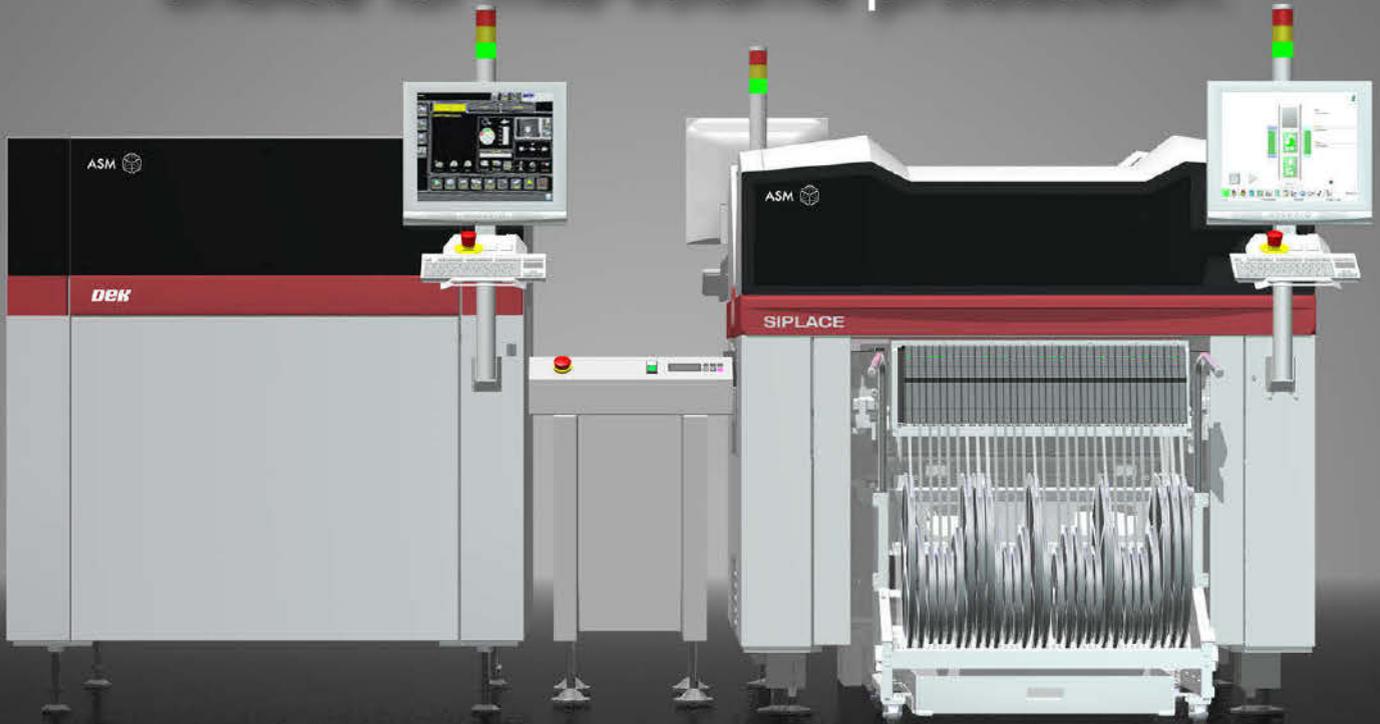


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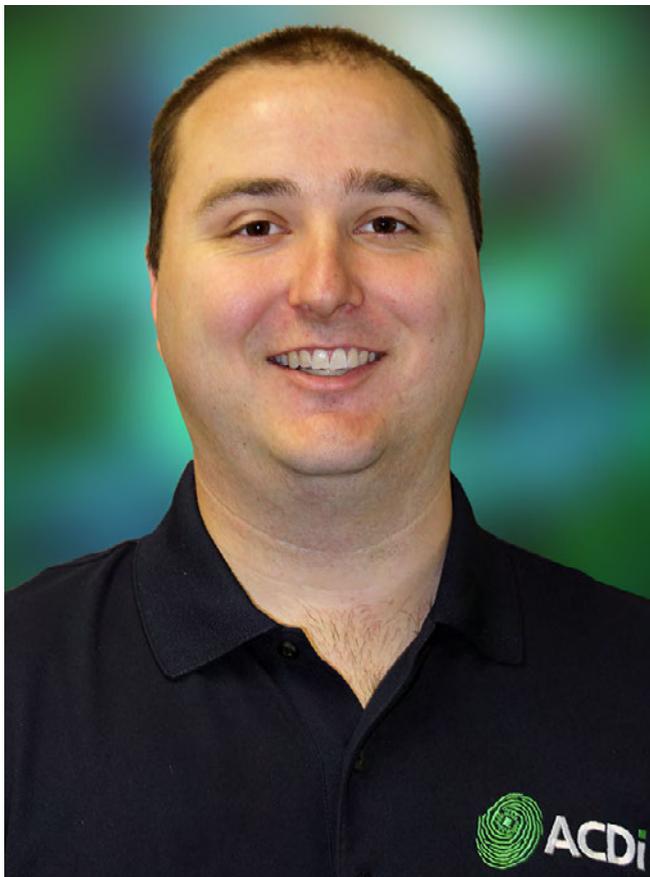
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Garret Maxson

HDI boards in the fabrication level of the bareboard. Obviously, you are driving up the complexity of the board, the cost of the board, with the different lamination cycles and drill passes and so forth. From the assembly standpoint, we are mainly dealing with the top and the bottom of the board—what's going on in the middle of the board doesn't have a huge effect on us.

The number one concern we would have, because of the HDI boards, is that designers are going to put the vias in the pads, so you've just got to make sure that they are filled and plated over to facilitate a smooth assembly process.

Las Marias: Are there key considerations or parameters to ensure successful assembly with HDI boards?

Maxson: Yes. There are a variety of different vias, and IPC-4761 specifies the seven types of via plugging process. Obviously, there's always

a trade-off. The assembly house wants you to fabricate the boards with the most assembly options to make their lives easier; and obviously the customer wants to use the cheaper option, so there's kind of a tradeoff there. You try to find somewhere in the middle where the customers will be willing to pay for a middle-of-the-road option.

Las Marias: Has there been an increase in the use of HDI?

Maxson: There has certainly been an increase. The industry is getting smaller and tighter, and they are trying to fit more and more into smaller boards, which leads the designer to having to use these new via topologies and high-density interconnects just to be able to fit everything into the board that the electrical engineers would like to have specified on the layout. Weight is another thing. The smaller and lighter the board, anything in flight applications where poundage is money, correlates there.

Las Marias: With HDI, will customers wind up with lower cost?

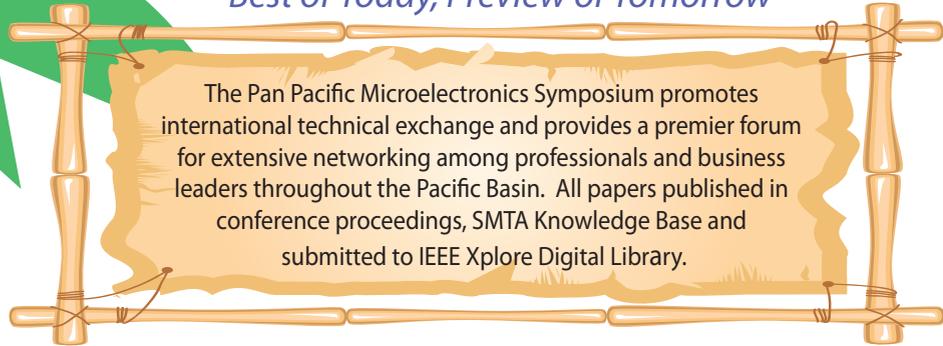
Maxson: Your bareboard will cost more there. Anytime you do an HDI, you got to pay for it to get smaller and tighter. There's a couple different options when you're going to HDI board, whether it's buried vias or blind vias, or microvias. In blind vias, you typically are doing, for instance, when you need more routing room and there's too many signals on the board, and frees up routing channels on the opposite side of the board. The buried vias are what you typically see employed with microvias on a dense placement where you are trying to fit too many parts on the board. What that will do is let you stand up the parts without interfering with what's on the opposite side of the board. If we have a dense placement board, we end up with buried vias; with dense routed boards, we end up with blind vias.

Las Marias: How often do designers discuss the design with the assemblers to have the best layout for assembly when dealing with HDI boards?

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Maxson: Anytime you had a component that you are going to be designing the layout for, you consult the SMT engineers, with respect to the footprint. We consult regularly with our in-house SMT engineers. A kind of a perk of having inhouse manufacturing is we can bounce ideas off them. And you will see most of the package types before, so they will have recommendations as to how we can adjust the artwork at the layout level, so it helps us facilitate a smoother assembly process, or help improve their yield. A strong line of communication at the upfront design level between our design group and our SMT engineers help ensure a reliable design making it out to the manufacturing floor, and improved product yield.

Las Marias: One of the problems with assemblies on HDI boards is the limited access to in-circuit tests. How do you address that?

Maxson: We see less and less request for ICT test with the emergence of flying probe technology. We have an in-house flying probe tester that we use, that the requirements for laying out the board for a DFT standpoint is drastically reduced. You go from needing a 25-mil round target pads for ICT fixtures down to 4-mil round pads for the flying probe. From a DFT standpoint, obviously the flying probe works great for your prototype runs, but you still need

to get that production type run where ICT still has the niche. And as far as designing an HDI board for that, you are going to run into space constraints. There's not as much space on the board, so you may have not as much nodal coverage as you would typically do on an ICT fixture.

You must have a certain amount of space between the probe and, if your whole exercise is making the boards smaller and more compact, obviously you are going to have to sacrifice somewhere. And that sacrifice is usually the smaller nodal coverage percentage.

Las Marias: Is there anything that we haven't talked about that you think we should be talking about?

Maxson: I think from a layout perspective, it really comes down to whether someone is running out of routing room or running out of placing room; that kind of dictates which interconnects we use, whether it's blind, buried, or microvias. With pitches of the ICs, when you get down to below a 0.65 mm pitch part, you tend to have to get creative with your HDI.

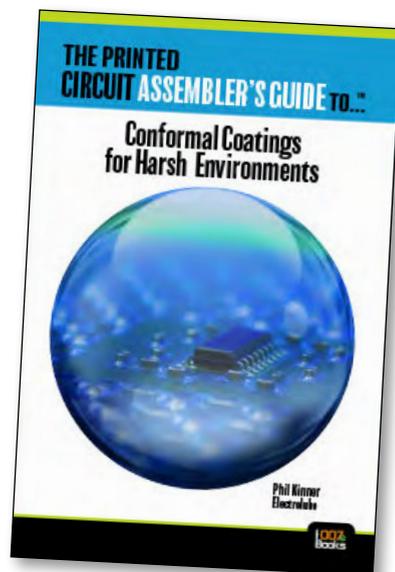
Las Marias: Great, thank you very much Garrett.

Maxson: Thank you. SMT

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Optimal Electronics Sets Sight on Growth

by **Stephen Las Marias**

I-CONNECT007

At the recent NEPCON South China event in Shenzhen, I interviewed Dr. Ranko Vujosevic, CEO and CTO of Optimal Electronics, to learn more about the latest technology developments at his company, and his plans to sustain growth. We also talked about his presentation on lights-out electronics assembly, the technologies that would support this vision, and the ultimate goal of Industry 4.0.

Stephen Las Marias: Dr. Vujosevic, please tell us more about Optimal Electronics and your role in the company.

Dr. Ranko Vujosevic: I founded the company in 1996. I worked as a research scientist at the University of Iowa, and I wanted to have my own company to develop software in one of the industrial engineering areas. Around that time, I was approached by Rockwell Collins plant in Cedar Rapids, Iowa, to design a production scheduling software for their new SMT lines. They funded my development, and then I decided to dedicate all activities towards electronics assembly, and that's how we started it. We market ourselves as a provider of smart software solutions for electronics assembly, not only manufacturing execution systems (MES), because we provide more than what a typical MES provides, including dynamic production scheduling and machine optimization. Recently, we became in-



Dr. Ranko Vujosevic

involved in Industry 4.0 and smart factory solutions, robotics, and artificial intelligence. We are now located in Austin, Texas. In 2003, Flextronics and National Instruments plants in Austin bought our software and instead of traveling often away from my family, I just moved the company to Austin.

Las Marias: What are your plans for the China market?

Vujosevic: Our plan for this year was to expand our markets by establishing distribution channels in Europe, China, and South East Asia. We had been focusing mostly on the United States and Mexico, with some Asian customers—but only American companies with plants in Asia. We already signed a distribution agreement for Europe, and we expect to sign agreements for China and South East Asia in October. China expansion is very important for us, and we are working very hard to establish our presence in China and provide local sales and support within a few months. I came here to present my paper and to meet several companies for

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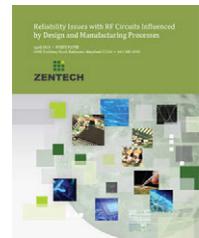
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a potential distribution partnership. I am very happy with the amount of relationships I established here this week.

Las Marias: What took you so long to consider Asia and China?

Vujosevic: We tried China about 10 or 12 year ago, but we didn't have a good experience, let's put it that way. We didn't have a really good experience talking to companies and I was discouraged. We decided we didn't want to do it, so we settled for the U.S. and Mexico market. But right now, things are a little bit different. Things are a little bit more professional everywhere, and we think we can develop honest and respectable relationships with companies in Asia—in a sense we know that a partner can trust us, we can trust the partner, but also we can trust our customers. Especially regarding intellectual property, which we guard very strongly, not just in Asia, but in Europe and everywhere else. So we're very careful what kind of partner we pick and what kind of customers we sell to.

Las Marias: Don't you think you might have missed out on the growth surge that happened about a decade ago?

Vujosevic: I don't think so. There are still a lot of companies that can use our smart software solutions and appreciate our outstanding support. We also have solutions no other competitor offers, so there is still a large market for our solutions in China and all of Asia. I am very encouraged with the interest and investment Chinese companies are making into Industry 4.0, and we hope to provide smart software solutions to our customers in China and other countries in Asia.

Las Marias: Dr. Vujosevic, earlier this week you presented at the SMTA technical conference about lights-out electronics assembly. Can you please give us a rundown of the whole presentation?

Vujosevic: First of all, I wrote that paper out of frustration. I'm frustrated that there's not much information about Industry 4.0 as it applies to



Figure 1: Optimal applications in MEMS sensor assembly clean rooms.

electronics assembly. You go to seminars, presentations, conferences, and they all talk about disruption, digitization, big data, and nothing really specific. We've been doing a lot of applications already related to Industry 4.0 for our customers. I wanted to go and present something that will get people's attention and maybe inspire someone to do something real even if that means proving I was wrong.

The ultimate goal of Industry 4.0 is a lights-out factory that can run unattended for extended periods of time. That will give us maximum throughput, save the cost of the labor and energy, and we can better meet customer expectations because there aren't interruptions. That's the final goal. Well, let's then go backwards. How do we get to that point? In my paper, I discuss the technologies you need to use, how all that should be designed, and the current technologies that can support that. Because, I think that we can now create lights-out assembly lines, but only for a specific type of components or machines that can place smaller components. We can now design, for example, a lights-out line for sensor manufacturing. You can't do that for every type of board or component placements because the machine designs don't support that yet.

In the paper, I discussed the steps the industry needs to take to achieve the goal. My goal was not only to present the paper, but also to summarize my thinking, to put it on paper and share with people, but also to have that as a blueprint for my company. And we're now following my paper, pretty much, and developing these things with our customers.

Las Marias: The goal is to have a totally unmanned factory?

Vujosevic: That's going to happen and I know some big companies that are making plans to do that. We know that's going to happen and I'm not, in my paper, talking about any social implications of that, you know, people are go-

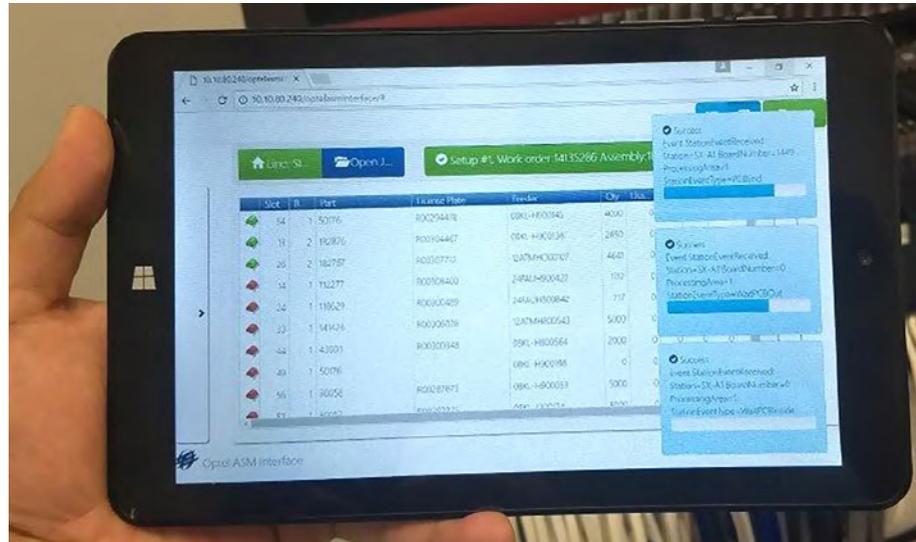


Figure 2: Optimal's focus is on mobile solutions plant-wide.

ing to lose jobs. But that's going to happen no matter what, whether we talk or not. We need to talk about it and prepare people to start training for high tech jobs especially younger generations. You can't hide behind lies that there's not going to be a loss of jobs. It will happen. Operator-free plants will happen soon.

Las Marias: What are the challenges that will be faced by the industry?

Vujosevic: The challenges are making more intelligent equipment designs and standard machine to machine interfaces. Machines don't support operator-free processes right now. The pick and place machines cannot be operator-free because you have to put reel on a feeder, and you have to put the feeder into the slot. A robot cannot do that right now. So, we need to eliminate tapes and feeders, and a different design needs to be in place. That's one challenge. Machines need to be re-designed.

The second challenge is the communications between machines—we need better protocols. They are developing several protocols right now, but everyone has some business interest in the whole process and we are going to end up again with a number of protocols and vendors supporting different protocols. Somehow we will be able to have machines talk to each other, but it's not going to be as simple as people

think or as standard as people think. It never is.

So, those are the two challenges. Social implications are challenging, of course, because if we want to build a plant without people, well, who's going to give you land to build or tax breaks that everybody's asking for these days? It's not going to be from the county or city because you're not hiring anybody. But, some companies can afford to build plants without that, so that will also be part of the decision making.

Las Marias: How should these issues be addressed?

Vujosevic: I think we have everything right now but machine designs. I mean, we have controllers, we have software, and machine to machine communication will happen. We have robots, we have automated guided vehicles (AGVs) that we can control for machine delivery, we have sensors, but the most important problem is that machines need to be re-designed. Because nothing new has happened in this industry for decades. Although, you hear that we lose jobs because of automation. That's not true in the electronics industry. There's no automation at all. Everything is the same as it was 20 years ago.

Now, people are introducing robots, but not in many companies. It's going to happen, but there are some technologies, like cloud computing, that's not going to happen any time soon because of security problems. In the U.S., nobody wants to do anything with that in the manufacturing industry. Okay, you can share iTunes and Amazon stuff, but nobody in the manufacturing industry wants to cloud anything. There are some technologies that are well-developed, but the machine designs are the most critical. They need to re-design the machines to support operator-free operation.

Las Marias: What about the inspection side?

Vujosevic: There are a lot of efforts to provide feedback and feed forward from inspection. Koh-Young is doing some really good stuff about that, for example. Our company now is involved in developing an AI-based system for intelligent process control. Right now, every test machine has some kind of statistical process control and charting, but nobody uses that. It is left to operators to fix the problem and often the easiest fix is to wash the board and do it again without addressing the underlying problem.

You've got an SPI machine and you see the process chart and nobody even looks at that. When there is a problem with the board, they will bring it back to the screen printer and redo it without ever considering what is wrong with the process. What we need an intelligent process control where the system will monitor every test machine, every line, and decide and even predict when a problem will get out of control, or predict a trend, you know, predict the next measurement, next point, and issue alarms or even stop the line. We need that for lights-out electronics assembly, and that can be achieved by an intelligent software. We want to take the operator out of the process control loop and achieve defect free self-correcting lines.

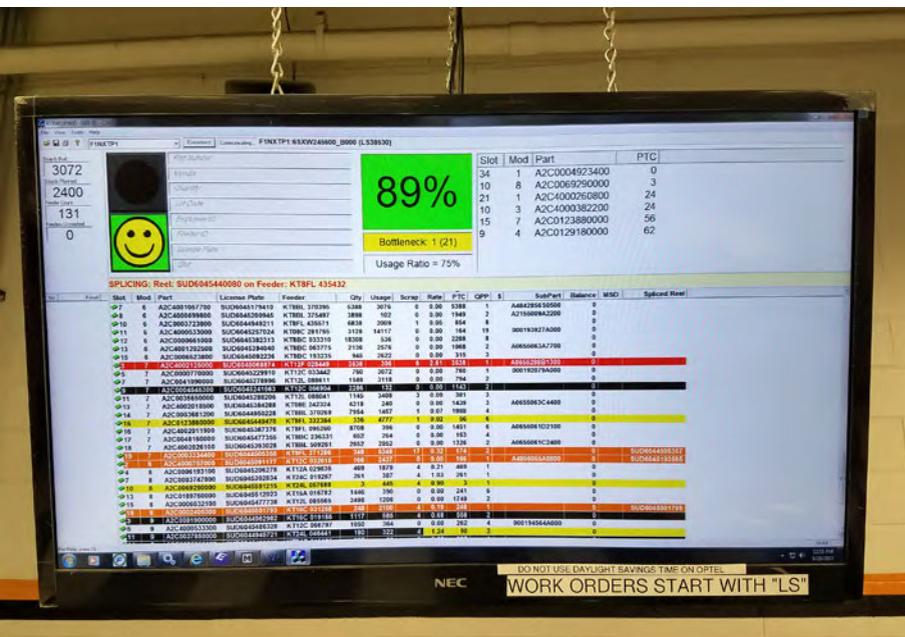


Figure 3: Real-time machine performance monitoring and component traceability data collection.

SEMICONDUCTOR PACKAGING SYMPOSIUM

HETEROGENOUS INTEGRATION – THE ROAD TO IMPLEMENTATION

11.30.2017

NOV. 30, 2017 | SEMI GLOBAL HEADQUARTERS | MILPITAS, CA

SYMPOSIUM 8:00AM - 5:00PM | EXHIBITS 9:30AM - 6:30PM | RECEPTION 5:00PM - 6:30PM

As the growing need to integrate disparate semiconductor technologies in a cost effective way with rapid cycle time and the driving demands of our increasingly connected world, we find many key hurdles in mainstreaming heterogeneous technology packaging solutions. In



KEYNOTE SPEAKER

Wilmer R. Bottoms, Ph.D.

Chairman, Third Millennium Test Solutions
Co-chair, Heterogeneous Integration Roadmap



KEYNOTE SPEAKER

David Armstrong

Director of Business Development
Advantes

Third Keynote to be Announced

particular, this event will explore three issues central to the successful execution of heterogeneous integrated packages:

- Can the packaging community establish a real design for heterogeneous integration ecosystem?
- Should we rethink the reliability standards for these heterogeneous integrated SIP packages?
- What are the best test strategies for these heterogeneous integrations, or at least what are the guiding principles?

The program will include three keynote presentations from industry experts outlining these three issues in more detail, each followed by an interactive panel discussion on these same topics. The panels will be populated with industry experts with diverse and perhaps conflicting views on these important topics.

Be sure to join for what promises to be an exciting and educational day as we debate the issues central to successful heterogeneous integration implementation!

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Las Marias: I think the industry will get there, but it's going to take some time.

Vujosevic: It's going to take some re-designs. The machines have to become smart. In the paper, I discuss how you can use a Windows 10 PC with embedded IoT to control everything about the machine on the line. You don't need to have any MES anymore. It can collect traceability data. It can switch the set up. It can communicate with other machines. It can send a sig-

.....

“ You don't need to have any MES anymore. It can collect traceability data. It can switch the set up. It can communicate with other machines. ”

.....

nal to the material tower to have AGVs bring the new reel, it can control predictive maintenance, and it can even self-schedule, i.e. pick a job available and schedule itself. We need intelligent machines that can do that.

Las Marias: The industry's looking into developing really strong AI capabilities in their machines.

Vujosevic: Right. That's why I was talking about process control. AI can help you because AI and neural networks are good in pattern recognition and classification and prediction. But to be able to achieve that, you need to train them, and you train them with a lot of data. You have data because you are doing the SPC and collecting measurements. So, AI can be really applied to that successfully as well as to predict machine maintenance, where you can collect sensor data and predict when the machines should be maintained instead of using preventive maintenance, which we know doesn't work very well.

Las Marias: Where does Optimal Electronics come into that picture?

Vujosevic: We provide smart software solutions. We have used AI in our production scheduling and pick-and-place machine optimization for past 20 years. We are now using AI for intelligent machine design, intelligent predictive maintenance, intelligent process control, etc.

Las Marias: Do you think companies in Asia and China will be among the first to transition to an Industry 4.0 vision in electronics manufacturing?

Vujosevic: I think so. In the U.S., the biggest companies are interested, and they will do it, or at least try. We have a customer in Texas where they are using AGVs and robots, 3D printing, etc. But that's only a handful of them. Industry 4.0 in the U.S. has had a lot of talk, but not a lot of action. Companies in Asia and China are much more interested in advancing towards real applications than those in the U.S.

Las Marias: What opportunities are you seeing in this region for Optimal Electronics?

Vujosevic: We want to do smart factory solutions. We want to position ourselves as a provider of Industry 4.0 solutions and we want to get away from the MES provider label. We will still deliver MES solutions for some time. We recently hired a robotic expert. We want to provide unique solutions and separate ourselves from traditional MES providers. We've never really fit very well. Although we provide MES solutions, we always try to sell our dynamic production scheduling first, and target customers that we can sell our unique capabilities to, and kind of carve out a little market for us there, which is most often OEMs.

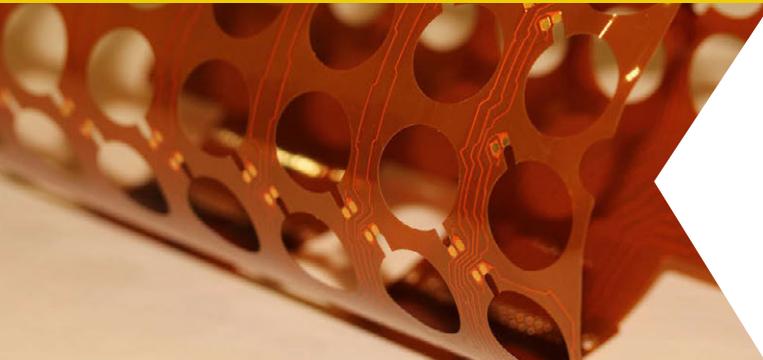
But now, again, we want to also include into that our smart factory solutions and open that market for us. But we are open, of course, to sell traceability solutions to any type of a company, which we do very well.

Las Marias: Traceability is also one of the issues when it comes to these smart factories.

Vujosevic: Yes. But traceability is something you have to do because your customer is asking you,

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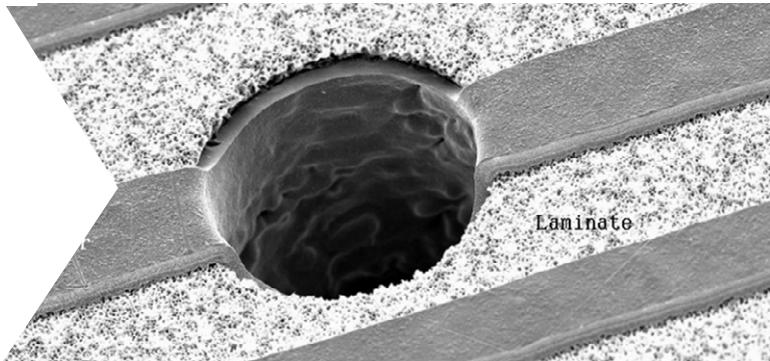
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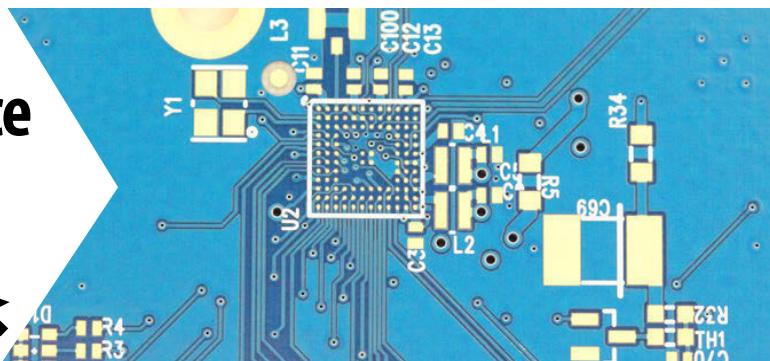
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in most cases. Companies don't like to do traceability, but they don't have a choice. They want a smart factory because it will make them more profitable, it's good for their PR and sales and showing to their customers. So, they like smart solutions better than traceability, but they must have traceability. Our goal is to create smart solutions that will help our customers, or soon people will lose interest in Industry 4.0.

Las Marias: What is your outlook for the electronics assembly industry and your niche in that market this year and the next?

Vujosevic: We are focusing on Mexico, Europe and Asia because we have very good references and happy customers and want to extend our customer base. I don't know about the industry as a whole because the world is not innovating. There's nothing new. Now, we are going to have an iPhone 10. That's not new. It's just bigger and has a better camera. Who cares? We need

a breakthrough. We need some new technology to drive our industry forward. They're talking about AI applications and most people have no idea what they're talking about, but they're talking about it because investors need a new thing. They gave them AI, and they're biting. They're investing money. They have to show good marketable solutions, not gimmicks, or the investors will lose interest soon. So we need better ideas and breakthrough solutions, and they're not happening. They haven't happened for a while. So I don't really know. I'm not very optimistic about the future of this industry unless we come up with some new products. New electronics products that people will buy. There are only so many iPhones we can sell.

Las Marias: Dr. Vujosevic, thank you very much for your time.

Vujosevic: Thank you. **SMT**

How to Tell if You Need PCB Assembly Services

By **Duane Benson**, SCREAMING CIRCUITS

If you're attempting to cross the median of a busy four-lane highway, it's entirely possible that there's a Jersey Barrier in your way. In that particular setting, having something sturdy blocking your way is probably a good thing. On the other hand, I would bet that for the majority of you reading this, there are some barriers around you that you'd much prefer not run into.

Barriers can bring on stress, uncertainty, risk and a general sense of despair. Despair can lead to hopelessness. Hopelessness can lead to you being rolled up in a fetal position under your desk, tangled up in the nest of cables that every good engineer has under their desk. As everyone knows, if you're under your desk tangled in cords and whimpering when your boss walks in the room, you're probably not going to get a Christmas bonus.

If you're still not sure how to remove the barriers in your way, it might be time to ask yourself if you need PCB assembly services. The answer isn't

always yes, nor is it always no. The answer is quite often "it depends."

When in doubt, ask yourself:

- Does it need to be done right?
- Is time a consideration?
- Are there too many placements for you to deal with?
- Are there more than one or two boards?
- Are the parts too small?
- Are there any BGA packaged chips?
- Will it be monotonous?

If you answered yes to any of those questions, you need PCB assembly services. If you aren't in a hurry, the parts are big enough and you're seeking a fun, valuable learning experience—build the boards by hand.

With the impending advent of desktop pick-and-place machines, there will be a few more options, but the basic question will remain the same in any industry. Which do you have more of, time or money?



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Conference

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Strategies for Reducing Product Warranty and Liability Risk in Manufacturing Services Agreements

IPC Members Only

Webinar

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Conference & Exhibition

San Diego, CA, USA

March 1–2, 2018

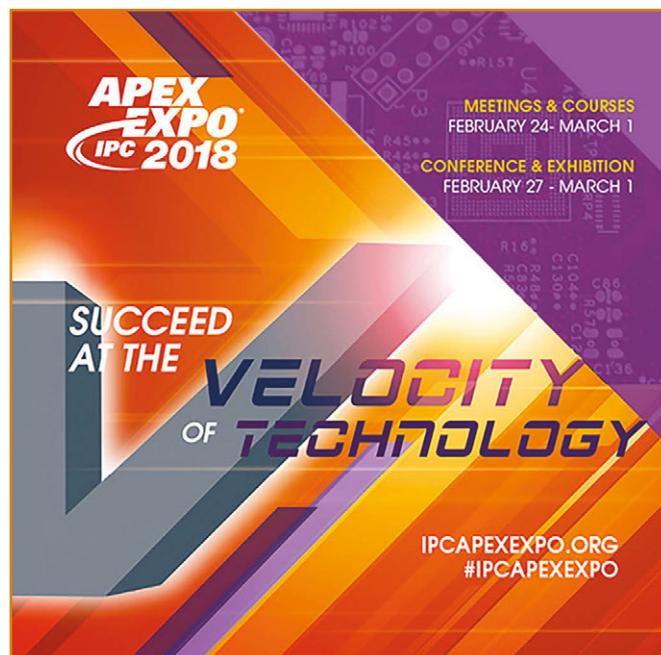
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Meeting

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For more information, visit www.IPC.org/events

TOP TEN



Recent Highlights from SMT007

1 It's Only Common Sense: Finding that Great Salesperson to Sell your CEM Services

"Aren't salespeople alike?" Yes, in some ways they are, but in other ways not so much. Here's what you should look for in a great salesperson.



3 The Root Causes & Solutions for Warped PC Boards

There are two primary types of causes of board warping: process related at the fab or assembly shop, and layout related issues.



2 Update on IPC's Validation Services and Hints of What's to Come

SMTA International is the perfect time to get updates on IPC happenings. At the show, I-Connect007 Managing Editor Patty Goldman caught up with Randy Cherry, IPC's director of Validation Services, to learn more about the latest developments in IPC's Validation Services programs.



4 What's Up in Scandinavia's EMS Industry?

Scandinavia, consisting of Denmark, Norway, Sweden, and Finland, is relatively small in regard to the overall European EMS revenues, and counts for less than 6% of the European EMS production value. Nevertheless, more than 160 companies offer EMS services, not to mention companies who only manufacture cable harnesses or just do design work, box building, and after-sales services.



5 Abstracts Sought for IPC APEX EXPO 2018 in San Diego

IPC—Association Connecting Electronics Industries invites researchers, technical experts and industry leaders to submit abstracts for poster presentations at IPC APEX EXPO, the industry's premier conference and exhibition for printed board design and manufacturing, electronics assembly and test.



6 Celestica Re-Energizes Brand Identity

Celestica Inc.'s renewed brand heralds an exciting new chapter in the company's evolution and represents its commitment to delivering bold solutions to its customers that solve challenges, drive innovation and create value.



7 RTW SMTAI: Gary Tanel Discusses How SMTA Helps the Industry Evolve

Gary Tanel, president of the SMTA Dallas Chapter, speaks with I-Connect007 Publisher Barry Matties on a myriad of topics, including the goal of the SMTA as an industry association, and how it is helping the industry evolve.



8 RTW SMTAI: MIRTEC on Staying Ahead of the Curve

Brian D'Amico, president of MIRTEC, talks with I-Connect007 Managing Editor Andy Shaughnessy about some of the latest 3D AOI challenges, including dealing with highly reflective surfaces of solder joints or wafer-level die, which make it impossible to characterize in 3D.



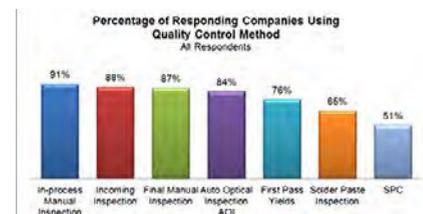
9 SMTA International 2017 a Success

The 2017 SMTA International Conference and Exhibition, which took place September 17 – 21, 2017 at the Donald E. Stephens Convention Center in Rosemont, Illinois, concluded successfully. A record number of international attendees from 22 countries were registered this year.



10 IPC Releases 2017 Quality Benchmark Study for Assembly

IPC's Study of Quality Benchmarks for Electronics Assembly 2017 is now available. The annual study provides valuable benchmarking data to electronics assembly companies interested in comparing quality measurements to industry averages.



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The I-Connect007 China team is seeking an experienced salesperson to generate and manage a revenue stream for our Chinese publications.

Key Responsibilities include:

- Sell advertising contracts for monthly magazine
- Develop and cultivate new business
- Keep timely and accurate records
- Generate and follow up on all leads
- Manage contract renewals
- Account management: work with local and international team to provide customer support
- Phone and email communications with prospects
- Occasional travel

Qualifications

Successful candidates should possess a university degree or equivalent, experience with managing and cultivating leads, projecting, tracking and reporting revenue. We are looking for positive, high-energy candidates who work well in a self-managed, team-based, virtual environment.

Compensation

This is a base salary-plus-commission position. Compensation commensurate with experience.

Requirements

- Must be located in China Mainland, South China area preferred
- Good command of Chinese language, proficient with English speaking and writing
- Able to follow established systems and learn quickly
- Able to maintain professional external and internal relationships reflecting the company's core values
- 2-5 years' sales experience
- Experience with Microsoft Office products
- Must be highly motivated and target-driven with a proven track record for meeting quotas
- Good prioritizing, time management and organizational skills
- Create and deliver proposals tailored to each prospect's needs
- Experience in the electronics industry desirable

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PCB Assembly Supervisor— full time Accurate Circuit Engineering— Santa Ana, CA

Position Summary: Responsible for all assembly processes to ensure continued growth as directed by management.

Essential Job Functions:

- Create, implement, and supervise in-house manufacturing facility
- Recruit, hire, train, and supervise assembly floor personnel
- Extensive hands on experience with all aspects of PCB assembly
- Understanding of IPC-A-610 standards
- Research and acquire additional assembly resources
- Gather data on product shortages, lead times, price changes, etc.
- Coordinate the assembly activities with sales to ensure 100% on-time delivery
- Create, implement, and supervise daily quality processes to ensure 100% accuracy
- Document, monitor and review progress of the business unit
- Respond to internal and external customers in a timely manner
- Coordinate walk-through, site audits, etc.

Qualifications:

- Minimum 3 years as operations supervisor of electronics assembly house
- 5+ years' experience in the electronics industry
- Previous experience as a quality or operations supervisor preferred
- Ability to solve practical problems using pre-established guidelines
- Strong facility in Microsoft Office applications
- Excellent verbal and written communication skills
- Ability to work with people of diverse backgrounds
- Highly organized/excellent time management skills
- Ability to perform at the highest level in a fast-paced environment
- Valid California driver's license.

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PCB Process Planner

Accurate Circuit Engineering (ACE) is an ISO 9001:2000 certified manufacturer of high-quality PCB prototypes and low-volume production for companies who demand the highest quality in the shortest time possible. ACE is seeking a skilled individual to join our team as a PCB process planner.

Responsibilities will include:

- Planning job travelers based on job release, customer purchasing order, drawings and data files and file upon completion
- Contacting customer for any discrepancies found in data during planning and CAM stage
- Consulting with director of engineering regarding technical difficulties raised by particular jobs
- Informing production manager of special material requirements and quick-turn scheduling
- Generating job material requirement slip and verify with shear clerk materials availability
- Maintaining and updating customer revisions of specifications, drawings, etc.
- Acting as point of contact for customer technical inquiries

Candidate should have knowledge of PCB specifications and fabrication techniques. They should also possess good communication and interpersonal skills for interfacing with customers. Math and technical skills are a must as well as the ability to use office equipment including computers, printers, scanners, etc.

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The application engineer is the first contact for our customers who have technical questions or issues with our product. We value our customers and wish to provide them with highest quality of technical support.

Key Responsibilities:

- Support customer base through a variety of mediums
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- Create various types of topic based content, such as online help, online user guides, video tutorials, knowledge base articles, quick start guides and more
- Distill complex technical information into actionable knowledge that users can understand and apply
- Continually develop and maintain product knowledge

Requirements:

- Understanding of EDA electronic design software, schematic capture and PCB layout software
- Bachelor's degree in electronics engineering or equivalent experience
- Sales engineering and/or support engineering experience
- Circuit simulation and/or signal integrity experience
- Understanding of ECAD/ MCAD market segments
- Understanding of micro controllers, SoC architecture and embedded systems market
- Database experience preferred (i.e., MySQL, PostgreSQL, Microsoft Access, SQL, Server, FileMaker, Oracle, Sybase, dBASE, Clipper, FoxPro) etc.
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- Preparing quotes to modify, rebuild, and/or repair Chemcut equipment

Requirements:

- Associates degree or trade school degree, or four years equivalent HVAC/industrial equipment technical experience
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- Experience with single and three-phase power, low-voltage control circuits and knowledge of AC and DC drives are desirable extra skills

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Duties include:

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- Initial customer contact (cold calling)
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
 - Market and product
 - Circuit types used
 - Quantity and delivery requirements
 - Competitive influences
 - Philosophies and finance
 - Quoting and closing orders
 - Bonding
- Submitting quotes and sales orders
- Providing ongoing service to the customer
- Problem solving
- Developing customer information profiles
- Developing long-term customer strategies to increase business
- Participate in quality/production meetings
- Assist in customer quality surveys
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The technical content specialist will:

- Assist in the development of key content and ensure consistency of message and format across platforms
- Develop a technically-detailed understanding of Indium Corporation materials and offerings to the SAAM industry
- Curate a library of technical conference papers and associated materials, including content related to Indium Corporation materials and their performance
- Assist in the development of, and ensure consistency for SAAM promotional materials, such as product datasheets (PDS), images, brochures, whitepapers and presentations (technical and sales)
- Attend at least one technical conference and its paper session per year

Requirements:

- Technical undergraduate degree (BS in Chemistry/Physics/Metallurgy/Materials Science or Engineering discipline)
- 5 years of work experience in semiconductor assembly or advanced electronics assembly
- Excellent written and spoken English language skills; fluency in Chinese desirable
- Proven ability to work independently with verbal or written instructions

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This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

Required Skills:

- BA/BS degree-desired, in a technical area is preferred
- Two years of outside/inside sales or manufacturing experience in the PCB manufacturing environment is desired
- Self-motivated self-starter with the ability to initiate and drive business with little supervision
- Independent worker with a strong commitment to customer satisfaction
- Understanding of consumable sales process
- Ability to organize activities and handle multiple projects simultaneously with effective and timely follow-up
- Ability to solve problems and make decisions for which there are no precedents or guidelines and be resourceful in nature
- Positive attitude while operating under pressure and be an independent problem-solver
- Computer skills in Windows, Outlook, Excel, Word and PowerPoint
- Must have a valid driver's license with good driving record

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Western Regional Equipment Service Technician

Technica, USA, a Western regional manufacturer's representative/distributor has an opening for an equipment service technician covering the Western USA, including but not limited to, California, Oregon, Washington, Utah, Colorado, and Arizona. The position will be responsible for servicing our PCB fabrication equipment product line, including installation, troubleshooting, repair service, rebuild service, etc. This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

Key responsibilities are to install and service equipment, conduct equipment audit, and provide technical service when appropriate to solve problems.

Required Skills:

- 2+ years of experience in a PCB manufacturing environment or similar
- Willingness to travel
- Positive "whatever it takes" attitude while operating under pressure
- Self-motivated self-starter with the ability to initiate action plans
- Ability to work independently with a strong commitment to customer satisfaction
- Excellent communication and interpersonal skills
- Strong ability to use all resources available to find solutions
- Computer skills with ability to write detailed service and equipment reports in Word
- Understanding of electrical schematics
- Able to work in and around equipment, chemical, and environmental conditions within a PCB manufacturing facility

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IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

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Experienced PCB Sales Professional

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. Prototron of Redmond, Washington, and Tucson, Arizona are looking for an experienced sales professional to handle their upper Midwest Region. This is a direct position replacing the current salesperson who is retiring after spending ten years with the company establishing this territory.

The right person will be responsible for all sales efforts in this territory including prospecting, lead generation, acquiring new customers, retention, and growth of current customers.

This is an excellent opportunity for the right candidate. Very competitive compensation and benefits package available.

For more information, please contact Russ Adams at 425-823-7000, or email your resume.

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Process Engineer (Redmond, Washington)

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. We are looking for an experienced PCB process engineer to join the team in our Redmond, Washington facility. Our current customer base is made up of forward-thinking companies that are making products that will change the world, and we need the right person to help us make a difference and bring these products to life. If you are passionate about technology and the future and believe you have the skills to fulfill this position, please contact Kirk Williams at 425-823-7000 or email your resume.

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Events

For IPC's Calendar of Events, click [here](#).

For the SMTA Calendar of Events, click [here](#).

For the iNEMI Calendar, click [here](#).

For a complete listing, check out [SMT Magazine's full events calendar here](#).

[PCB Carolina 2017](#)

November 8, 2017
Raleigh, North Carolina, USA

[productronica 2017](#)

November 14–17, 2017
Munich, Germany

[HKPCA/IPC International Printed Circuit & South China Fair](#)

December 6–8, 2017
Shenzhen, China

[47th NEPCON JAPAN](#)

January 17–19, 2018
Tokyo Big Sight, Japan

[DesignCon 2017](#)

January 30–February 1, 2018
Santa Clara, California, USA

[EIPC 2018 Winter Conference](#)

February 1–2, 2018
Lyon, France

[IPC APEX EXPO 2018 Conference and Exhibition](#)

February 27–March 1, 2018
San Diego, California, USA

[China International PCB & Assembly Show \(CPCA Show 2018\)](#)

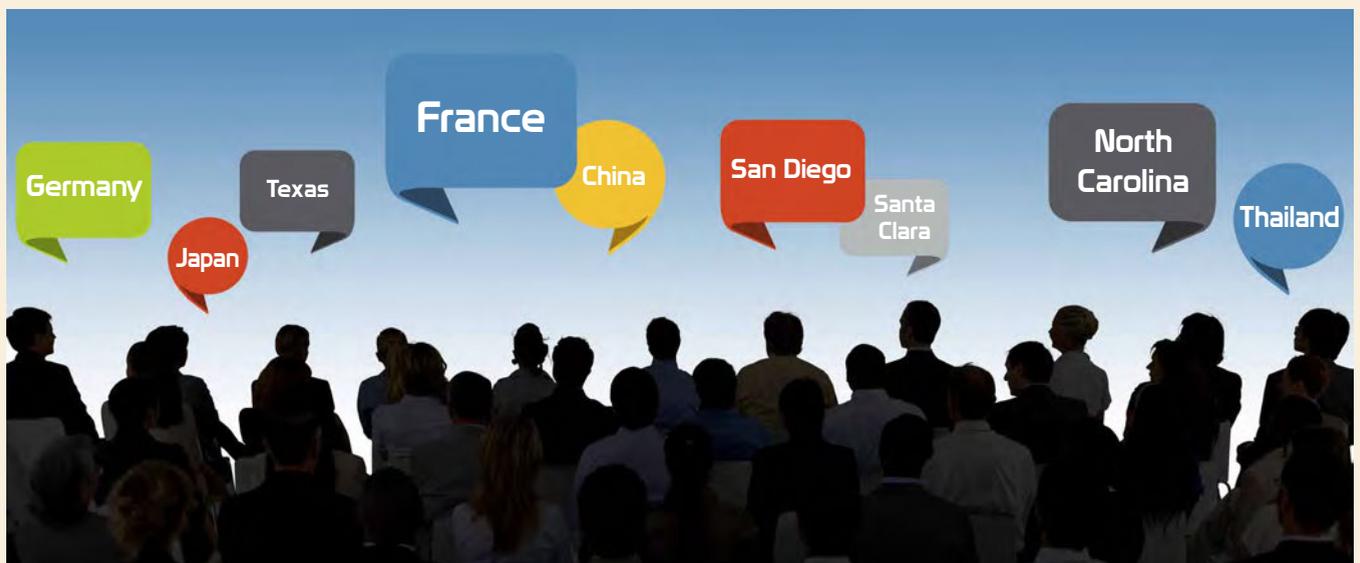
March 20–22, 2018
Shanghai, China

[PCB EXPO Thailand](#)

May 10–12, 2018
Bangkok, Thailand

[Medical Electronics Symposium 2018](#)

May 16–18, 2018
Dallas, Texas, USA



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