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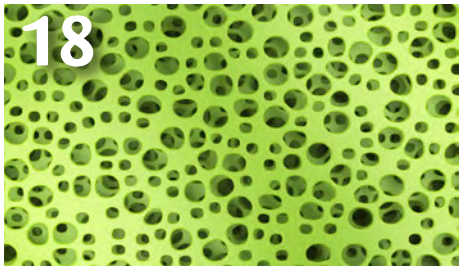

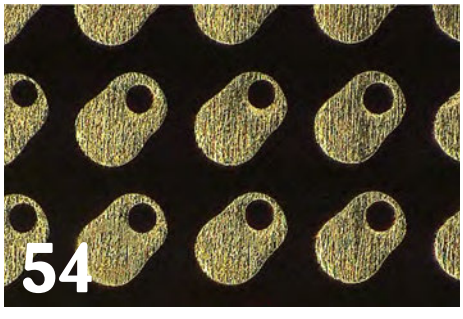

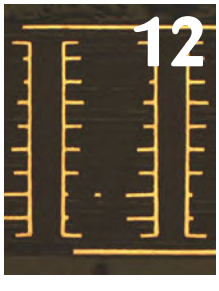

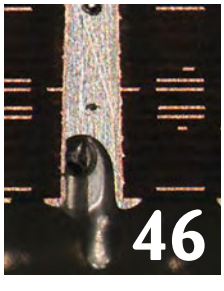

Vias and More Vias!

Blind, buried, landless…IPC defines no less than seven types of vias. This month, our experts shed light on the many different types of vias, their functions, and the various challenges associated with them.

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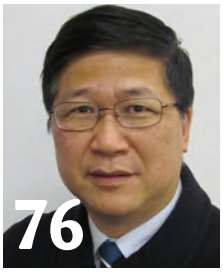

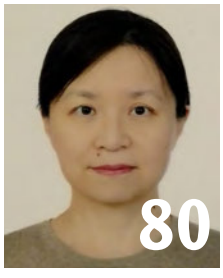

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Everything You Want to Know about Vias but Were Afraid to Ask

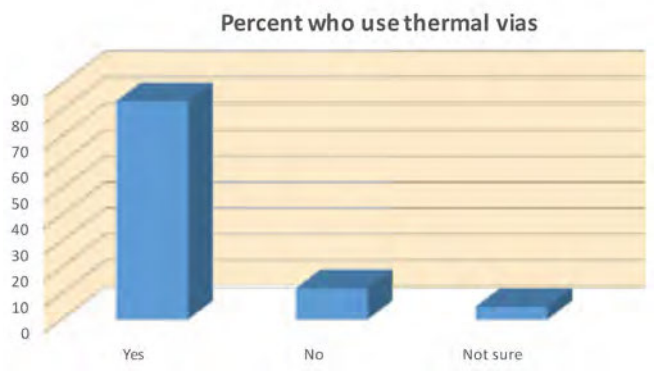
by Patty Goldman
I-CONNECT007

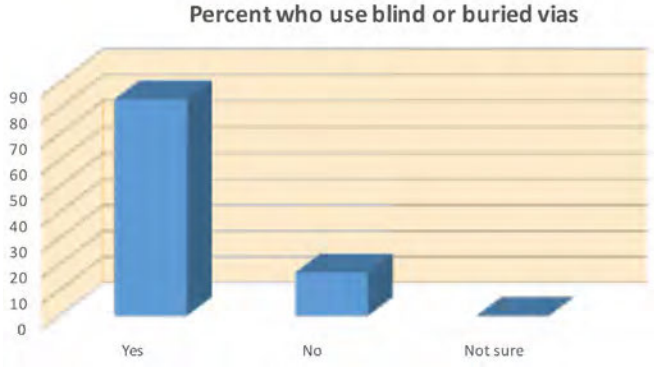
"Via" is one of those words appropriated by our industry and completely redefined—one of hundreds, I believe (think of mouse bites, tombstones, etc.). In my mom's old Funk and Wagnall's Dictionary (1968), "via" is defined as a preposition: "By way of; by a route passing through." Merriam-Webster online today has the same basic definition: "By going through… By way of (a particular place)." Not a noun as we so blithely use it and not a thing about very small holes and electrical connections. But in our industry, IPC defines no less than seven types of vias (a noun!). (See Keith Sellers' column for those.)

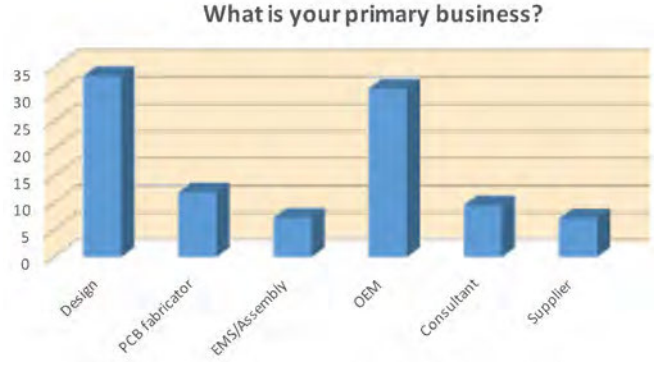
Regarding our survey on vias, almost 85% of our respondents said they used blind/buried vias. And since 15% of those answering were either suppliers or consultants, it seems that approximately 100% use the B/Bs. OK then, on to a tougher question. We then asked how often, and it turns out that "use" covers everything from rarely to pretty much all the time, with a definite undercurrent of "because we have to." When asked about thermal vias, over 82% of respondents said they use them and nearly as many expect to see increasing numbers of them, as one person noted, "Absolutely. ICs are getting smaller and hotter."

We asked several other open-ended questions, including, "What are the greatest challenges you face when it comes to vias?" The number of different responses was widely varied and seemed to cover everything: impedance match, routing density, aspect ratio, annular ring, DFM, diminishing pad size, cost efficiency, tenting, filling, via-in-pad, CAF concerns, signal integrity, plating, equipment, reliability concerns… And of course, density, density, density.

We also asked, "What are the greatest challenges in back-drilling your vias?" We received many different answers here, too: not enough internal copper clearance, thickness variations, alignment of primary drill to backdrill, stub length tolerance, machine precision, spacing, via integrity, processing time, and finally, "the solution is to avoid back drilling." Ouch, I think back-drill is a pain point.







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In a final question, we asked, "Are you aware of landless vias?" About 57% of respondents answered yes, which was good news considering we published an article on that subject just a few months ago. More interesting was the follow-up response on how often they were used. Roughly 95% said never, with a few mentioning ongoing evaluations and several bringing up reliability concerns. I personally know of two PCB facilities that can absolutely produce reliable landless vias based on their internal process. It's easy if you have the right process.

Now on to our lineup this month. As I mentioned, Keith Sellers of NTS-Baltimore leads our discussion with a wonderfully detailed explanation of vias in his column. He includes plenty of photos and clearly explains the difference between blind and buried vias.

He is followed by none other than the father of HDI, Happy Holden, who writes on four old ideas for increasing density on a PCB—all involving vias. He then delves into each and provides highly detailed explanations including layout and manufacturing processes. While the discussion may seem overwhelming, as always, there is much useful information within. Dig in.

The bailiwick of RBP Technology's Mike Carano is troubleshooting and electroplating, no doubt about it. This month he turns his attention to drilling through-holes (aren't these vias, too?), reviewing mechanical drilling basics while pointing out potential causes for problems down the line.

There is no doubt that advances in laser technology have been a big facilitator for smaller vias and finer features. Spectra Physics' Jim Bovatsek provides us with a thorough overview of laser technology as it relates to vias, microvias, and things like patterning in flex coverlay.

We are happy to have an excellent paper originally from IPC APEX EXPO 2016, written by Amphenol's Cynnthia Verbrugge, et al., which presents a unique packaging solution for a server involving a loose-leaf rigid-flex circuit board with backdrilling and LGA interconnect. The profusely illustrated article includes details from initial concept through design and build and onto qualification and full production.

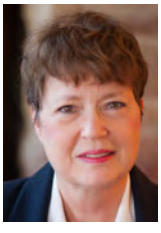
As I mentioned, lasers have become a necessity for microvia processing, as well as for flex circuit manufacture. In this month's Laser Pointers column, Mike Jennings and Patrick Riechel of ESI provide a step-by-step guide for installing laser equipment, from transportation and initial setup through verification testing and initial operation.

And now on a rather sad note, we include Karl Dietz's very last regular column, number 225. Karl has been such a (wonderful) fixture in our magazine and we will certainly miss his insight into so many varied subjects. He promises to be back on occasion; I truly hope that he finds many topics to pique his interest and inspire him to write more columns over the next years. Thanks so much, Karl. We will miss you!

And that brings us to Barry Lee Cohen and his latest Launch Letters. This month, Barry writes about trade shows—appropriate as the season is almost upon us. He offers much useful and expert advice on graphics as well as other media for your booth. I can fully attest to Barry's expertise, having worked with him for several years at Enthone. His suggestions are well worth following.

And there you have it. Much meat for the techies plus some tidbits for others in your organization. Want more assembly-related info? Then by all means check out *SMT Magazine*. Looking for articles and info on PCB design? Then open a few issues of *The PCB Design Magazine*.

Next month our topic is sales and marketing. We will be bringing you insightful articles and columns to help get you ready for the New Year. Hit this subscribe link to get any or all of these magazines delivered right to your email inbox—and while there, make sure you are getting our Daily Newsletter as well. See you all next month! **PCB**



Patricia Goldman is a 30+ year veteran of the PCB industry, with experience in a variety of areas, including R&D of imaging technologies, wet process engineering, and sales and marketing of PWB chemistry. Active with IPC since 1981, Goldman has chaired numerous committees and served as TAEC chairman, and is also the coauthor of numerous technical papers. To contact Goldman, click here.

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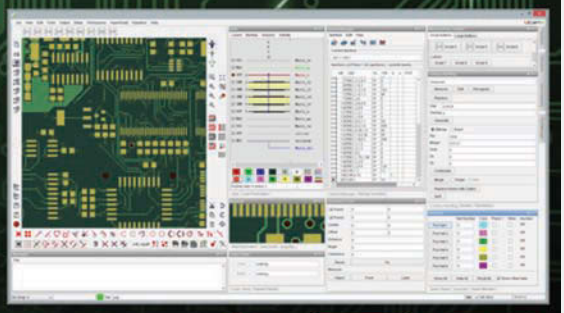

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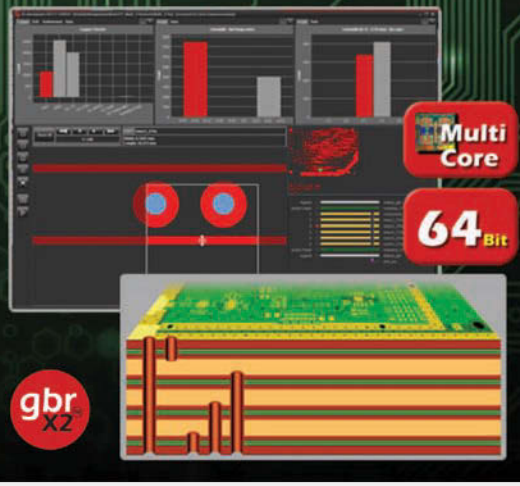

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Vias for Dummies

by Keith M. Sellers
NTS-BALTIMORE

In simple terms, a circuit board is but a composition of things designed to be connected and not. The number of layers and number of connections make no real difference as the geometry shapes the landscape. The via is but one tool that helps in building the wonder that is a printed circuit board, and in this column, we'll discuss the via in relation to the variety of types available for use as well as some of the testing that can be performed on them to ensure their reliability.

A small—sometimes very small—yet important part of the circuit board landscape, the via, by definition, is simply the means by which layers of the board can be interconnected. What differentiates the via from a plated through-hole is simply the fact that nothing (i.e., a component lead) will get inserted and possibly soldered into the structure. Further, vias don't have to extend from one side of the board to the other, although they certainly can as a through via. Blind vias start at the surface on one side of the board but don't extend to the other side, while buried vias (Figure 1) are completely encapsulated within the board with no end extending to either surface of the board.

From there, IPC has defined seven types of vias. From IPC-T-50M[1], Terms and Definitions for Interconnecting and Packaging Electronic Circuits, these types are identified and described as follows:

- **Type I**—Tented: A via with a mask material applied bridging over the via wherein no additional materials are in the hole
- **Type II**—Tented and Covered: A Type I via with a secondary covering of mask material applied over the tented via
- **Type III**—Plugged: A via with material applied allowing partial penetration into the via (Figure 2)

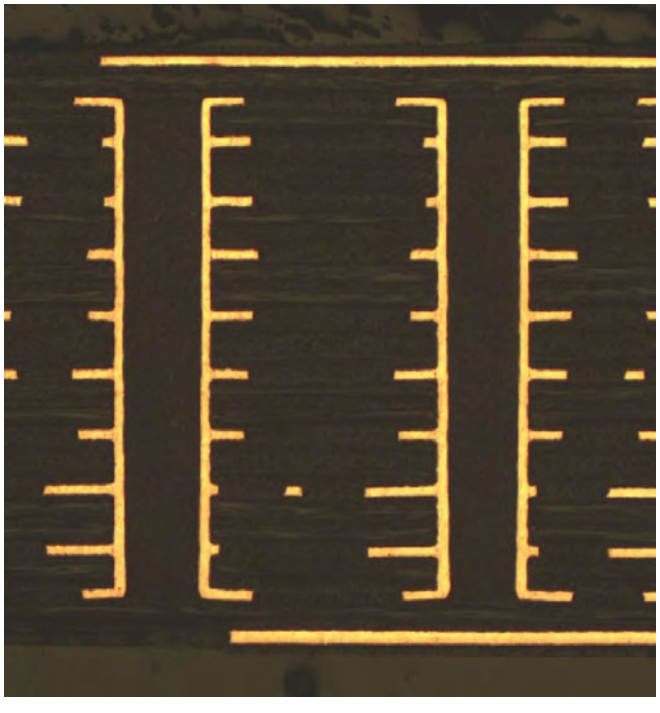

Figure 1: Buried via.

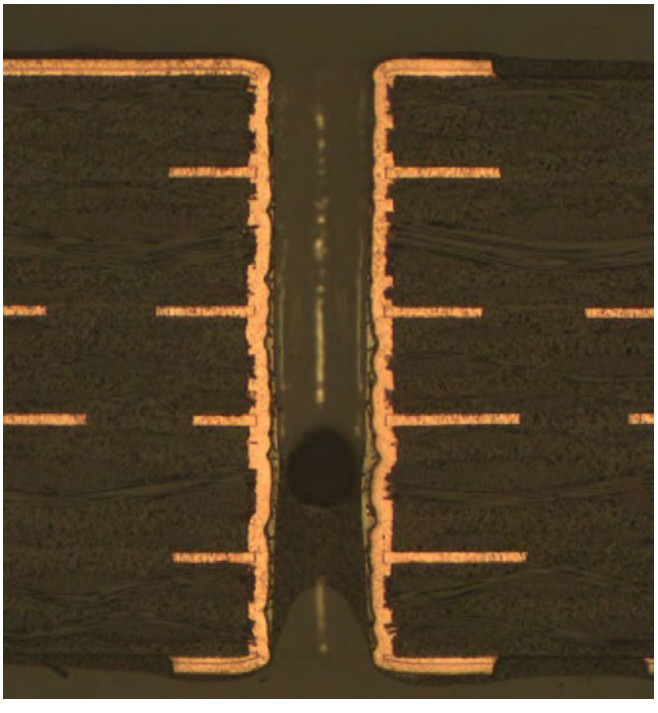

Figure 2: Type III via, plugged.

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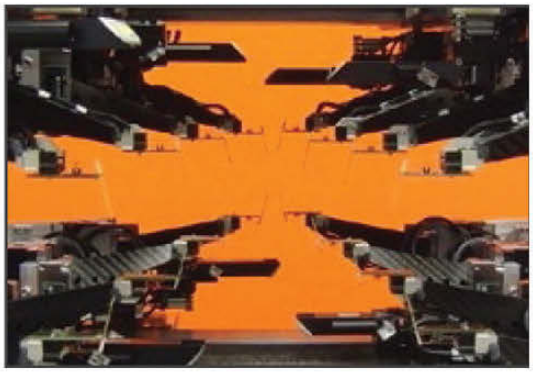

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• **Type IV**—Plugged and Covered: A Type III via with a secondary covering of material applied over the via
• **Type V**—Filled: A via with material applied into the via targeting a full penetration and encapsulation of the hole (Figure 3)
• **Type VI**—Filled and Covered: A Type V via with a secondary covering of material applied over the via
• **Type VII**—Filled and Capped: A Type V via with a secondary metallized coating covering the via (Figure 4)

These type identifications simply specify how the different via structures are categorized, even though the term 'via' is commonly used generically or in combination with the 'through,' 'blind,' or 'buried' adjectives mentioned above.

Additionally, the microvia is another via structure that is commonly used for board interconnections and it is, in essence, just a blind via with dimensional requirements. More specifically, a microvia cannot have an aspect ratio greater than 1:1 and cannot have a total depth into the board greater than 0.25 mm. Figures 5 and 6 show examples of microvias.

Switching gears, qualifying one's ability to manufacture reliable via structures is, obviously, accomplished through testing. These tests generally focus on thermally stressing a specially designed coupon in an attempt to 'open' a connection. After all, the main failure mode associated with vias is that of discontinuity…an interruption in the electrical signal that the via has been constructed to transfer.

For reference, two common IPC test methods for this type of investigation are:

• IPC-TM-650, method 2.6.26A[2]—DC Current Induced Thermal Stress
• IPC-TM-650, method 2.6.27[3]—Thermal Stress, Convection Reflow Assembly Simulation

The reasoning for these stress tests, as well as others that can be used, is to evaluate the ability of the via structure's connections to withstand expansion and contraction within and around the structure itself. The thermal cycling nature of the test/exposure could result in an open circuit that can be diagnosed electrically and/or a mechanical separation that can be observed visually (Figure 7). This visual

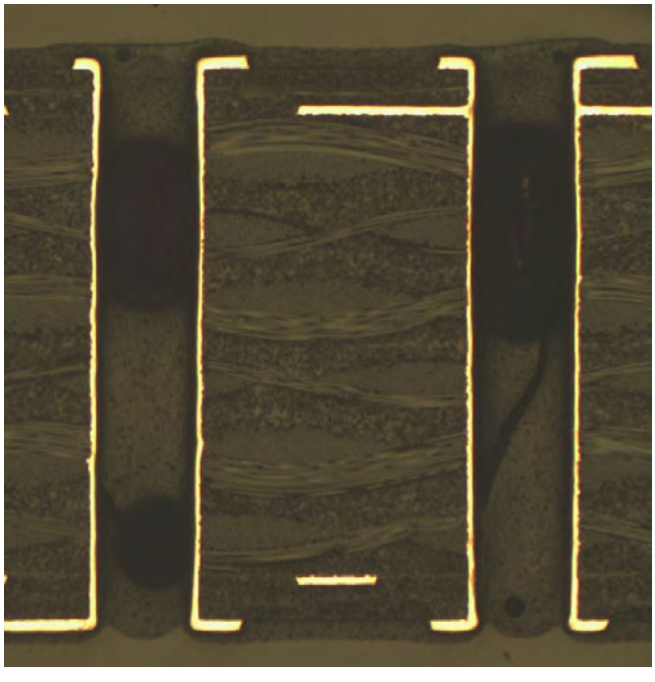

Figure 3: Type V via, filled.

Figure 4: Type VII buried via, filled and capped.

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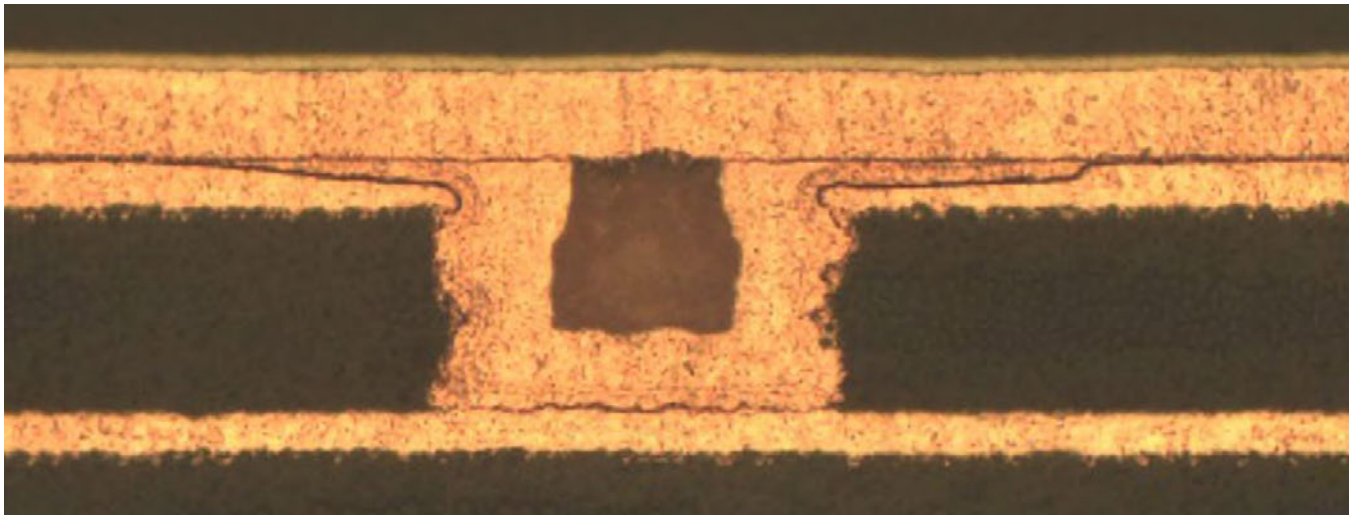

Figure 5: Filled microvia.

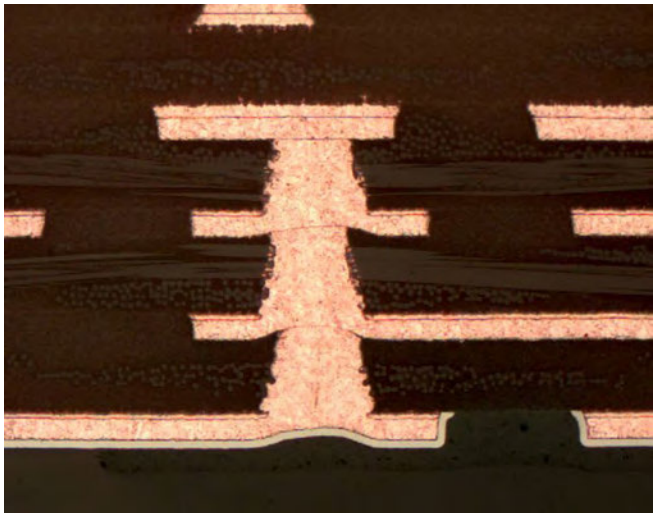

Figure 6: Stacked microvias.

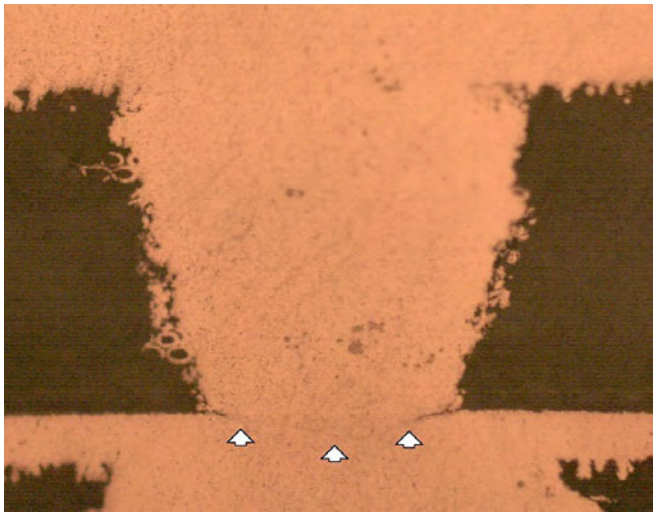

Figure 7: Separation in a microvia.

examination would be completed in cross-section using microsection analysis techniques—as shown in many of the via structure images within this article as well as, likely, in your past experiences.

Ultimately, the via is a simple but critical structure used in the construction of printed circuit boards and understanding the options available can be especially helpful when designing a product. This column is a very brief introduction into the world of vias. As with most things, a little due diligence can result in a plethora of information (as you can read in my October column!). **PCB**

References

1. IPC T-50-Revision M Terms and Definitions for-Interconnecting and Packaging Electronic Circuits
2. IPC-TM-650, method 2.6. 26A
3. IPC-TM-650, method 2.6.27

Keith M. Sellers is operations manager with NTS in Baltimore, Maryland.

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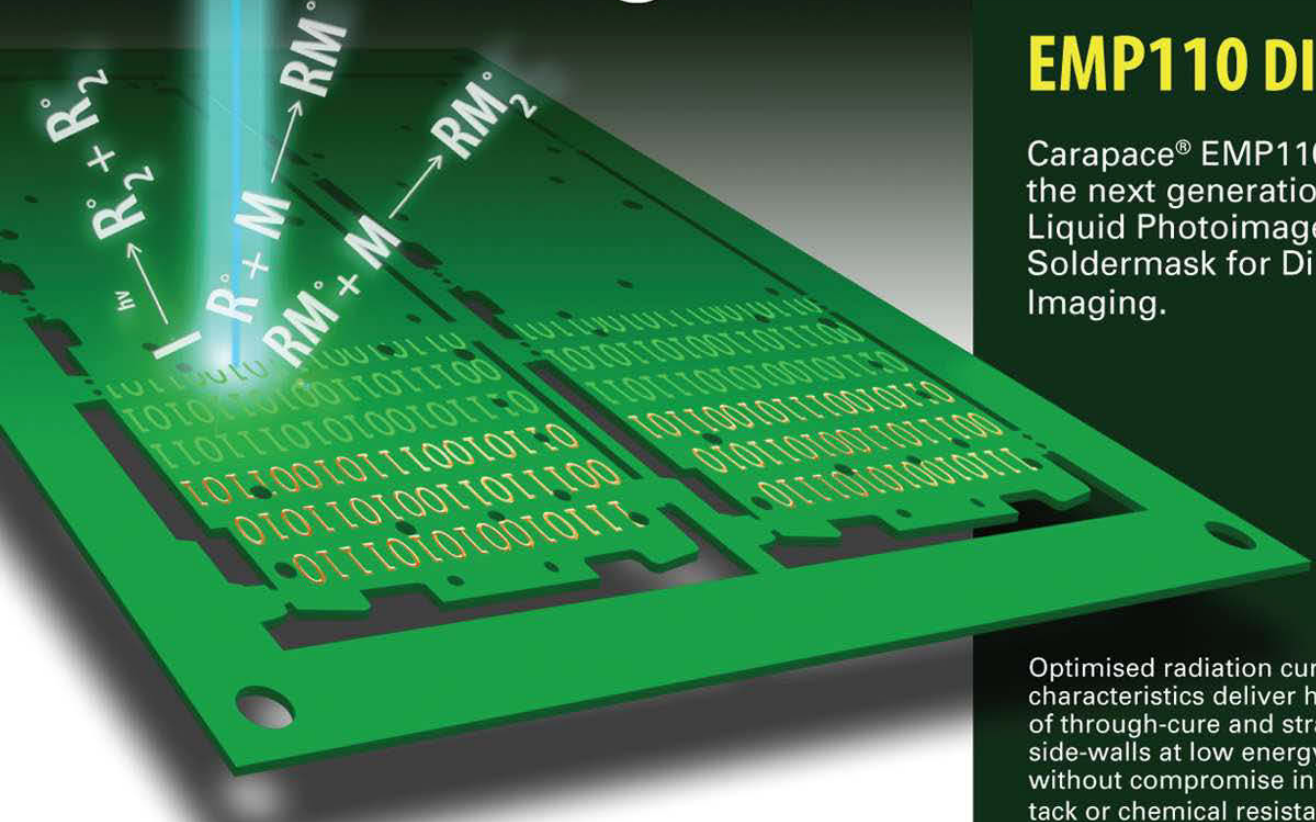

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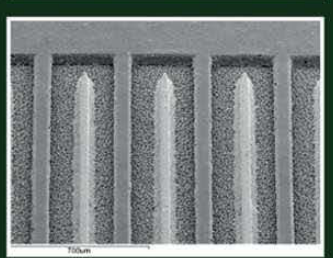

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Innovative Use of Vias for Density Improvements

by Happy Holden

Introduction

In today's fast-paced global, economic environment—which requires constant innovation, upskilling, and performance improvements—there is a need for increasing density. The classic way to increase density is to reduce the trace and spacing. But in many high-speed board applications, the copper and dielectric losses from smaller traces, or the increased crosstalk from reduced spacings, does not permit this.

Four old ideas used in board design and fabrication can offer some insight into how routing density can be increased. These four ideas are:

- Landless vias
- Swing vias for BGA breakout
- Solid paste vias for via-under-pads
- Power mesh for increased layer density

Getting Over the Density Wall

When it comes to getting higher routing density, you only have five degrees of freedom:

- Smaller traces
- Traces closer together (spaces)
- Smaller vias (down to microvias)
- Smaller annular ring for the vias
- Higher layout efficiency when routing (definition in column #10-DFM/A, June 29-2016 Newsletter)

I'm talking about routing density on a single layer; more signal layers will result in more total routing distance on a board.

The equation for routing density is:

$$N = \left[\frac{G-(D_v+2D_a)-C_s}{2C_w}\right]_{INT}$$ Equation 1

Where:
N = number of traces in the channel
G = routing channel dimension
Dv = via diameter (FHS)
Da = via's annular ring
Cs = conductor spacing
Cw = conductor width

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Trace width (in.)	Trace spacing (in.)	Finished hole size (in.)	Finished hole land (in.)	Routing density (traces/inch)	Increase in Density (%)
0.003	0.004	0.010	0.018	80 traces per inch	25%
0.004	0.003	0.010	0.018	60 traces per inch	0 %
0.004	0.004	0.008	0.016	80 traces per inch	25 %
0.004	0.004	0.010	0.016	60 traces per inch	0 %
0.004	0.004	0.010	0.010 (ldls)	80 traces per inch	25 %
BASIS: channel = 0.05"; trace = 0.004"; spacing = 0.004"; FHS = 0.010"; Annular ring = 0.004"					

Table 1: Effect of PCB design rules on routing density on one layer.

If you reduce some of the variables in this equation (Equation 1), then the resulting routing density will go up by the percent indicated in Table 1. The largest effect on density is reducing the trace width, but this can come with electrical issues, the second-best way to increase density is the reduce the vias annular ring, but very small AR will significantly reduce the vias reliability. Therefore, landless is an excellent way to achieve higher density with reducing trace widths or spacings.

Because the number of through-holes on a multilayer block numerous routing channels all through the board, the use of blind and buried vias can significantly increase a layers routing density, on the order of 2x to 4x without their use. This is also measured by layout efficiency (L.E.), the amount of space used for routing as compared to the entire area on the signal layer. L.E. is also enhanced by blind and buried vias, to the order of 2x to 4x. The L.E. for a TH multilayer is 8% to 10%; 16% with TH and blind vias; to 24% for TH/with 2-sided blind-vias and multiple build-up layers. Some of the contributions to increased density, including the maximum number of traces available for various routing channel widths as a function of via diameters, annular rings (including landless) are seen in Table 1.

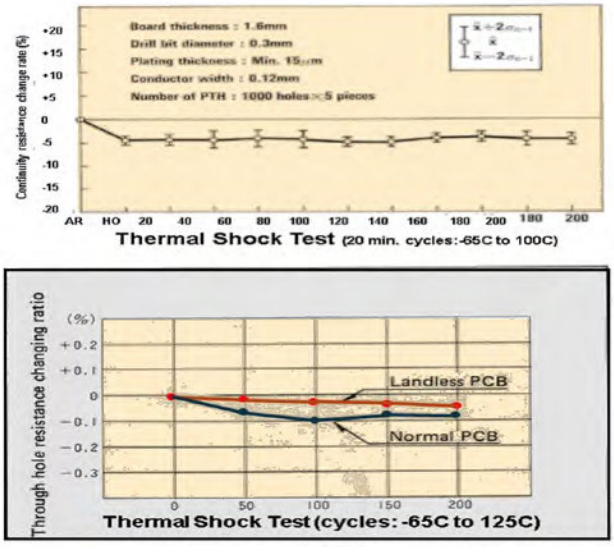

Figure 1: Reliability data from NEC on their landless via fabrication process[1].

Landless Vias

I saw my first landless via multilayer while visiting NEC at Toyama, Japan back in 1985[1]. They were an enormous automated facility making Japanese telecom and mainframe computer boards, kind of like IBM and Western Electric rolled into one. NEC was using the liquid electrophoretic, positive-acting photoresist process with panel-plating. I wouldn't see another landless via multilayer until our Japanese partner (OKI) introduced it to us in 1988. OKI was using landless vias to achieve higher density without having to pay the extra costs of finer lines. They knew about the higher reliability that resulted; they had done their own testing (Figure 1) but were after the higher routing density. These vias are seen in Figure 2 and it allowed them to route five traces between 0.100 inch PTH centers.

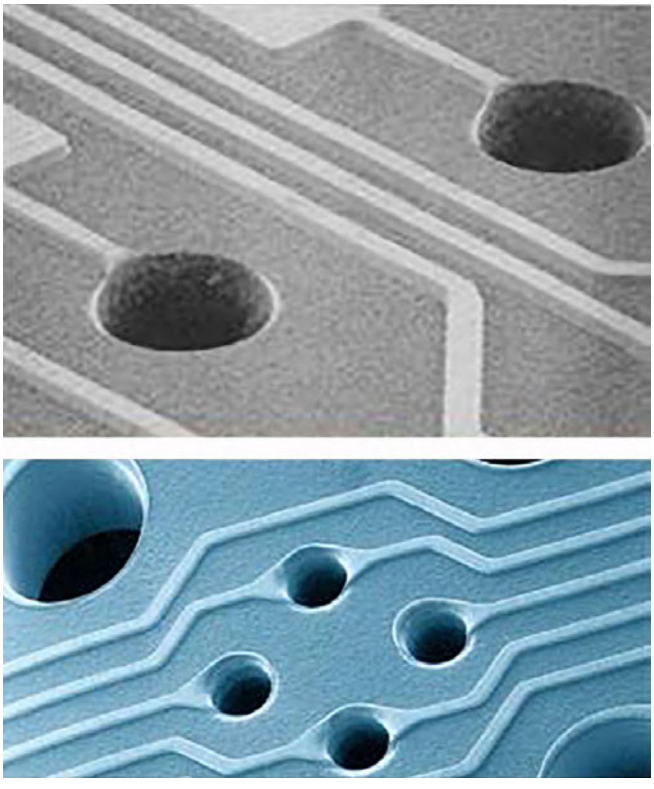

Figure 2: Typical landless vias on a Japanese multilayer from around 1985[1].

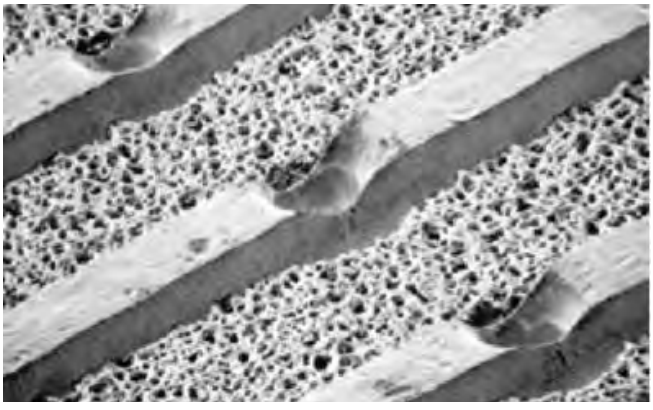

Figure 3: Landless via supplemented with the same diameter as the trace width, in this case, 0.004" (0.1 mm). These are referred to as 'invisible vias.' (Source: HP Sunnyvale PC)

Landless Via Processes

There are numerous patent applications about landless vias. All require laser sculpting of the via or pinpoint laser exposure for the imaging. None of these have ever entered production. The two that have been used in high-volume production are listed here, with two additional techniques that appear to be very practical.

HP Process Learned from the Japanese

The Japanese process for making landless vias is very simple, but anyone I talked to never figured it out until I explained the process. It is a true example of thinking outside the box:

1. Whatever your registration tolerances are, then reduce the artwork land opening size by that amount when using dry film photoresist. The dry film will now extend beyond the wall of the drilled hole.

2. Two things will happen with this arrangement: 1) the plating bath will be forced to throw into the hole thus improving the distribution; 2) There will be no land except where the trace enters the hole.

3. After stripping and etching, there will be landless vias with the trace dropping into the barrel of the PTH or blind via.

4. This process does not work for panel plating; that requires theuse of the next process like NEC.

Positive Liquid Electrophoretic Photoresist

As I reported, I first saw this process in Japan in 1985 at NEC. They were using a positive electrophoretic photoresist from Nippon Paint, evolved from the electrophoretic paints used on automobiles. A similar photoresist was available in the USA and Europe by Shipley[2,3]. A more recent photoresist and process came from PPG Industries and is documented in a paper by Patricia Goldman (at that time with PPG) and Tim Schmidt of Compunetics[4]. The positive-acting photoresists have many properties that can be very useful. The most useful is multiple exposure and developing, its resistance to plating especially Ni-Au and etching, its fine-line resolution [down to 10 micron (0.4 mil)] and its insensitivity to dust and clean-room debris. The coating process is relative simple:

- Clean panel
- Coat for 60 to 90 sec at 60V~100V (voltage will determine finished thickness)
- Rinse
- Bake dry

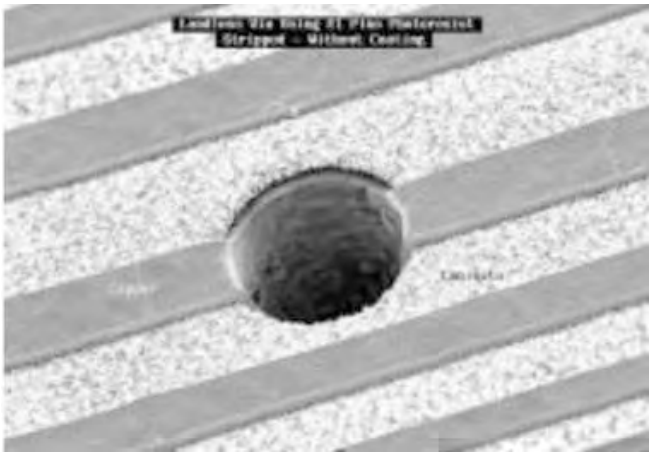

Figure 4: Landless via [0.010 in (0.25 mm) and .004 in (0.1 mm) traces] created with the liquid, electrophoretic, positive photoresist from PPG. (Source: Compunetics Inc.)

The panels are now ready for exposure or transportation. A finished panel after plate/coat/expose/develop/etch is shown in Figure 4.

Perfect Registration

Now with the advent of direct digital imaging (DDI) and board scanning, it is possible to have perfect registration on both sides of a board. There are DDI units that have nine cameras that scan a panel as it enters the machine from both sides. Then, as it starts to expose each side, the artwork is modified on-the-fly so that each land is perfectly registered to its hole. Without high-speed computers, scanners and the new software, this was impossible before.

Novel Russian Technique

At a recent PCB West conference, I had a conversation with a Russian PCB fabricator. It seems the Russians also used landless vias after they saw them in Japanese computers. The Russian process was novel and I wish I had thought it up! They used the property of dry film photoresist's sensitivity to oxygen. When they laminate the dry film to the panel, they have a shroud around the unit filled with oxygen. Thus oxygen is trapped in the holes by the dry film. They expose the panel with their normal artwork (but there are no lands for traces that will interconnect to the landless vias). They then do a short 100°C bake of the panels, remove the cover sheet on the dry film, and develop normally. The oxygen and heat has polymerized the dry film from the inside at exactly the same diameter as the hole. Thus when developed, the via has perfect dry film registration and is landless.

More details, including figures that show how landless vias are more reliable than vias with small annular rings, can be found in the recently published article, "Against the Density Wall: Landless Vias Might be the Answer."[5]

Swing Vias for BGA Breakout

A new concept resulting from HDI is to arrange the blind via rotation not in the normal north-east-west-south rotation but to move them into the same channel and stagger them. This arrangement forms a broad boulevard between the buried vias 4x larger than the device pitch. This boulevard is 4X and can permit a vast freeway for global routing. The "swing"concept is explained further in an article I wrote with Charles Pfeil in 2011:

> *"The principle is to 'swing' the vias away from the ball pads forming wide boulevards on the innerlayers for routing. Depending on the size of the micro-via, the pin-pitch and size of the ball pads, you may be able to align the micro-vias into straight columns and rows. This will maximize the available space for routing."*[6]

Boulevards Enhanced by Via Structures

Boulevards can be enhanced by the 3D via structure. The various depths of blind vias help to create larger boulevards. These structures can be created by skip vias, multiple build-up or sequentially laminated drilled and laminated vias. This is also a via structure you will want to have because it provides routing of high-speed critical nets using only the cross-over from horizontal to vertical of small low-inductance blind vias. These are the lowest inductance vias in the board and ideal for the highest-speed nets. These will also have a very high density because the crossover will be small blind vias, not the larger buried or through-hole vias.

Boulevards Created by Via Placement

A new concept in applying different types of fanout patterns for BGAs has been developed

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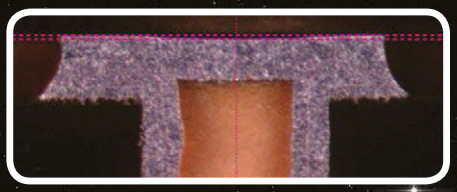

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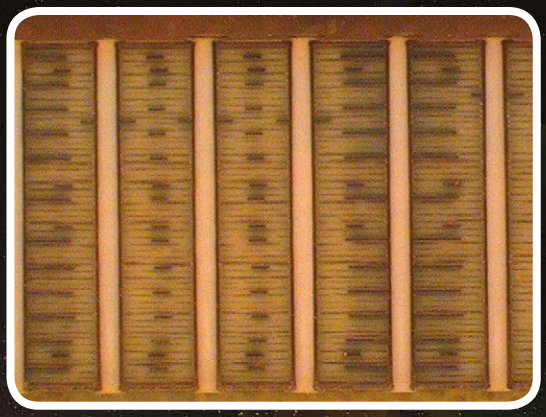

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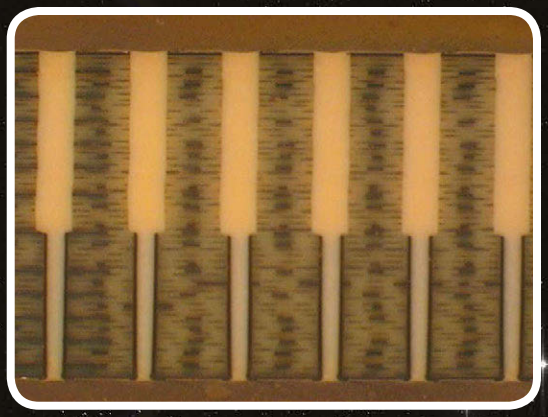

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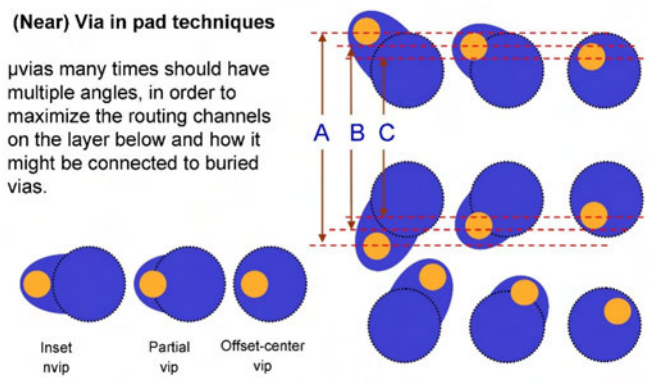

Figure 5: By 'swinging' the vias, depending on where the via is placed in respect to the SMT land, channels are created, A, B or C. These channels are the boulevards for 2X to 3X greater routing density[7].

by Mentor Graphics[7]. Instead of the standard four-quadrant dog-bone (N-S-E-W), the BGA is segmented into four regions from the outside-in. The smaller blind vias, with their improved registration and smaller annular-rings are now "swung around" to form routing channels. Figure 5 shows a sample BGA blind via placement.

The description of this concept is provided by Charles Pfeil, the developer:

> *"Region 1 comprises the outer rows. The number of rows will vary from 4 to 6, depending on the design rules. This region uses a 1:2 microvia with the intent of routing the traces on Layer 2 at maximum route density. This pattern can be varied by moving the via closer to the ball pad and changing the angle, so that the via spacing exceeds the minimum. If you do this, the route density will decrease; however, you may increase room for plane fill and reduce potential crosstalk between the vias."*

> *"Region 2 includes all the inside rows. Once the outer rows of BGA pins are routed using the 1:2 micro-vias, the next 4 to 6 rows should use the 1:3 skip vias, with the intent of routing the traces on Layer 3 at maximum route density. Using the skip-via allows a connection from Layer 1 to Layer 3 without a pad on Layer 2. This pattern can also be varied by moving the via closer to the ball pad and changing the angle so that via spacing exceeds the minimum.*

> *"Region 3 is the transition between the inside rows (Region 2) and the center rows (Region 4). Since the patterns between Regions 2 and 4 will usually conflict and cause DRC violations, a transition area is appropriate. A 1:2 or 1:3 via can be used in the transition area depending on your routing strategy. In this example, the pattern is a simple orthogonal short dog-bone. Other angles may be used depending on the via size used.*

> *"Region 4 is the center. The center rows are those left over after other regions have been defined. Usually, the center of the BGA has power and ground pins, and thus putting the through vias in a standard dog-bone pattern. Note that the vias are not located in the exact center of the ball pad matrix – this allows for a greater ground plane fill on Layer 1.*

> *"The Diagonal Region(1). The pins along the diagonals could have conflicting patterns when the Region 1 and Region 2 fanouts merge. The example in Figure 5 shows a method that not only merges the patterns, but also spreads the vias away from the centerline, providing greater route density along the diagonal. Dividing up the BGA into regions enables maximum route density, and can thereby reduce the number of layers needed. When the BGA has over 1500 pins, simply routing out of the BGA tends to be the primary contributor to increased layer count. By varying the number of rows used in each region, based on the stackup and via spans available, you can obtain the most optimal fanouts and routing in the context of your own specific design."*[7]

This aligned-via pattern of shifted blind vias increases breakout from big BGAs significantly. However, it also has other advantages:

- 24% increased route density per layer over through-vias and unshifted blind vias
- More room for a ground plane on the mount layer (but not as much room as with via-in-pad)
- If you route the high-speed single-ended nets on the layers using blind vias, via stubs are eliminated and via-to-via crosstalk is minimized

• Any signal routed on the blind via layers will not need to have a buried via, thus opening up route space on the buried via layers as well

• The disadvantage is that blind and buried via stackup is slightly more expensive than a through-via stackup

Example of Shifted Blind Vias

An excellent example of shifted-aligned-via pattern is the Xilinx Virtex-4 and Virtex-5 FF1760 series FPGA with 1760 pins and a 1 mm pin-pitch from an article by Pfeil[5]. Xilinx Application Data sheets show the use of six-signal layer to breakout their device. In Pfeil's article, using the shifted-aligned-via pattern to form boulevards, he completed the breakout is only two signal layers. The stackup is also seen in Figure 6 and is a common and cost effective IPC-Type II 12-layer HDI.

To understand how this was accomplished requires you look closely at both the HDI stackup and the aligned-shifted blind vias. This close-up can be seen in in Figure 7. Two rows of the FPGA pins fanout to layer 3 (with a skip via-for the 50 ohms single-ended Rocket I/O) and the next two rows fanout to layer 2 then drop to the

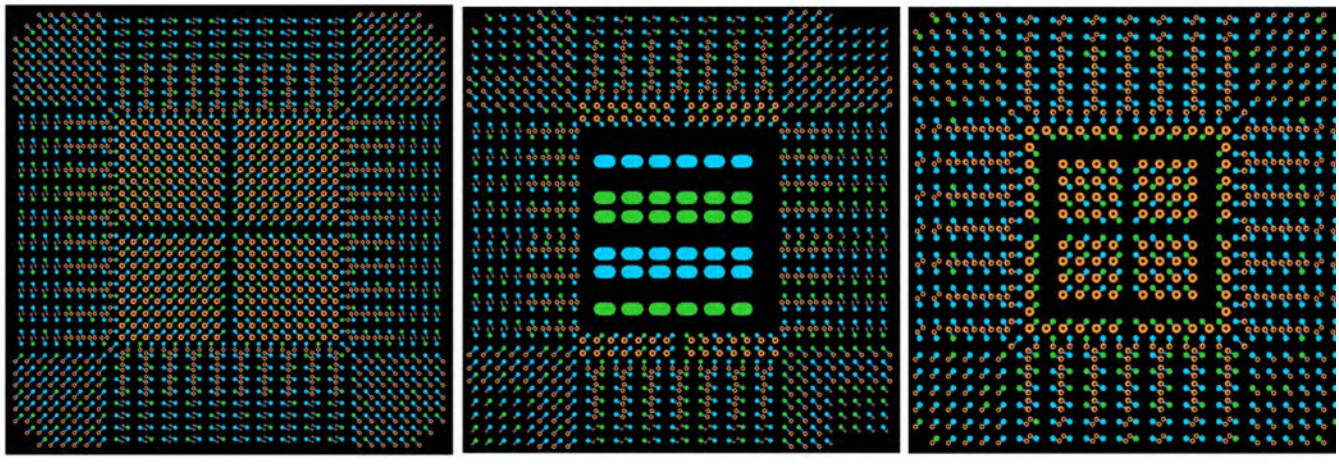

Figure 6: Example for a Virtex 5, 1760 pin FPGA. Three alternative surface breakout using 'swing vias'[7].

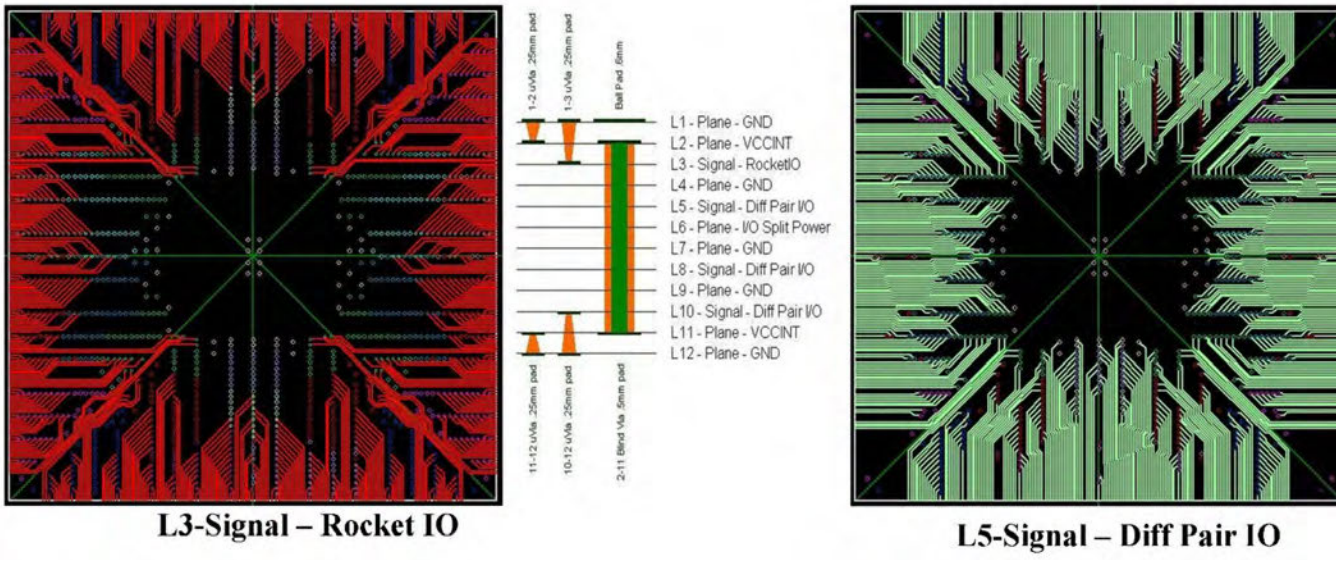

Figure 7: Example for Virtex 5, 1760 pin FPGA, Layer 3 and Layer 5 breakout boulevard routing with stackup view[7].

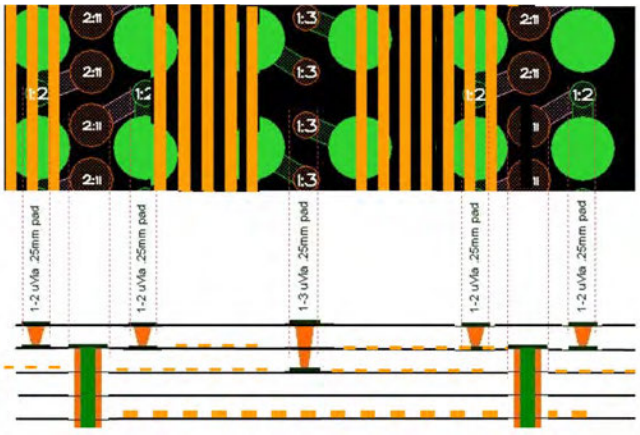

Figure 8: Close-up of Virtex 5 breakout of Figure 7[7].

buried via to layer 5 (the 100 ohm differential-pair I/O). This arrangement forms a broad boulevard between the buried vias four times larger than the device pitch. This boulevard is 4.0 mm and can permit the routing of up to 13 traces—a vast freeway for global routing. Under layer 5, the BGA disappears as there are only the buried vias creating this via-lined-boulevard for mass routing.

Solid Paste Vias

The purpose of this section is to examine a variety of advanced HDI fabrication processes that have evolved over time. It must be understood that interconnect via hole (IVH) formation is just one element of fabricating HDI wiring boards and, although the laser drilling method is the most popular, a number of other methods for defining the IVH have taken root. The other two important factors are the various dielectric materials and the methods of metallization. Fabrication of HDI wiring boards with microvia holes involves many new processes not common to conventional board fabrication. Therefore, additional emphasis will be placed

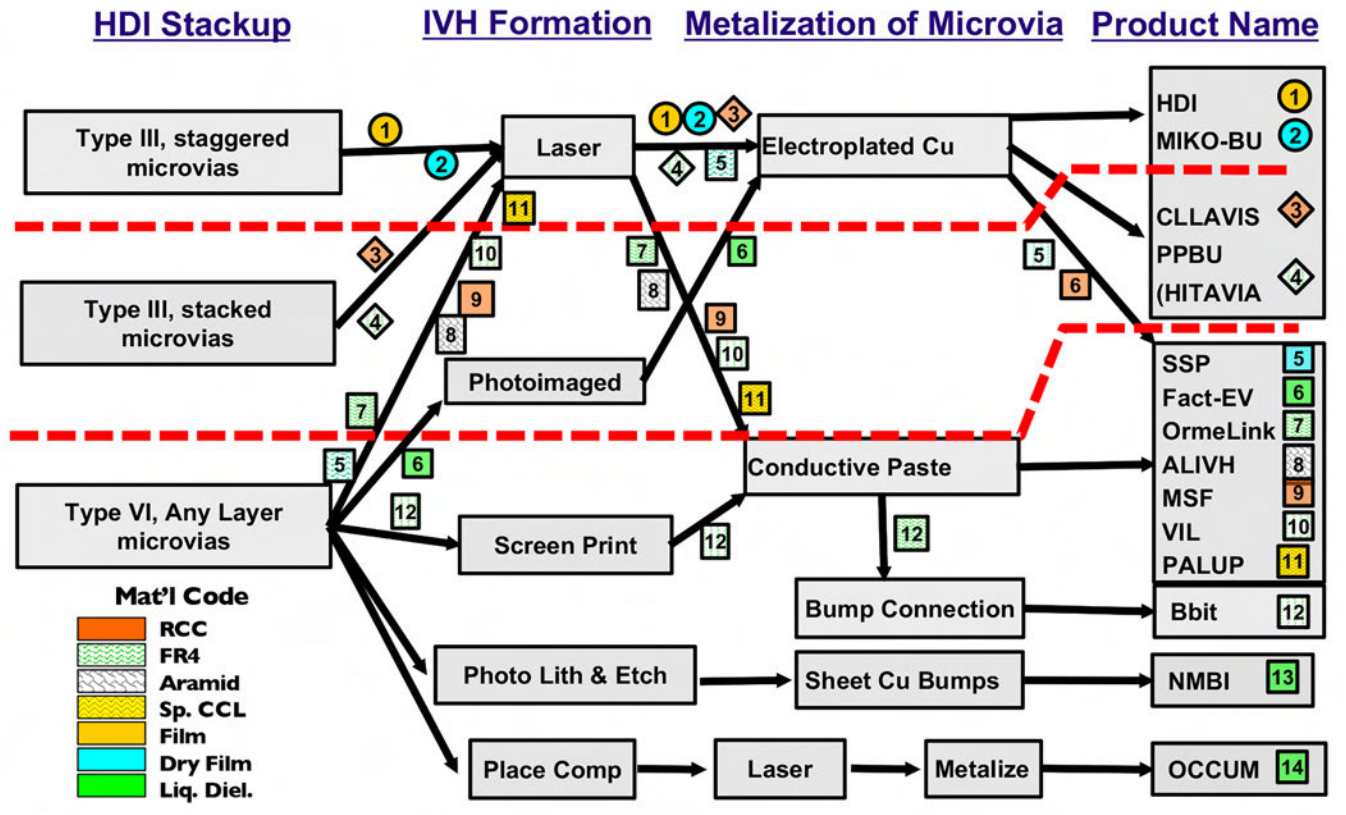

Figure 9: The HDI technologies in use today are made up of four important factors: The microvia stack-up architecture, the dielectric materials, the methods of IVH formation, and the method of metallization of those z-axis via connections. In recent years, 14 different HDI processes have been developed[8].

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upon these new fabrication processes that are common too other microvia technologies.

Definitions of HDI Process Factors

In Figure 9, the HDI technologies in use today are made up of four factors: The via stackup, the dielectric materials, the methods of IVH formation, and the method of metallization of those z-axis via connections. In recent years, 14 different advanced HDI processes have been used.

Solid Conductive Via Fill

The IPC Type VI group of HDI technologies all utilize metallic pastes or a solid sheet of metal to form the via connections. Table 2 presents these alternatives to copper plating for forming IVH connections.

OrmeLink

Ormet's innovative metallic paste allowed CTS's co-lamination process with their (Ormet's) transient liquid phase sintering (TLPS) process (OrmeLink) to be similar to the ALIVH process conductive paste. It is a via paste of copper-tin organometallic matrix that sinters into a solid metallurgical via. CTS's process is called ViaPly. Past users, in addition to Sheldahl, included Litronics, acquired by Allied Signal/Honeywell in 1997. Up to four layer pairs have been connected (eight metal layers) using OrmeLink. Other uses of the Ormet paste have constructed multilayers of up to 60 layers.

Structure

The Ormet structure is made up of polyimide or FR-4 layer pairs. Different materials can be mixed if a rigid core or heat spreader is required. The conductive paste is a TLPS ink of copper-tin. The structure is shown in Figure 10. Figure 11 shows the cross-sections of two finished circuits with lasered-via polyimide layer pairs, with TLPS solid metallurgical vias connecting the layer pairs and FR-4 innerlayer cores with buried TLPS vias.

Fabricator	Trade Name	IVH Process	Metallization
Dyconex	DYCOre	Copper etching	Etched copper bumps
Ormet, San Diego, CA	OrmeLink	Laser, plasma, or photodielectric	Cu/Sn organo-metallic
Matsushita Comp.	ALIVH	Laser	Copper particles in epoxy
Toshiba	Bbit	Insulation displacement	Silver/epoxy paste
Parelec	PARMOD	Drill, laser, or photodielectric	Metallo-organic decomposition, Cu or Ag
Namics	Unimec	Punch, drill	Silver, palladium, and copper particle pastes
North Corp.	NMBI NMTI (Neo-Manhattan)	Image and etch	Etched copper bump
Denso	PALUP	Laser	Cu organo-metallic
Shinko	MSF	Laser	Conductive paste
Victor	VIL	Laser	Silver/epoxy paste

Table 2: Alternative HDI technologies utilizing filled, solid IVH[8].

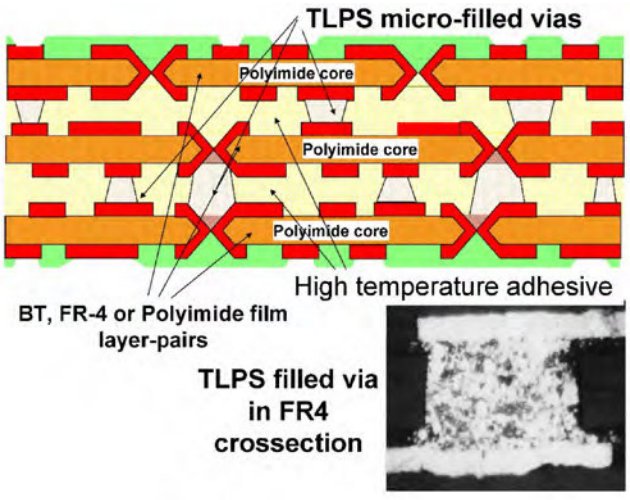

Figure 10: The co-lamination (OrmeLink) multilayer structure[8].

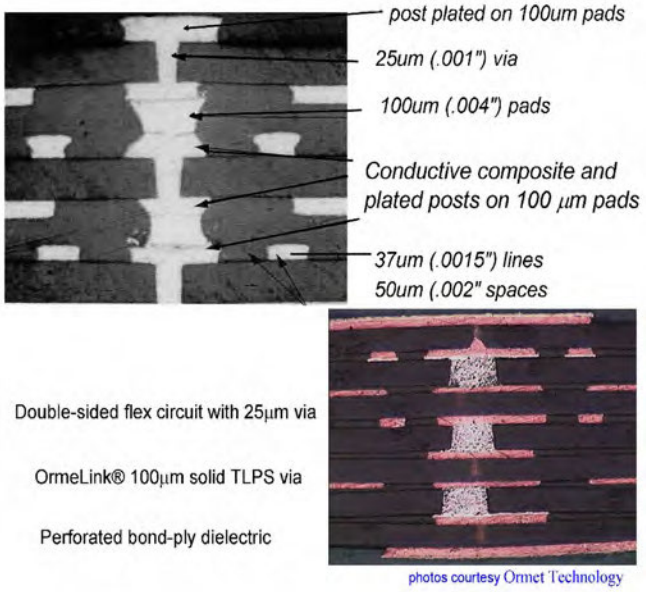

Figure 11: Examples of TLPS cross-sections of three layer pairs with lasered-vias filled with TLPS paste vias and buried vias for FR-4 innerlayers[8].

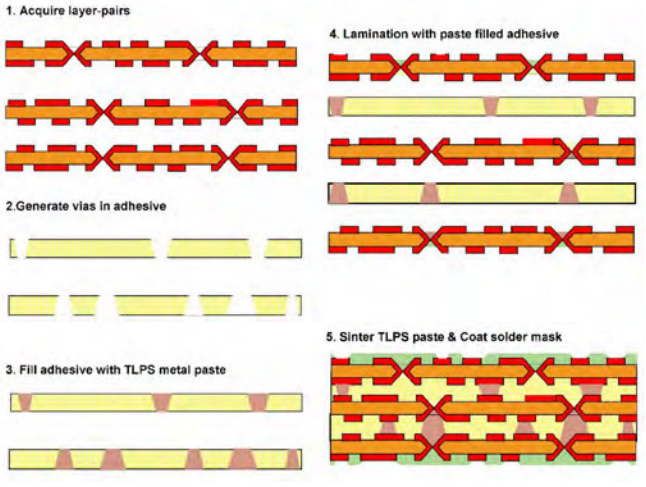

Figure 12: The OrmeLink multilayer substrate fabrication process[8].

Manufacturing Process

The manufacturing process is shown in Figure 12. The microvias are lasered or punched in the polymide adhesive and then filled with the TLPS paste. The structure can now take layer pairs from any other HDIS process (such as Sheldahl's) and turn them into a multilayer structure through sintering. The conductive pastes have to be sintered in a condensing vapor of fluorocarbon at 215°C for 2 min. The structure is then postcured by baking for 40 min. at 175°C. Table 3 details the process.

Power Mesh for Increased Layer Density

Power mesh is a layer topology architecture that merges power supply routing with signal routings. The techniques use the old RF techniques of co-planar power. Conventional design utilizes dedicated power planes as seen in Figure 13a. Increasing density and the number of voltage rails has required that split planes be introduced, shown in Figure 13b. But higher pin-count BGAs like FPGAs can have numerous voltages, and this is where utilizing blind vias minimizes both the plane perforations and insures coupling and a return path for the signals. A further experimental HDI technology, can increase the split planes to as many as eight different voltage rails.

That is to use two, orthogonal layers to distribute POWER as a 'mesh structure' and to place signals between the different voltages. This can be seen in Figure 13c and the structure is called a 'Dual Offset Coplanar Stripline w/Separate GND Reference' (Figure 13d). Line widths and dielectric distances are given for the various impedances that are commonly used. This structure has the advantage of lower crosstalk but more importantly, it provides voltage to all the components from 'LAYER_2' and

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Property	Curing Process
Ormet 2005 Series Ink	Specification and processing parameter
Electrical Conductivity	Bulk 4.0×10^{-3} Ohms-cm. Sheet resistance 10.0×10^{-3} Ohms/sq. in.
Adhesion (Tensile Pull) on Various Materials FR-4 (T_g = 125°C)	1,300 psi (minimum)
Copper	2,921 psi (average)
Printability	With 230 stainless steel wire mesh and emulsion thickness of 7.5 µm Sintered thickness 28–38 µm 200 µm traces on 400 µm pitch
Cure Cycle	30 min. drying at 85°C 2 min. vapor cure at 215°C 40 min. postcure at 175°C

Table 3: Properties and curing processes for the Ormet type of TLPS conductive pastes.

LAYER_N-1' using only a blind-via to keep the 'loop area' small.

The power mesh architecture was derived from the Interconnected Mesh Power System (IMPS) developed and patented in the 1990s by the High Density Electronics Center (HiDEC) of the University of Arkansas, Fayetteville, AR[9].

Power mesh architecture is the result of applying IMPS lessons to the common microvia multilayer. A four-layer structure is used for the printed circuit. Only power is meshed on the innerlayers because ground is on the outerlayers along with via-in-pad technology as shown in Figure 13c and 13d. This reduced layer count microvia multilayer is so efficient in layout, it can replace three times (3x) the number of normal signal innerlayers on a conventional through-hole multilayer and the power and ground planes they require.

The table in Figure 13e shows the values for 50 ohm single-ended and 100 ohm differential impedances for different trace widths, spacings, core thicknesses and overall thicknesses.

The crosstalk model indicates that the power mesh architecture creates a naturally low crosstalk condition. Each signal trace of 5 mils is approximately 3x or 4x distance from the next signal, depending on the power trace width. This creates horizontal crosstalk of less than 2%.

The wiring models used to predict actual wiring density are presented in the Power Mesh article[8] and has 17 to 40 signal inches per square inch per layer while the conventional through-hole multilayer will have 5 to 12 signal inches per square inch or is 3x to 4x more dense.

Conclusion

These four techniques can all increase density and have been proven in volume production. They are relatively old (>20 years) techniques, but can still be used today. Looking for ways to increase multilayer density and reduce layer count, but not reduce the trace width or trace spacings, leave all of these techniques open for new innovations. **PCB**

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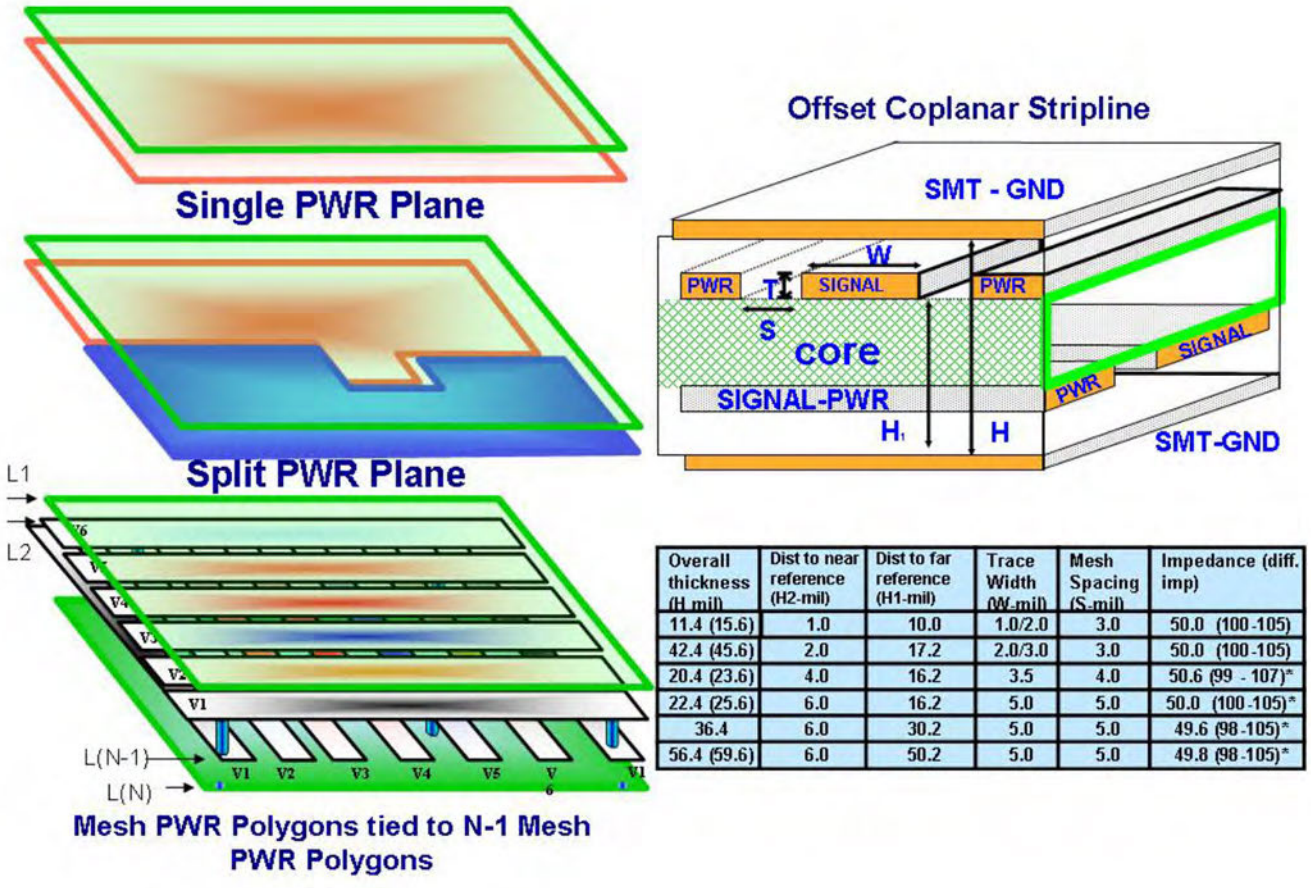

Overall thickness (H mil)	Dist to near reference (H2-mil)	Dist to far reference (H1-mil)	Trace Width (W-mil)	Mesh Spacing (S-mil)	Impedance (diff. imp)
11.4 (15.6)	1.0	10.0	1.0/2.0	3.0	50.0 (100-105)
42.4 (45.6)	2.0	17.2	2.0/3.0	3.0	50.0 (100-105)
20.4 (23.6)	4.0	16.2	3.5	4.0	50.6 (99 - 107)*
22.4 (25.6)	6.0	16.2	5.0	5.0	50.0 (100-105)*
36.4	6.0	30.2	5.0	5.0	49.6 (98-105)*
56.4 (59.6)	6.0	50.2	5.0	5.0	49.8 (98-105)*

Figure 13: Single (a) and split plane (b) PDN for multilayers with (c) the power mesh architecture modeled as (d) offset coplanar stripline and (d) impedances of this structure[9].

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Happy Holden has worked in printed circuit technology since 1970 with Hewlett-Packard, NanYa/Westwood, Merix, Foxconn and Gentex. Currently, he is the co-editor, with Clyde Coombs, of the Printed Circuit Handbook, 7th Ed. To view past columns or to contact Holden, click here.

Supply Lines
Highlights

Isola CEO Jeff Waters Shares Insights and Reflections
It's been eight months since Isola's Jeff Waters was appointed CEO, marking his transition from the semiconductor space to the PCB industry. At PCB West, Jeff reflected on his first impressions of the PCB industry and how Isola continues to adopt changes in its manufacturing strategy and product development with a plan to become the industry leader with a global, competitive presence.

Ventec International Appoints Denis McCarthy Jr. as Technical Sales Account Manager
Ventec International is delighted to announce the appointment of Denis McCarthy Jr. as technical sales account manager based at the company's Chicago facility.

Taiyo America Adds Customer Service Rep After Linda Merrell Retires
Taiyo has added a new customer service representative, Alyssa Orellana. The recent change was due to the retirement of Linda Merrell, a 22-year veteran of the customer service department.

Karl's Tech Talk: EPOXY—Supply Chain and Use in Electronics
From a PCB fabricator's perspective, epoxy resin supply chain issues are of indirect concern as they become a subset of laminate quality, supply, and cost considerations.

Insulectro Hires Industry Sales Veteran Bill Linse as Technical Account Manager
Insulectro has hired industry sales veteran Bill Linse as Technical Account Manager.

Shengyi Launches High-Performance, Low-Loss RF/Microwave Material
Shengyi Technology has announced the availability of AeroWave, a high reliability, cost-effective material system targeted towards auto radar (24GHz.), base station transceivers, power amplifiers, telemetry devices and antenna systems.

Seacole Hires Account Manager Dedicated to PCB Market
Seacole Specialty Chemical is excited to announce the hiring of Walt Forgacs as a printed circuit board account manager. Forgacs' mission will be to strengthen and grow Seacole's printed circuit board segment of the business.

Gardien Names Cheng De Electronics Technology as Agent in Taiwan
The Gardien Group has signed a new agency agreement with Cheng De Electronics Technology Co. to act as its Taiwanese agent in support of the company's equipment product lines.

Nordson MARCH Wins Award for FlexTRAK-CDS High-Volume Plasma System
Nordson MARCH, a Nordson company, won an award for its FlexTRAK-CDS high-volume plasma system at a ceremony held in conjunction with the SMTA International conference in Rosemont, IL on September 27, 2016. The system removes contamination, etches surfaces to improve adhesion, and provides surface activation prior to die attach, wire bond, mold encapsulation, and underfill to lead frame strips, laminated substrates, and other strip-type electronic components.

Ventec Celebrates a Decade of Innovation, Excellence and Business Growth at electronica
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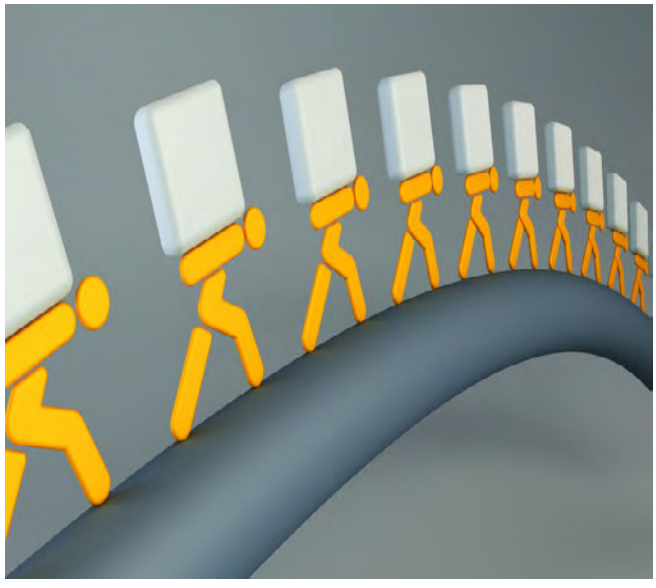

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Advanced UV Lasers for Fast, High-Precision PCB Manufacturing

by Jim Bovatsek
SPECTRA-PHYSICS

Introduction

For more than 30 years, lasers have played a significant role in the manufacturing of PCBs. It is not a coincidence that electronic devices have, at the same time, become increasingly miniaturized. The ability to tightly focus a laser beam much smaller than a mechanical tool has been an enabler of such dense, compact circuitry; and the elimination of consumables such as drilling and routing bits has reduced manufacturing costs.

The workhorse laser technology over the years has been the carbon dioxide (CO2) laser, which has provided manufacturers with reliable, cost-effective power for various applications. The most identifiable laser process in PCB manufacturing is what is referred to as via drilling, which involves laser drilling a hole through an electrically insulating dielectric layer on a copper substrate. Generally, if the substrate is left intact, the hole is a blind via; if it is also drilled through, it is a through via. Very small holes having diameters below about 150 micrometers are commonly referred to as microvias. After a subsequent copper plating step, an electrical interconnection through the dielectric layer is formed. By arranging these vias in various two-dimensional configurations and by implementing additional build-up, drilling, and plating steps to introduce a third dimension, the high-density interconnect (HDI) and packaging needs of today's powerful yet compact electronic devices are satisfied.

Making it Smaller

As always there is a mandate for smaller: smaller mobile devices, smaller microchips, smaller electronics packages, and smaller interconnect vias. Vias drilled with CO2 lasers are generally limited to diameters of 60–80 µm or larger due to the long (~10 µm) wavelength of the light, which has a direct bearing on how small the beam can be focused. While smaller via sizes can technically be achieved, the business case quickly vanishes due to higher overall process complexity (and therefore cost).

Here is where shorter-wavelength pulsed ultraviolet (UV) diode-pumped solid-state (DPSS) laser technology enters the picture. The short UV wavelength—about 30 times shorter compared to CO2 wavelengths—can easily be focused to

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the small sizes necessary for the fabrication of increasingly small microvias. Since the mid-1990s, pulsed UV DPSS lasers with nanosecond (ns) pulse durations have been commercially available for industrial/OEM use. While during the early days of the technology the relatively high cost and troubling reliability issues limited their appeal, today's products are vastly improved in both areas. Indeed, over the past decade, the cost per Watt for such lasers has fallen by an order of magnitude, and product lifetimes have improved dramatically, in some cases surpassing 20,000 operating hours at high power levels.

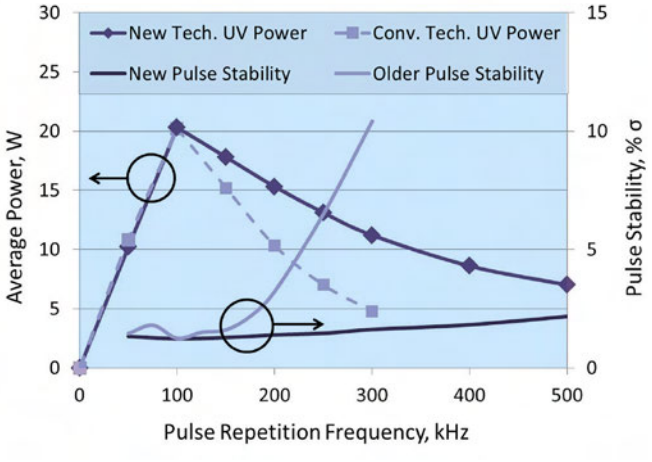


Figure 1: Advanced UV light conversion leads to high power and high-pulse energy stability well beyond the nominal pulse frequency.

Today's UV DPSS Laser Technology

Typically, a UV DPSS laser begins with a high-power laser source at a fundamental infrared (IR) wavelength of ~1 mm which is focused into nonlinear optical crystals to generate the UV output, a phenomenon known as harmonic conversion. The IR to UV conversion efficiency is dependent on the IR pulse energy, among other factors. The pulse energy is equal to the laser's average power divided by the pulsing frequency or pulse repetition frequency (PRF).

For IR wavelengths, the average power is relatively constant above some particular frequency, and therefore higher PRFs result in lower pulse energies, and vice-versa. As for the converted UV light, the maximum average power is achieved at some nominal frequency, PRFnom, the specific value of which is determined by the design of the laser. The average power at the UV wavelength decreases with operation at higher PRFs since the IR pulse energy, and hence the IR to UV conversion efficiency, diminishes.

If elevated UV power levels can be maintained for a wide range of operating PRFs through a careful laser design consideration then this offers a high level of machining flexibility for the end user. Higher energies can be used to machine large features and deep cuts, but if lower energies are required for precision drilling, cutting and micromachining, operation at higher PRF levels can be used to proportionally scale up throughput. In short, the ability to have relatively high power levels for an extended PRF range would make for a highly flexible tool with a large application space. And if one laser can operate across this continuum, then tool builders can reap the cost savings inherent in having both a single equipment interface (mechanical, electrical, optical, communication) and a single equipment supplier (higher volume orders reducing cost per unit).

Increasingly, lasers incorporating such advanced design and UV conversion technology (including Spectra-Physics' latest industrial UV lasers) are becoming available on the marketplace. While the exact techniques for achieving this performance are generally proprietary and closely guarded, they typically require strong expertise in harmonic conversion methods as well as access to advanced optical coating technology.

Compared to other UV DPSS nanosecond lasers (including Spectra-Physics' older generation technology), the new harmonic conversion technologies allow elevated power levels to be maintained at an extended range of PRFs—well beyond PRFnom—as shown in Figure 1. Indeed, going beyond 3× PRFnom, the power output advantage approaches a factor of 2. Furthermore, the pulse energy remains remarkably stable (well below 5%) out to 5× PRFnom. More conventional UV laser technologies technically do allow operation at such higher PRF values, but beyond about 2–3× the PRFnom, the pulse energy stability degrades very rapidly.

PCB Microvia Drilling with UV Lasers

A common laser via drilling application is microvia formation in Ajinomoto Build-up Film-

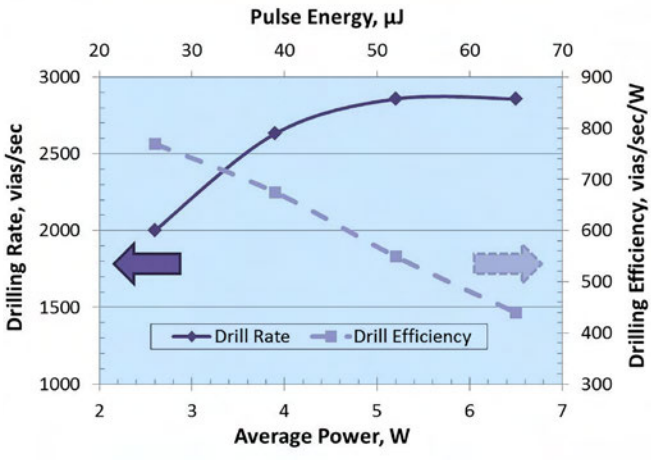


Figure 2: Via drilling rate and efficiency with increasing average power at a fixed PRF. NOTE: This data is at a condition of non-optimized system configuration and process parameter set.

coated thin-rigid copper-clad substrate. The goal is to quickly and cleanly remove the material with minimal copper damage and with a small, controlled amount of sidewall taper angle. Using a pulsed nanosecond UV laser combined with high-efficiency flattop beam-shaping optics, experiments were performed to determine drilling throughput at varying average power levels. The ABF type was GX13 with a thickness of 30 µm, and the targeted via-diameter was in the 50–60 µm range. The power was varied within the range 2–7 W with a fixed PRF of 100 kHz, resulting in a pulse energy window of 20–70 microJoules (µJ). The number of irradiating pulses was varied for each power level, and the minimum count required to cleanly expose the copper substrate was noted. Dividing this number into the 100 kHz PRF generates the maximum theoretical drilling rate in vias per second.

Results of the study are summarized in Figure 2. The rate of drilling is plotted on the left-hand axis and the drill rate per unit Watt of laser power, a measure of efficiency, is on the right-hand axis. As the power and hence pulse energy increases, the drilling rate initially climbs rapidly, approaching 3000 holes per second. Above ~40–50 µJ of energy, however, a saturation regime is encountered and the drilling rate levels off which results in the downtrend in drilling efficiency. This saturation phenomenon is caused by the exponential nature of light extinction in the material, whereby beyond certain fluence (energy per unit area) levels, only marginal increases in ablation depths can be achieved even with large increases in fluence. With UV light and strongly absorbing polymeric materials, this transition can be quite abrupt. A consequence of this phenomenon is illustrated in Figure 2: A doubling of pulse energy from 25 µJ to 50 µJ only resulted in a 1.4× faster drilling/ablation rate, much lower than the 2× one might have expected.

Since the laser used for the tests maintains high power at high PRFs, drilling rates easily exceeding 3,000 vias/sec could be achieved simply by increasing the PRF used for the process. In Figure 3, microscope images of a ~50 µm diameter laser-drilled via show that the ABF is drilled with high quality and with minimal damage to the underlying copper. For this via, 45 pulses at 150 kHz PRF were used, which equates to a drill rate of 3,300 vias per second.

Since small microvias require less energy due to the higher concentration of the beam, it can be a challenge to design a system and define a process that can make efficient use of today's higher power UV sources, which in many cases are designed to operate nominally (i.e., with maximum output power) at lower PRFs and higher pulse energies. One simple way to maximize throughput is to increase the laser's PRF until the optimal combination of pulse energy and pulse rate is en-

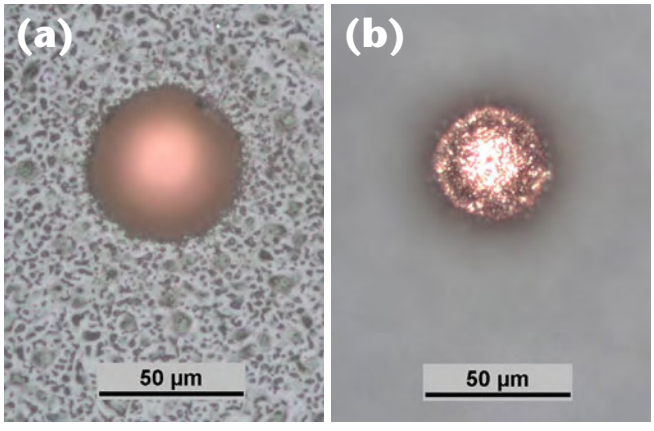


Figure 3: Top ABF surface (a) and bottom copper surface (b) views of a blind microvia drilled with a pulsed UV laser at high PRF with 3,300 holes/sec throughput.

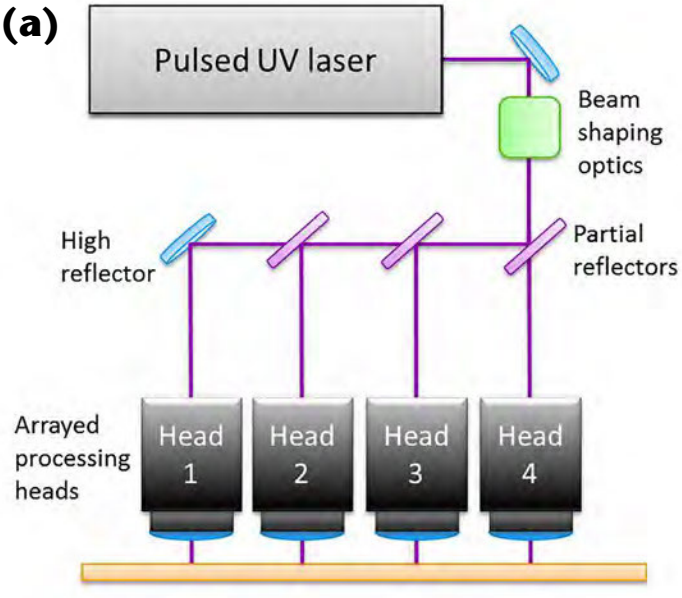
countered, resulting in the most efficient processing and maximum throughput. As an example, consider the case where this optimal combination happens to occur at 200 kHz for a laser having PRFnom of 100 kHz. Both the average power and pulse energy are lower than at PRFnom, but the same number of pulses are emitted in half the time; and although the pulse energy is lower and the per-pulse ablation rate will therefore be lower, the data in Figure 2 indicate it will not be lower by a factor of 2. Hence, a net improvement in the process throughput will be realized. In this fairly common scenario—a mismatch between the design point of a laser and the needs of a specific application—lasers with elevated power levels for an extended range of PRFs are highly advantageous.

There are other ways to maximize the potential of today's higher-power UV lasers. If the optimal energy for efficient processing is significantly lower than the energy at the designed PRFnom for maximum laser average power, then it may make sense to split the beam into multiple lower energy beams and route them to multiple processing heads (as shown in Figure 4a). Using such a configuration, the effective throughput of the processing laser can be further improved compared to the above described approach of simply increasing the PRF. The throughput advantage is greater for smaller vias since they require lower energy and therefore a larger number of beam splits can be made. As an example, Figure 4b contains a table demonstrating the effective via drilling rate for the case of a single beam/high PRF vs. a split beam configuration for drilling ABF blind vias of diameters 50 and 100 µm which using a 15 W UV laser system. With the latest 30 W version of the laser, the throughputs would be about double that of the 15 W model.

Laser Processing for Flex PCB Manufacturing

Not only is packaging becoming smaller, it is by necessity becoming increasingly flexible. Device miniaturization has reached the point where modules can be integrated into very thin items—credit cards, passports, clothing (wearables), even paper—and interconnection and packaging schemes must accommodate the same. In addition, the flex PCBs allow for more versatile and compact arrangements within portable devices, leading to reduced form factors, increased functionality, and design flexibility. With such driving forces, manufacturing of flex PCBs has experienced rapid growth for several years and this is likely to continue.

(a)



(b)

Beam delivery type, efficiency	Drill rate, at via diameter	
	50-60 µm Ø *vias/sec*	100 µm Ø *vias/sec*
Using beam splitting at PRF_{nom} 60% eff.	6000	3300
Single beam, High PRF 75% eff.	3300	2800

Figure 4: Splitting a laser's high-power beam (a) allows higher overall drilling rates (b), especially for smaller diameter vias which require less pulse energy.

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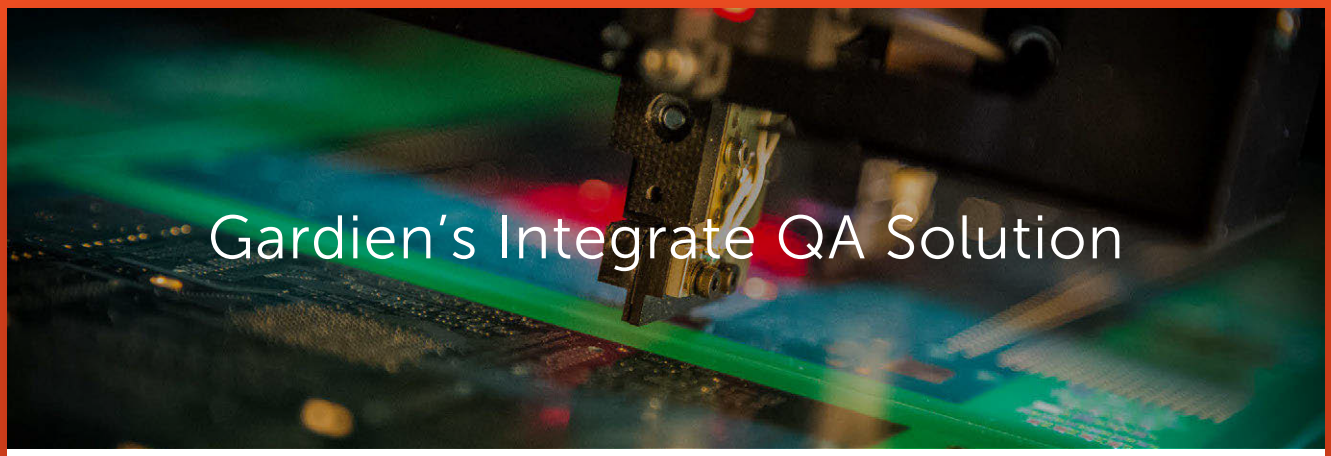

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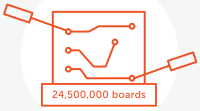

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A commonly used material in flex PCB manufacturing is the copper/polyimide/copper laminate. The foil thicknesses within the laminates have shrunk over time, with copper and polyimide layers currently down to below 10 and 13 µm, respectively, and likely to trend thinner still. Common flex PCB laser processes include profile cutting and both blind and through via drilling. Compared to ABF resin-on-copper via drilling, flex PCB via drilling has the additional requirement that two very different materials—copper and polyimide—must be processed, ideally with the same laser source. As it turns out, CO2 lasers, with their far infrared (~10 µm) wavelengths, are not suitable because the long wavelength light is strongly reflected by the copper. Hence, UV DPSS lasers are used heavily in flex PCB manufacturing.

Using a high-power 30 W UV laser, processes for drilling both blind and through vias have been developed and characterized for drilling throughput. The flex PCB laminate consisted of 1 mil thick polyimide laminated on both sides with ½-mil copper foil. Since the materials are fairly thin, very small vias of 25 µm diameter or below can be percussion drilled using a very small focus spot. The small spot size and strong coupling of the UV light to both the copper and the polyimide allows for processing with relatively low energy levels, which means the laser can be operated at very high PRFs, thereby achieving high drilling rates. If larger vias are required, a larger focus spot could be used (with more energy per pulse from the laser) and for yet larger vias, high-speed beam scanning optics can be employed to rapidly move the tightly focused beam in a circular pattern—a process technique known as trepanning—while the laser is ablating the material. Typically, the small-circle trepanning process is limited by the speed of the scanning optics, and sometimes operating the laser at very high PRFs can result in undesired heat affects. In such cases, a laser with a lower PRF (and therefore lower average power) is preferred in order to match the speed of the beam scanning equipment, thereby ensuring best quality.

For percussion drilling (Figure 5 a, b), throughputs can be very high because there are no moving parts required to drill, and the laser can be operated at a very high PRF since the focus spot is small and therefore energy requirements are reduced. The percussion drilled blind vias in Figure 5 were drilled with a laser-capable drill rate of about 9,000 vias/sec, while the drill rate for the through vias was more than 5,500 vias/sec. Both drill processes used a higher laser PRF of 300 kHz. The trepan drilled via in Figure 5c involved a 2-axis scanning galvanometer processing head that deflected the beam with small circular motion—an approach that is inherently slower compared to percussion ablation. In this case, three repeat scans at 200 mm/s were used, which resulted in an effective drill rate of >250 vias/sec. In this case, the laser PRF was much lower at 60 kHz in order to match the speed of the beam scanning equipment. The 3D optical profilometer data plot in Figure 5d shows the high-quality, much desired, very low edge burring that can be achieved with careful process optimization. In this case, the 2–4 µm edge burr is not much larger than the native roughness of the copper foil.

Coverlay Patterning

In flex PCB manufacturing, coverlay patterning is an important process for cutting various

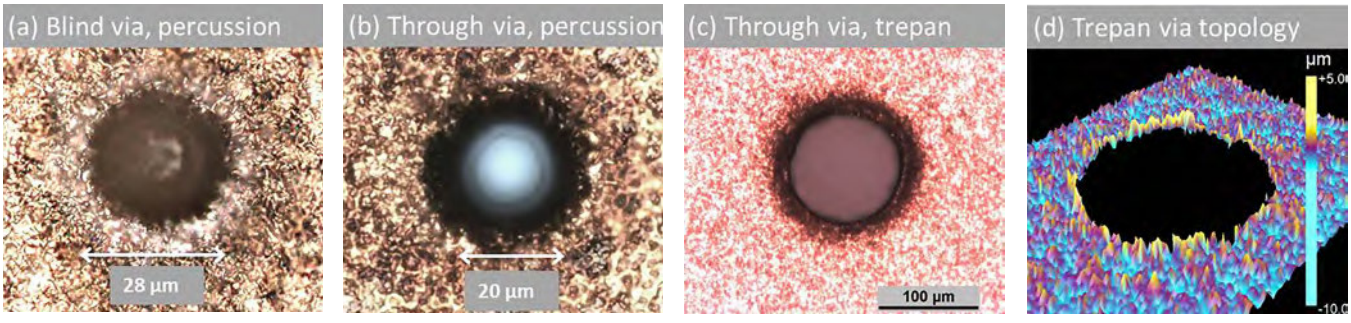

Figure 5: Optical photomicrographs of blind (a) and through (b) vias in Cu/PI/Cu laminate as well as trepanned via (c), and surface topology of trepanned via (d) generated with pulsed UV lasers.

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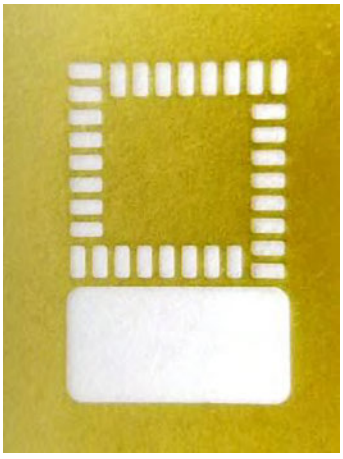
geometric shapes in a thin polyimide sheet which may be loosely adhered to a paper backing. The coverlay itself is then adhered to a flex circuit as a protective layer, and its purpose is functionally analogous to that of solder mask for rigid PCBs. In some cases the polyimide and adhesive are attached to a release paper, and it is important to have non-thermal ablation of a UV laser source to avoid burning the paper. To cut through the materials, high energy levels are not necessarily required because the sheets are very thin which allows a very small focus spot to be used (smaller focus spots are also more divergent and hence less suitable for cutting thicker materials). If this energy can be applied at very high PRFs, then high patterning speeds can be achieved accordingly. As UV laser power is varied from 6 W upwards to 30 W, different patterning speeds can be achieved with either a single beam, high-PRF approach or a more advanced beam splitting tool design.



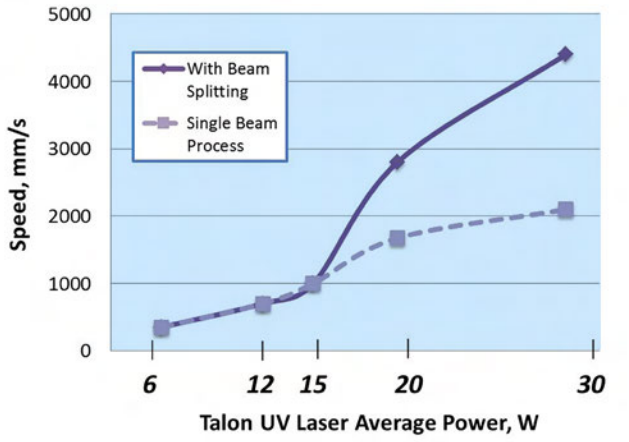


Figure 6: Coverlay patterning—high-speed cutting of thin polyimide, can benefit greatly from a split-beam system configuration.

At lower power levels, the increase in processing speed is approximately linear with increasing average power. However, when transitioning to 20 W UV a stronger throughput advantage is realized. This is because lasers at 20 W UV and higher are typically designed for a higher PRF-nom (100 kHz vs. 50 kHz), which means even higher energy is still available at the very high PRFs. Furthermore, the advantage of beam splitting becomes increasingly significant because several multiples of the required pulse energy are available at the higher powers. Higher power levels allow for more beam splits, such as 2× beams for 20 W and 3× beams for 30 W.

Conclusion

Pulsed ns UV DPSS lasers have been rapidly making inroads into high-volume advanced high-density PCB manufacturing for many years, and the drive to thinner, more flexible PCBs is likely to maintain if not accelerate the trend. For most laser product offerings on the marketplace, however, the output power is sufficiently high for only a small range of pulse output frequencies, which limits the flexibility of the laser and hence narrows its application space. More recently, with new UV laser technology, a substantial broadening of the application space is achieved due to the ability to maintain high power levels at high PRFs. The technology is also conducive to lower cost of manufacturing which can further expand the serviceable application space. With continued technology development for UV DPSS lasers expected to further increase the availability of higher power, low cost, reliable laser products, further miniaturization of electronic circuitry and packaging thereof should lead not only to the improvement of current electronic devices, but may also help accelerate more nascent industries such as the manufacturing of wearables.

Acknowledgements

The author would like to thank Robert Sposili and Andrew Tian for their technical contributions and Raj Patel for his editorial guidance and support. **PCB**

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Via Formation and Drilling Mechanics, Part 1

by Michael Carano
RBP CHEMICAL TECHNOLOGY

Introduction

In the extensive process of printed circuit board fabrication, one of the steps involves mechanically drilling through-hole vias. Via formation is then followed by desmear and metallization. The quality of the through-hole drilling process (and by inference the quality of the drilled through-hole) or lack thereof will also impact the desmear and metalization processes. While drilling equipment, tools and methods have been continually improved over the years, the fabricator must adhere to strict guidelines with respect to maintenance of the equipment, quality of the drill bits, the drilling operation parameters as well as the proper selection and use of entry and back-up materials. When simple maintenance of drill equipment and drill bits is lacking, drilled hole wall quality deteriorates. This then leads to defects in the PTH that are not attributable to the plating processes such as electroless copper. However, for this month's edition of "Trouble in Your Tank," I will present some of the basics of drilling.

Drilling Basics

Through-holes are formed by the cutting action of drill bits in numerically-controlled drilling machines. Figure 1 shows a five-head drilling machine.

There are multiple factors to consider when mechanically drilling plated through-holes as well as blind and buried vias (assuming mechanical drilling will be used on a few applications for blind/buried vias). These include the drill machine, drill bits, entry and back-up materials, drilling parameters, stack heights, etc. In addition, the type of resin that makes up the circuit board, along with glass weave style and content, will play a role in via drilling quality. This will be the subject of a future column of "Trouble in Your Tank."

Figure 2 depicts what can happen when the drilling operation is not in control. Note the gouges in the resin and the torn out glass bundles. When a drilled hole such as this makes its way to the PTH (plated through-hole) process, the ability of the electroless copper or direct metallization chemistries to properly deposit in

Figure 1: Five-head drilling machine.

Figure 2: Rough hole walls due to less than optimum drilling (Source: IPC photo archive).

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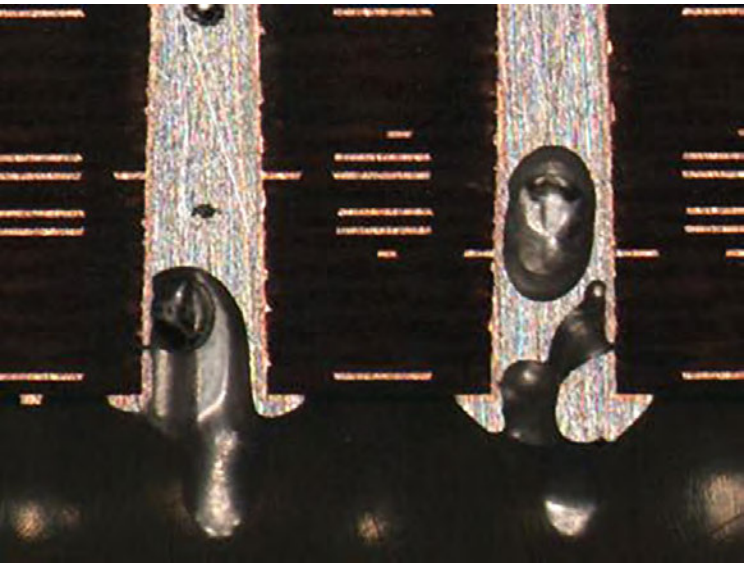


Figure 3: Large air pockets show where gas or moisture was expelled during the assembly process.

these drill gouges is compromised. Even if the PTH metallization is successful, subsequent electrodeposition of copper will yield areas where the copper thickness is either too thin (thus violating copper thickness requirements) or potentially having a situation where the plated copper folds over. In the latter case, the copper cannot level due to the drill gouge. This leaves a very thin area and leads to the potential for a blowhole in assembly or an open in the PTH. This is precisely why many finished bare boards successfully pass in-circuit test—only to exhibit some interrelated non-conforming defect after assembly (Figure 3).

Certainly, it is possible that there may be issues with the wave solder flux. But for purposes of this discussion, assume flux is not contributing to the issue. Note the areas of thin copper plating, small voids and rough hole walls. All of these issues will contribute to the potential for the occurrence of blow holes. While it is possible that thin copper plated deposits and voids can be attributed to the plating processes, these issues can also be directly related to poor hole drilling conditions. That is why the old adage "Garbage in, garbage out" applies here. One cannot expect plating chemistries to defy physics and Faraday's Law and always make up for poor hole wall conditions as shown in Figure 2.

Drilling and Basic Definitions

Drilling conditions depend on the drilling machine, brand of drill bit, drill bit design, type of spindle, stack height, PCB material, amount of copper to be drilled, drill aspect ratio, entry and backup materials, etc. Hole wall quality, drilling accuracy, and the potential of drill bit breakage are results of the combined effect of all drilling parameters.

Let's review a few very key drilling parameters and their definitions:

Feed Rate: The speed of a drill bit toward and through the circuit board stack to be drilled. Feed rate is measured in meters per minute (m/minutes) or inches per minute (IPM). One of the key parameters of chip load.

Spindle Speed: RPM or rotational rate of the drill spindle. The other key parameter of chip load.

Chip Load: The depth or distance through a stack that a drill bit travels for each revolution it turns. Chip load is typically measured in mils or inches per revolution (IPR), or micrometer per revolution (µm/rev).

In order to calculate chip load, use the following equation:

$$\text{Chip Load (IPR)} = \frac{\text{Feed Rate (IPM)}}{\text{Spindle Speed (RPM)}}$$

So, chip load in inches per minute is determined by feed rate of the drill spindle divided by the rotational rate of the spindle. One may also calculate chip load in mils of feed divided by the RPM of the spindle.

Variation in the feed rate and chip loads affects hole wall quality. On the positive side, low feed rates will improve hole positional accuracy. On the negative side, low feed rates will cause excessive heat, resulting in smear and nail heading. Low feed rates may also cause glass fiber damage resulting in wicking of copper plating chemistries. On the positive side, high feed

rates will reduce resin smear. On the negative side, high feed rates can cause burrs, hole wall roughness and debris in the holes.

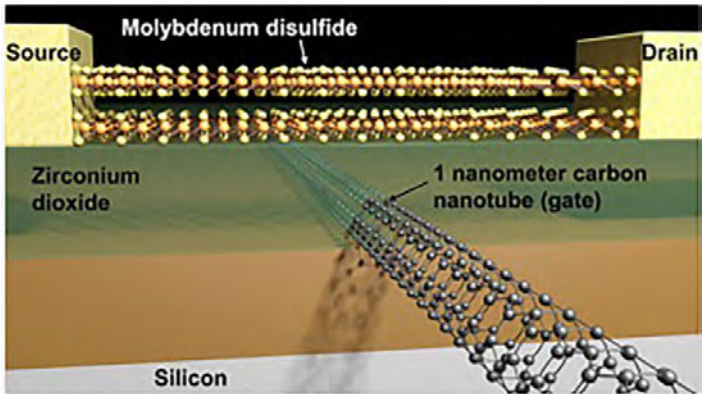
Per standard drilling guidelines, smaller diameter holes and thicker boards require lower chip loads. In part 2 on this subject, I will present more in-depth information on drilling and its ramifications on PTH quality and reliability.

Summary

When this monthly column first appeared on the pages of The PCB Magazine, five years ago, it was suggested that producing high-quality, high-reliability printed circuit boards requires strict adherence to processing guidelines along with vigilance in understanding and executing on the principles of trouble-shooting. A thorough understanding of each of the process steps is critical in minimizing or eliminating non-conforming defects—the ones that cost the fabricator money and can lead to lost customers. Each process must be deeply understood on its own merits. Mechanical drilling is one such process. **PCB**

Michael Carano is VP of technology and business development at RBP Chemical Technology. To read past columns or to contact Carano, click here.

Smallest. Transistor. Ever.



For more than a decade, engineers have been eyeing the finish line in the race to shrink the size of components in integrated circuits. They knew that the laws of physics had set a 5-nanometer threshold on the size of transistor gates among conventional semiconductors, about one-quarter the size of high-end, 20-nanometer-gate transistors now on the market.

Some laws are made to be broken, or at least challenged.

A research team led by faculty scientist Ali Javey at the Department of Energy's Lawrence Berkeley National Laboratory has done just that by creating a transistor with a working 1-nanometer gate. For comparison, a strand of human hair is about 50,000 nanometers thick.

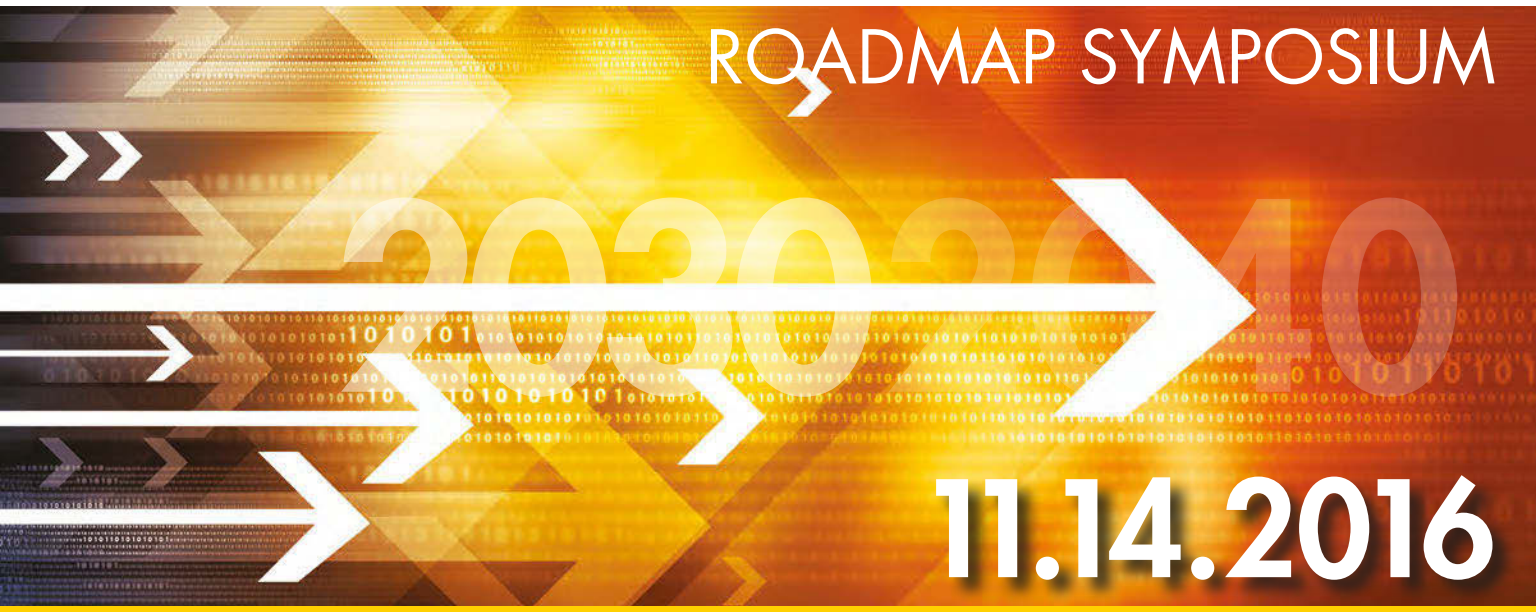
"We made the smallest transistor reported to date," said Javey, lead principal investigator of the Electronic Materials program in Berkeley Lab's Materials Science Division. "The gate length is considered a defining dimension of the transistor. We demonstrated a 1-nanometer-gate transistor, showing that with the choice of proper materials, there is a lot more room to shrink our electronics."

The key was to use carbon nanotubes and molybdenum disulfide (MoS2), an engine lubricant commonly sold in auto parts shops. MoS2 is part of a family of materials with immense potential for applications in LEDs, lasers, nanoscale transistors, solar cells, and more.

The findings were published today in the journal *Science.* Other investigators on this paper include Jeff Bokor, faculty senior scientist at Berkeley Lab and professor at UC Berkeley; Chenming Hu, professor at UC Berkeley; Moon Kim, professor at the University of Texas at Dallas; and H.S. Philip Wong, professor at Stanford University.

The development could be key to keeping alive Intel co-founder Gordon Moore's prediction that the density of transistors on integrated circuits would double every two years, enabling the increased performance of our laptops, mobile phones, televisions, and other electronics.

2016 SEMICONDUCTOR PACKAGING ROADMAP SYMPOSIUM



MEPTEC INITIATES COLLABORATION WITH HETEROGENEOUS INTEGRATION ROADMAP

MONDAY, NOVEMBER 14, 2016 | SAN JOSE, CALIFORNIA

SYMPOSIUM 8:00AM - 5:00PM | EXHIBITS 9:30AM - 6:30PM | RECEPTION 5:00PM - 6:30PM

In this post ITRS era, there is great need for the industry to collaborate in charting a direction into the future. In 2015, the SIA announced their decision to bring ITRS to a close, with the 2015 edition being the final edition. The IEEE CPMT Society took the initiative to establish a technology roadmap focused on heterogeneous integration, to be modeled after the ITRS in purpose, structure, and governance. This initiative quickly found resonance with SEMI, and the IEEE Electron Devices Society (EDS) joined the effort, resulting in the launch of the Heterogeneous Integration Roadmap (HIR). **MEPTEC has moved to participate in this roadmap collaboration.**

MORNING KEYNOTE SPEAKER

Wilmer R. Bottoms, Ph.D.

Chairman, Third Millennium Test Solutions
Co-chair, Heterogeneous Integration Roadmap (HIR)

AFTERNOON KEYNOTE SPEAKER

William (Bill) Chen, Ph.D.

ASE Fellow and Senior Technical Advisor, ASE Group
Co-chair, Heterogeneous Integration Roadmap (HIR)

MORNING SESSION:

Strategic Directions in Heterogeneous Integration

The morning session will address the strategic directions in heterogeneous integration that address the market inflection points and technology fault lines. What will be the crucial roles for integrated phonics for data to the cloud, and for sensing? What technologies will be developed and implemented for the self driven cars be introduced into our cities and byways? How embedded sensing will enable the transition from IoT to IoE around the world.

AFTERNOON SESSION:

Innovations in SiP and Integration

This session will address the major developments in heterogeneous components – power devices, analog, MEMS sensors, photonics, and in SiP integration – fan out, 2.5D, embedded, and co-design technologies. How will the momentum of these technology developments move forward to address road blocks moving ahead? What research areas and ecosystem collaboration will be needed for continued progress? These and more questions will be addressed.

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Electronics Industry News
Market Highlights

Enterprise Wearables Find First Inflection in Industrial and Field Service Markets

The warehouse and manufacturing vertical, along with field services, represent one-quarter of the wearable devices shipped to enterprise end users in 2016. With device hardware improvements from companies like Epson, Microsoft, ODG, and Vuzix, ABI Research forecasts shipments to these segments will more than triple to top 35 million units in 2021.

Four IC Industry Clusters Emerge with China's 13th Five-Year Plan

According to the global market research firm TrendForce, committed policy efforts and investments from the Chinese government have resulted in the formation of four IC industry clusters that are respectively located in the country's four major regions of activities: the Yangtze River Delta, the Pearl River Delta, the Beijing-Tianjin Bohai Sea region and the Central-Western region.

Energy-efficient Lighting Technology Industry: Growing Demand for LEDs Vital for Global Market

The global energy-efficient lighting technology market is dominated by players such as OSRAM GmbH, GE Lighting, and Royal Philips Electronics. According to Transparency Market Research, focusing on the development of energy-efficient LED lighting is likely to a popular strategy among leading players in the global market in the coming years.

Energy Management: Highly Intelligent Homes of the Future

For 18 months, Prof. Franz Hagn and his family experienced for themselves what it is like to live in a house that not only produces its own energy, but also manages it intelligently. The concept of the "e-MOBILie" project also included an electric car. What the results show: On a small scale, the pilot project is a present-day implementation of the functions of a smart grid of the future.

IoT Revolution Revitalizes Demand for High-end Flexible Sensors

The global market for printed and flexible sensors is predicted to reach $7.51 billion by 2020. By type, the global printed and flexible sensors market will be led by the biosensors segment, followed by the Pizoelectric sensors segment.

Human Brain Project: Pilot Systems for Interactive Supercomputer

The Jülich Supercomputing Centre has begun operation of two new pilot systems for an interactive supercomputer. The systems—JULIA, created by Cray, and JURON from IBM and NVIDIA—are specifically designed for applications in the neurosciences.

New 3-D Wiring Technique Brings Scalable Quantum Computers Closer to Reality

Researchers from the Institute for Quantum Computing (IQC) at the University of Waterloo led the development of a new extensible wiring technique capable of controlling superconducting quantum bits, representing a significant step towards to the realization of a scalable quantum computer.

DARPA's Microsystems Technology Office Streamlines Contracting for Innovators

DARPA's Microsystems Technology Office (MTO) has a proud history of making seminal investments in breakthrough technologies that ultimately became critical components in our electronics-filled world, from flash memory to radio frequency (RF) semiconductors to microelectromechanical systems (MEMS).

T-rays will 'Speed Up' Computer Memory by a Factor of 1,000

Together with their colleagues from Germany and the Netherlands, scientists at the Moscow Institute of Physics and Technology (MIPT) have found a way to significantly improve computer performance.

IPC Releases PCB Industry Results for August 2016

IPC—Association Connecting Electronics Industries announced the August 2016 findings from its monthly North American PCB Statistical Program.

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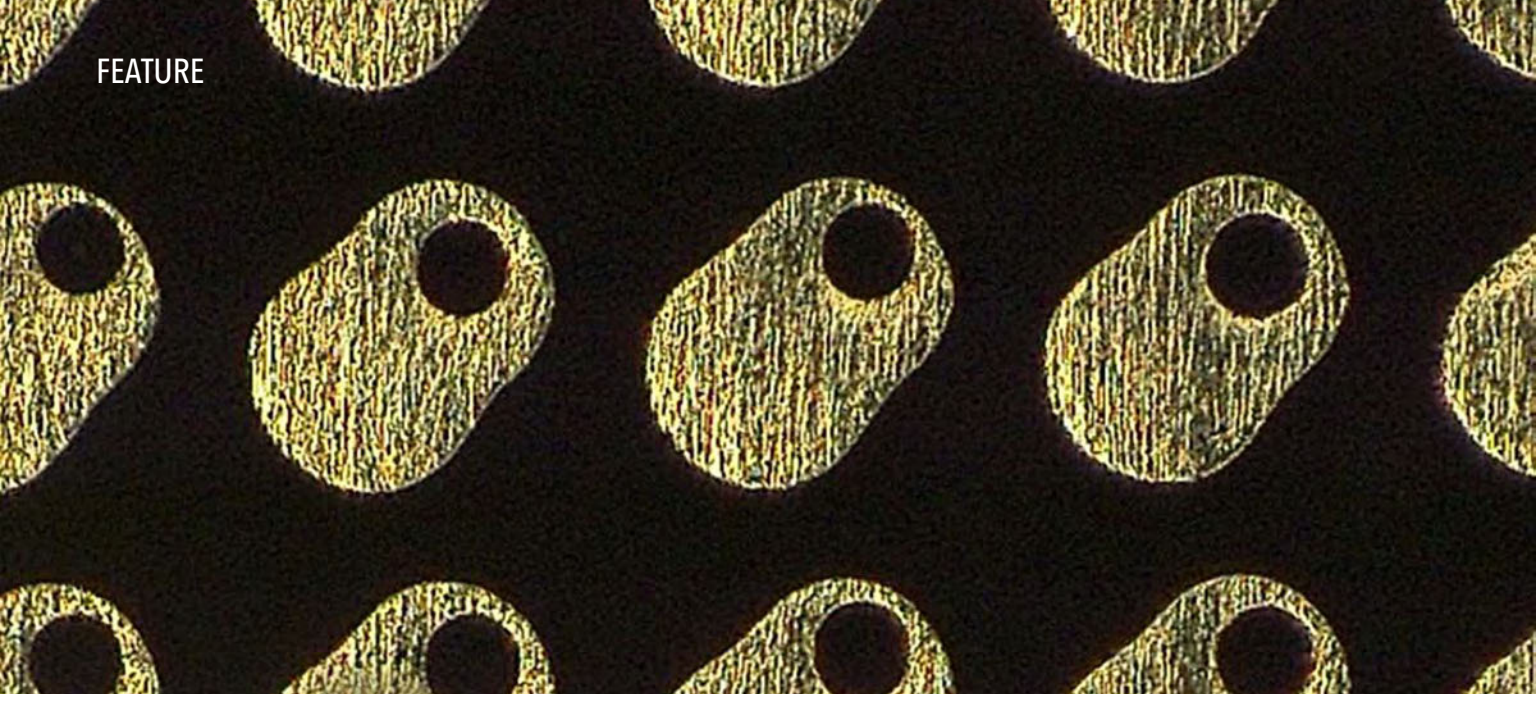

Unique Implementation of a Rigid-Flex Circuit

by John Dangler, IBM;
Jeffrey Taylor, LENOVO;
and Cynnthia Verbrugge, AMPHENOL

Editor's Note: This paper was originally presented at IPC APEX EXPO 2016 and published in the proceedings as: *Unique Implementation of a 15-Layer, Unbonded/Looseleaf, Bookbinder Rigid-Flex with Backdrill and LGA Interconnect*.

Abstract

While flex and rigid-flex (IPC-6013 Types 1 through 4[1]) have always been important in 3D packaging to help resolve space constraints and meet other design requirements, the continued push for denser packaging and higher performance has only increased the demand for more complex interconnects. Often, we forget that a flex is more than a mechanical solution but that it is a critical part in controlling signal integrity and meeting other electrical performance requirements. Any design must be manufacturable, reliable, and meet cost constraints.

We will be examining a packaging solution for a server application that met all requirements through a combination of key design points, including:

- Rigid-flex (IPC-6013 type 4)
- 15-layer cross-section
- Unbonded/looseleaf construction
- Bookbinder construction
- Backdrill
- LGA (land grid array) interconnect

Cost, manufacturability, reliability, signal integrity, thermal and mechanical requirements were all considered during development. The collaborative efforts of mechanical development, signal integrity modeling and input, qualification engineering, production engineering, cost engineering, sourcing team support and manufacturability and cost feedback from the fabricator were key to creating a final design that was an optimum balance considering various trade-offs.

More than a simple stack of circuit materials, the unbonded/looseleaf, bookbinder cross section and LGA interconnect was able to meet the tight rigid-flex mechanical bend radius requirements and the small interconnect footprint requirements. The flexibility of the rigid-flex met the system mechanical requirements related to tolerances between the two mating LGA interconnect areas. Critical signal integrity requirements were met through the selected cross-section, backdrill and the utilizing an LGA interconnect solution.

This paper includes details as to how we went from concept to initial development, to design iterations and prototyping, through qualification into a final product in volume production.

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Introduction

In developing any server, especially high density, scalable, high performance blade servers, significant electronic packaging challenges are encountered. High speed, dense interconnect between blades is often required to achieve desired system performance.

In the application described in this paper, challenging space, signal integrity, cost, scalabilty and usability requirements were defined for signal interconnect between blades. An interconnect solution using rigid-flex cables, LGA interconnect and scalability cards was proposed (Figure 1).

Construction

While flex may be ideally suited for applications requiring interconnects within a tight form-factor, not all flex constructions are up to the job of delivering high density interconnects when space is at a premium. This application required we bend 13 conductive layers 90 degrees within a span of 15.25 mm. Adding to the difficulties associated with such a severe bend was the impedance requirements on the five signal layers. Impedance control and good signal integrity properties depend on thick innerlayer dielectrics resulting in a significantly thicker flex than standard non-impedance controlled circuit.

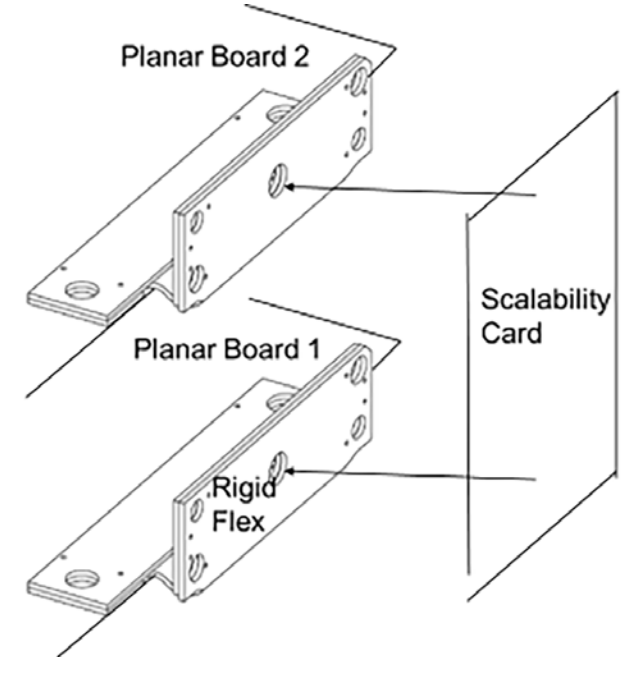


Figure 1: Original interconnect concept.

Why Type 4 (rigid-flex)

Special considerations are required when building high layer-count FPCs (flexible printed circuits). A standard construction multilayer (IPC-6013 type 3) is adequate for most applications; however, as layer count rises, or more importantly circuit thickness increases, special attention must be paid to the materials used within the stack. Of primary importance is CTE (coefficient of thermal expansion) match between all materials within the stack. As seen in the Figure 2, a large portion of the stack-up is comprised of acrylic adhesive from the bond plys.

In Figure 3, we can see the materials that make up the typical IPC type-4 multilayer. Successive layers of dielectric, adhesive, and conductive layers make up the flex. When it comes

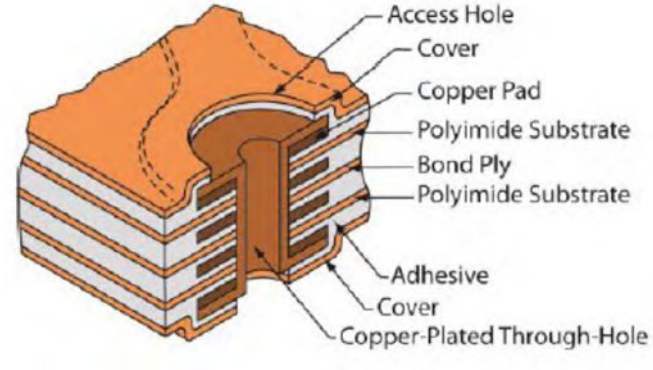


Figure 2: Typical type 3 construction.

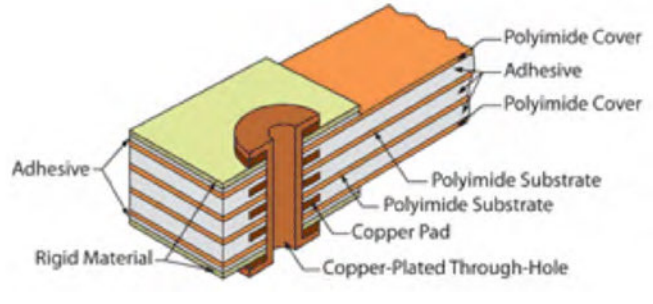


Figure 3: Typical type 4 rigid-flex construction.

FR-4 (rigid material)	50-70 ppm/°C
Polyimide	100-105 ppm/°C
Acrylic Adhesive	100 ppm/°C (400 ppm/°C >Tg)
Note: Acrylic Tg 40°C	

Table 1: Common CTE values for flex materials (z-axis).

to PTHs (plated through holes) the expansion of the materials in the z-axis with temperature rise becomes a real concern. As the material 'swells' in the z-axis it creates strain on the plated barrel—with enough strain the barrel cracks, resulting in an electrical open. It is important the CTE match as closely as possible. The most common flex materials have a pretty good CTE match in the 'x' or 'planar' direction, but not so for the 'z'.

As we can see in Table 1, once we rise above the Tg (glass transition temperature) of acrylic adhesive at 40°C, our z-expansion rises to 4x the rate of the other materials in our stack. This is the critical reason we moved to a rigid-flex type 4 construction with cutback coverlay and acrylic bonding films. These layers were stopped in the flex/rigid transition zone. This eliminated acrylic adhesive in the via area. The cutback coverlay and acrylic bonding films can be seen in Figures 7 and 8.

A note on the Tg value regarding acrylic adhesive. There can be concern on the part of designers when they see a Tg value of 40°C. This is really of no concern as long as proper design considerations are followed in our stack-up. Acrylic adhesive is uniquely qualified for use in FPCs. Its properties are both thermo-set and thermoplastic. It is exactly these properties that allow the multiple lamination cycles required when building up a multilayer with several sub-composites. FPCs of this construction are often rated for a MOT (maximum operating temperature) of 105°C. Many flexes of this construction are operating at elevated MOTs of 150°C for extended time with no detrimental effect.

Bend Radius Considerations

IPC-6013 recommendations state that a flex circuit should have a minimum bend radius of 10-times its thickness. As far as guidelines go, this one is pretty safe, however it fails to account

Progressive layer lengths	
Flexible layers	Overall width (mm)
2, 3, 4, 5	47.46
6, 7, 8	46.69
9, 10, 11	45.92
12, 13, 14	45.16

Table 2: Progressive lengths of sub-composites.

for initial part thickness or material type. A very thin flex can go significantly tighter, even folding over on itself, whereas a thicker circuit may require a more relaxed bend. In our application we had to bend a very thick circuit of 0.965 mm (0.038″)—if we did not use an unbonded/loose-leaf design. Our calculated minimum allowed radius per IPC-6013 would have been 9.65 mm (0.38″). In real-life situations radii are not perfect and we often require a bit more flex length for a comfortable installation. We had an unbonded flex section length of 15.25 mm to form our flex to 90 degrees. Our 'real world' finished radius requirement was determined to be 2.54 mm (0.1″) for best fit. This makes our planned design 3.8 times tighter than allowed by industry design standards without unbonded/loose-leaf/bookbinder.

In a typical instance where we must go below the minimum recommended bend radius, we would incorporate a 'loose-leaf' approach. Individual layers would be separated within the flex stack-up (Figure 5). By separating the layers into multiple sub-composites within the stack-up, we can recalculate our minimum bend radius based on the thickness of the individual layer. This can be quite effective; however, in our situation we still had a flex region of only 15.25 mm. Even unbonded layers would not allow for enough give within the stack to allow for a stress-free bend.

The Bookbinder

By making each of our unbonded sub-composites slightly longer than the one below it, we can allow room for our sub-composite to bend without applying undue stress to itself or

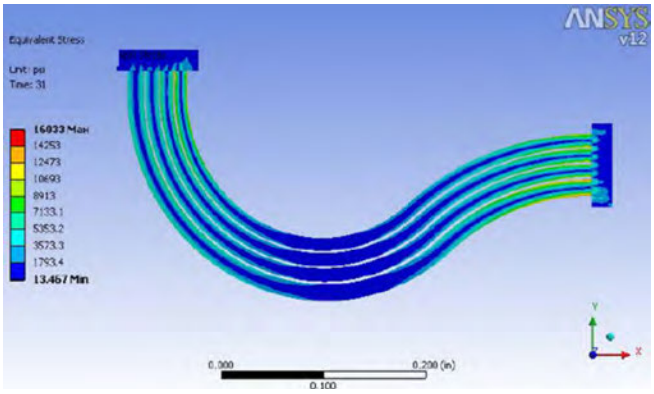


Figure 4: Sub-composite stress model.

the layer immediately adjacent to it. Each sub-composite length is calculated to allow the sub-composite to rest under it without interference.

By virtue of our thickest sub-composite now being 0.3 mm (0.012") we can recalculate our minimum bend radius based on this new value. We now have a recommended minimum bend radius of 3.0 mm (0.12"), one-third of our original design minimum!

Stress Applied in Flex Zone During Form

Using the materials above the stress-forces on the book-binder portion of our rigid-flex were calculated.

Plane strain allowed for a 2D cross-section. Contact between sub-composites was modeled allowing the effect of sub-composites coming into contact with each other to be observed. As there are no direct modeling parameters for flex materials, assumptions had to be made. The flex layers were all assigned the same modulus with the rigid sections being treated as steel.

As seen in Figure 4, the reactive force between the two ends of the rigid-flex was analyzed.

Final Rigid-Flex Stack-up and Microsections

Figure 5 shows the final stack-up. Figure 6 shows the construction without cutback cover-

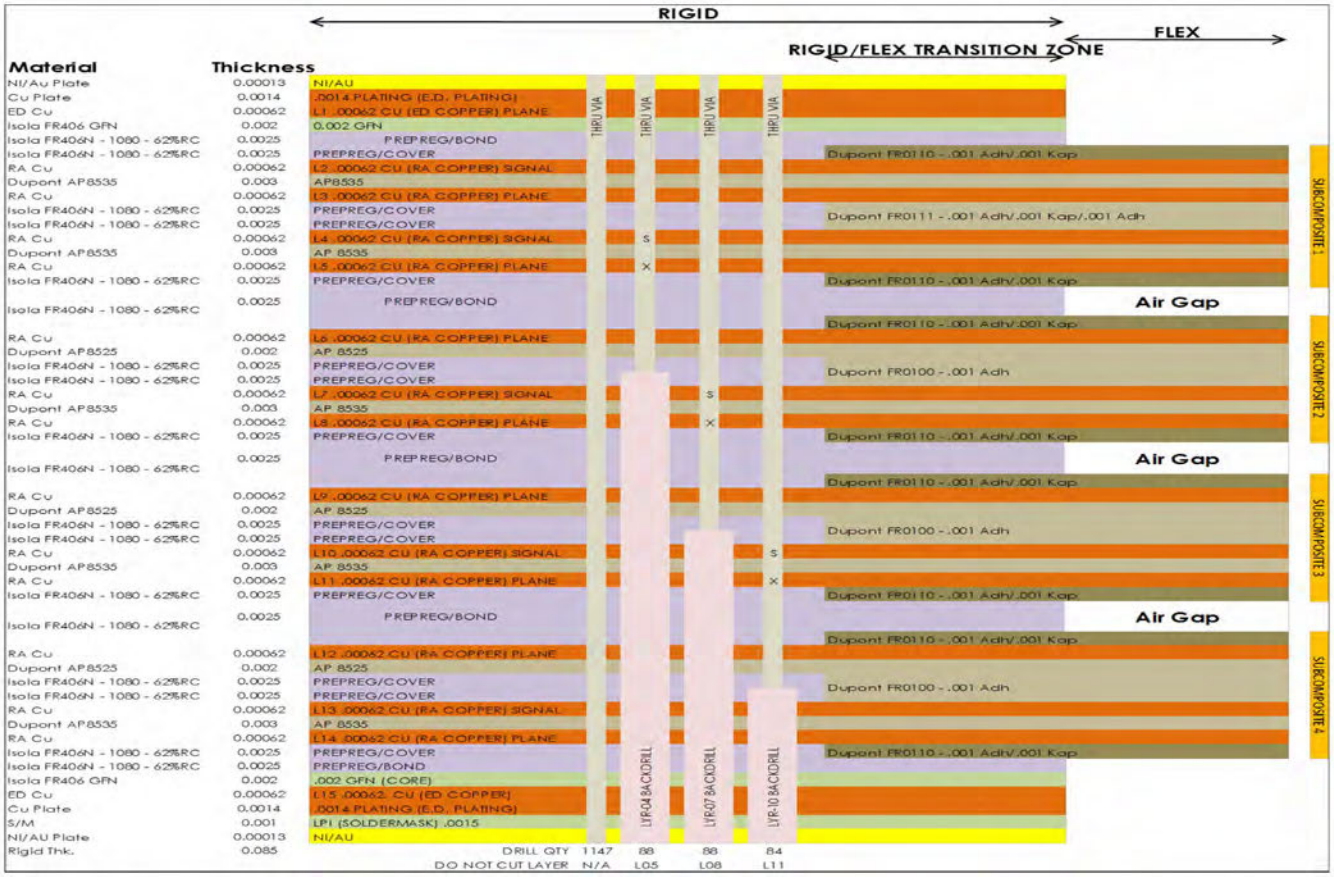


Figure 5: Final bookbinder rigid-flex stack-up.

lay/acrylic bonding film which would have put 8 mils of acrylic adhesive in the via area, which is not preferred per previous discussion and was not used. Figures 7 and 8 show microsections of the final product. Figure 9 shows a microsection of vias in the rigid area.

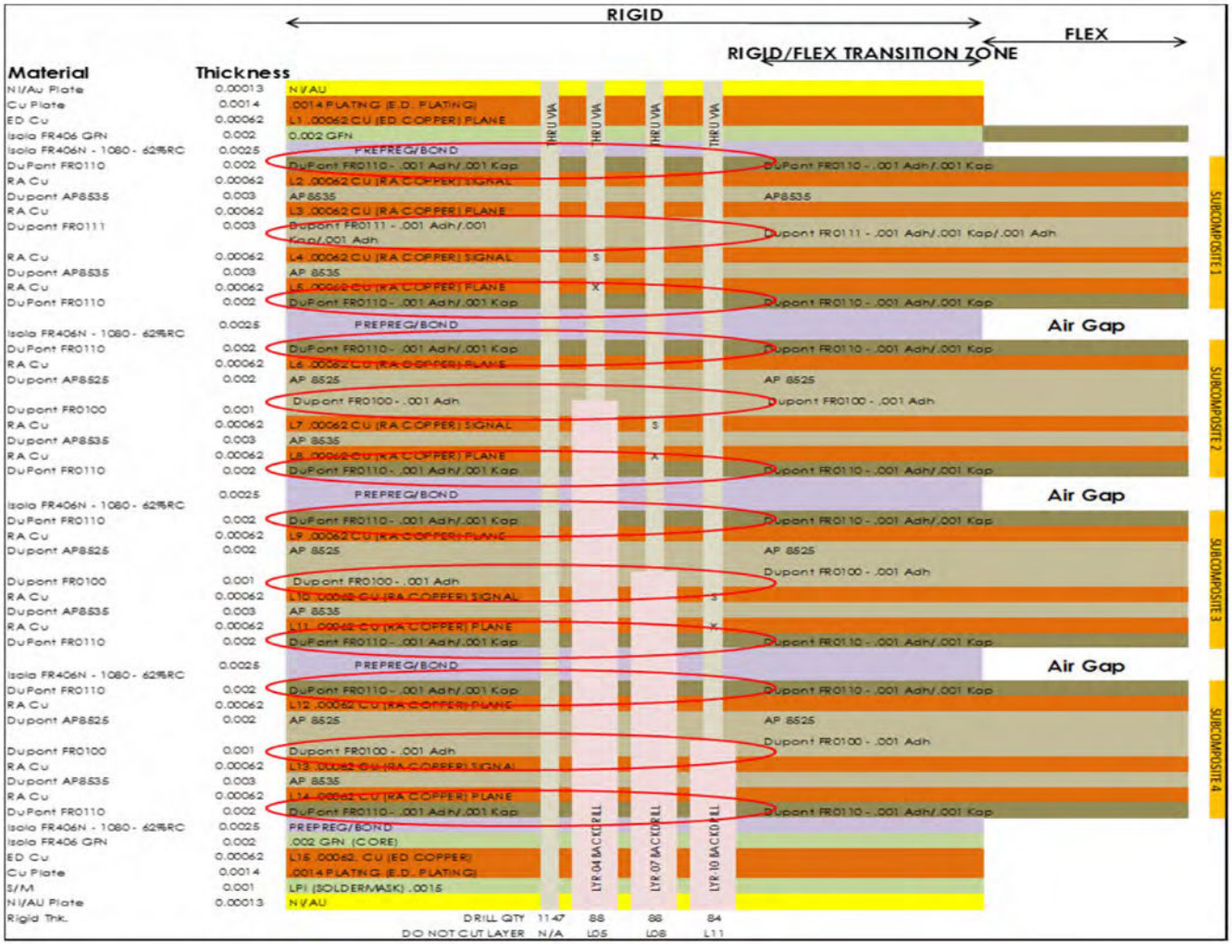


Figure 6: Alternate stack-up without cutback coverlay/acrylic bonding film (not used).

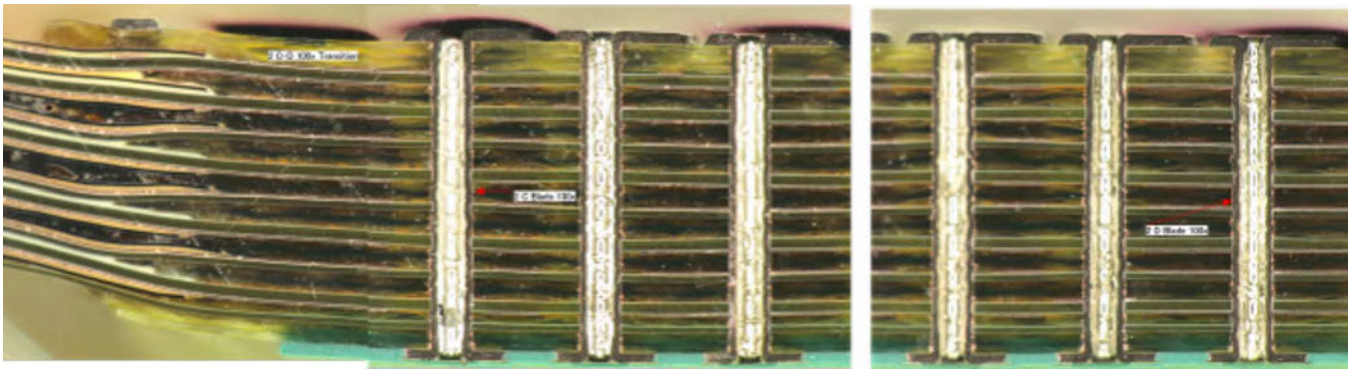


Figure 7: Microsection of flex/rigid transition zone and rigid section (with vias).

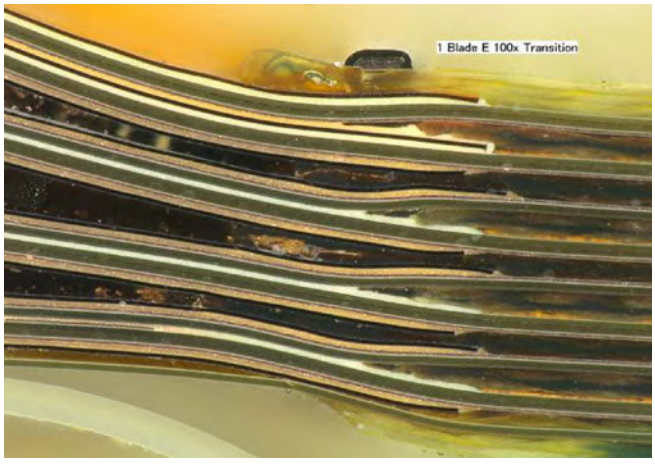


Figure 8: Microsection of flex/rigid transition zone.

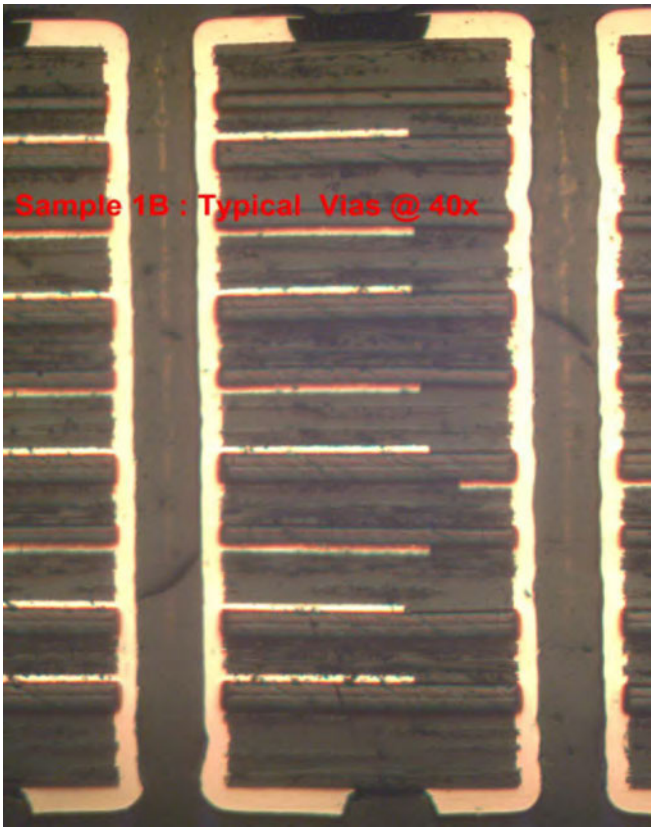
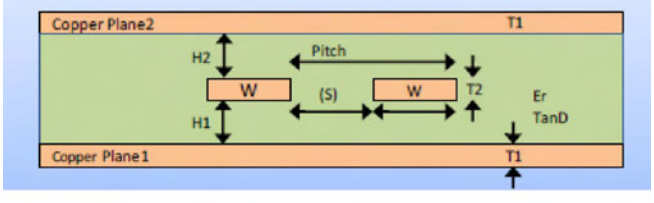


Figure 9: Microsection of vias.



Var	Desc.
W	Trace Width
Pitch	In pair pitch
(S)	In pair airgap (Pitch - W)
T1	Copper Plane Thickness
T2	Signal conductor thickness
H1	Dielectric thickness below signal conductor
H2	Dielectric thickness above signal conductor
Er	Dielectric constant
TanD	Dielectric loss tangent

Figure 10: Impedance calculation parameters.

Impedance Considerations, Calculations

Adding to the complexity of this design is the requirement for multiple impedances, both stripline and microstrip. Critical signals were kept off the microstrip layer (layer 2).

Stripline Modeling

Stripline modeling was straight forward. With our signal layers lying completely between the return planes there is no impact on impedance values due to proximity of adjacent layers. Calculations are straight forward and the resulting values are consistent between unbonded layers in the flex. Loss per inch @ 3.2 Ghz are recorded for each line width.

Part size, Panelization and Costs

The rectangular shape of the product and 78 mm x 45 mm overall size allowed for good panelizations even with panelization considerations for the bookbinder manufacturing processes. Initial production was done 28 up on a 457 mm x 610 (18" x 24") panel. Production was moved to 60 up on a 610 mm x 914 mm (24" x 36") panel to reduce costs. A second low-cost geography manufacturing site was qualified using a 229 mm x 305 mm (9" x 12") panel size.

General Development and Qualification Activities

During product development, backdrill was added to the product requirements to improve signal integrity margin. The backdrill requirement was added to vias with the three longest stub lengths covering 260 vias. The vias with the shortest stubs did not require backdrill. Fig-

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RUN#	W	Pitch	(S)	T1	T2	H1	H2	Er	TanD	Zd	Loss dB/in @3.2Ghz	Notes	Reaction Force (lb) (see pg 11-21 for details)	
Stripline - 0.5 oz copper, 3 mil cores					Nominal Design Point								up/down	Left/Right
1	3.2	9.8	6.6	0.65	0.65	3	3	3.3	0.01	92.7	0.43	min trace width	12.5	92.5
2	3.8	9.8	6							84.6	0.42	nominal trace width		
3	4.4	9.8	5.4							76.6	0.41	max trace width		
Stripline - 0.25 oz copper, 3 mil cores														
4	3.5	9.8	6.3	0.33	0.33	3	3	3.3	0.01	93.5	0.46	min trace width	5.6	41.5
5	4.2	9.8	5.6							84.0	0.44	nominal trace width		
6	4.8	9.8	5							77.2	0.44	max trace width		
Stripline - 0.25 oz copper, 2 & 3 mil cores														
7	2.8	9.8	7	0.33	0.33	2	3	3.3	0.01	93.1	0.53	min trace width	4.1	30.3
8	3.3	9.8	6.5							85.0	0.52	nominal trace width		
9	3.9	9.8	5.9							76.9	0.50	max trace width		
Stripline - 0.25 oz copper, 2 mil cores														
10	2.3	9.8	7.5	0.33	0.33	2	2	3.3	0.01	93.5	0.59	min trace width	2.8	20.8
11	2.8	9.8	7							84.0	0.58	nominal trace width		
12	3.2	9.8	6.6							77.8	0.56	max trace width		
Taconic Stripline - 0.5 oz copper, 3.4/2.0 mil core,												Nominal design point		
19	3.5	9.8	9.8	0.65	0.65	3.4	2.1	2.6/2.45	0.001	93.3	0.29	min trace width	13.3	98.1
20	4.1	9.8	9.8							85.2	0.29	nominal trace width		
21	4.8	9.8	5.1							77.1	0.30	max trace width		

Figure 11: Impedance modeling results.

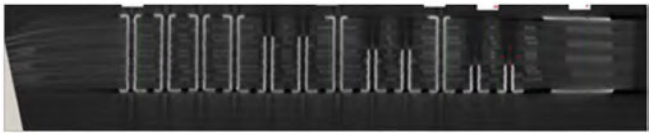

Figure 12: 3D X-ray image of rigid-flex section including backdrill.

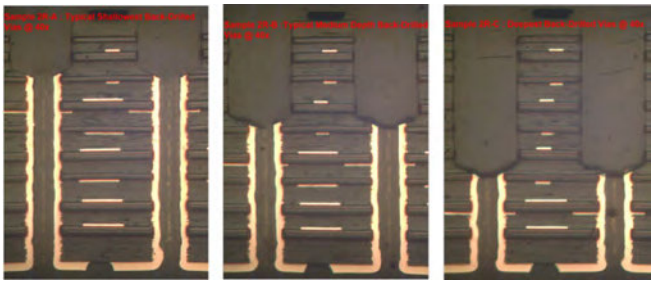

Figure 13: Microsection of three backdrill depths.

ure 12 shows a 3D X-ray image of the product with backdrill. Figure 13 shows microsection mounts of the three backdrill depths.

Via hole copper plating minimum average requirements for through-holes is higher for flexible printed boards than for rigid boards. Type 3 and 4 flexible printed boards have a 25 µm (984 µin) minimum average requirement per IPC-6013C. Rigid boards class 2 have a 20 µm (787 µin) minimum average per IPC-6012[2].

Qualification tests included Accelerated Thermal Cycling testing of backdrilled coupons. No fails were seen through 600 cycles from -40°C to +90°C.

The LGA interconnect for this application uses gold-over-nickel to gold-over-nickel interconnect metallurgy. For high reliability, minimum gold thickness on the rigid-flex interconnect pads was specified as 0.00076 mm (0.000030"). Minimum nickel thickness was specified as 0.00127 mm (0.000050"). Porosity testing, gold and nickel harnesses testing, FTIR analysis, and ESCA analysis were performed on the interconnect surfaces during qualification.

Additional data collected during qualification included:

- First article inspection reports from the fabricator
- Itemized confirmation of compliance to all print notes
- Verification data for of all print dimensions/print notes

- Process capability data for key print requirements including impedance, plating thickness and critical mechanical dimensions
- Delivery of microsection pictures, measured data and physical mounts
- Failure analysis of all early build fails to determine root cause
- Hi-Pot test data

The LGA interconnect allowed for a dense interconnect solution with good signal integrity properties. Mechanical hardware including bolster plates, alignment pins and screws were designed to provide proper alignment and normal force for the LGA contacts. Figure 27 shows several of these features. Use of the LGA interconnect eliminated thermal exposures to the raw rigid-flex due to soldering. Figure 14 shows the via and pad structure for the LGA interconnect.

Conductive Anodic Filament Testing and Prepreg Rotation

Low- or no-flow prepregs are often required for rigid-flex applications to control epoxy flow at the rigid flex to flex interface. With the 1 mm LGA contact pitch and 0.39 mm vias there was significant concern in early development to drive initial CAF coupon build in parallel with initial part builds and early testing.

Test methods and coupons were similar to the conductive anodic filament (CAF) resistance test: X-Y axis as defined in IPC-TM-650 number 2.6.25[3]. The coupon cross-section replicated the rigid portion of the rigid-flex. Fails occurred within the first 50 hours of testing. A significant numbers of fails occurred within the first 150 hours of testing on coupons built with both standard and spread glass pre-pregs.

A team consisting of the prepreg supplier, the fabricator and the end user evaluated options which included additional glass types, better CAF performing materials, additional flow testing in conjunction with additional cutting back of prepregs and alternate lamination conditions. Based on available data from this and other programs and engineering judgement all options had significant risk due to short program schedules.

The team then considered prepreg rotation.

With the LGA connector on both ends of this rigid-flex and no additional vias on the part, the original design had all vias on a 1 mm x 1 mm grid. While this is unique compared to complex flex or boards with logic, it is fairly common for flex cables used in interconnect solutions. By rotating the prepreg 26.6 degrees as shown in Figure 15, the via to via distance was increased from .75 mm to 2.0 mm. Prepregs were rotated instead of rotating parts to facilitate manufacturing the progressive bookbinder sub-composite lengths in multiple parts across a panel.

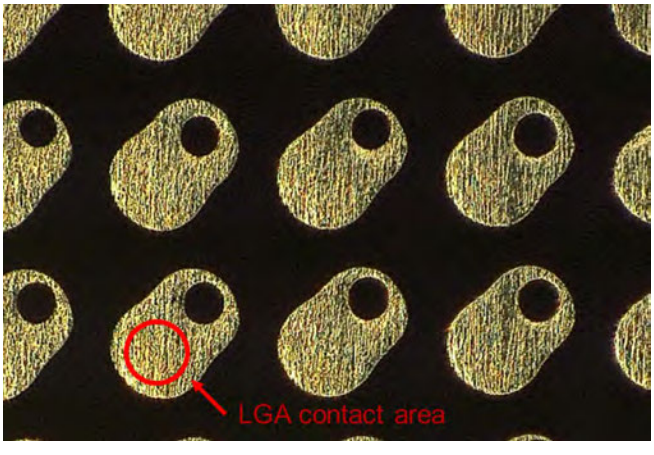

Figure 14: Via and LGA pad structure.

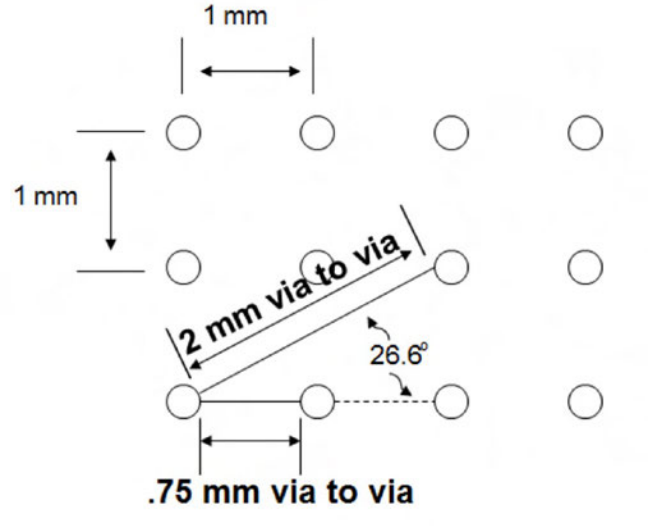

Figure 15: Via-to-via distance with rotated and non-rotated prepregs.

Figures 16 and 17 show CAF coupon failures. Failure analysis of the original coupons verified electromigrated copper as the defect mode. The orthogonal view in Figure 18 shows voiding and electromigrated copper between and along individual glass fibers.

Cross-section of parts and coupons with rotated prepreg confirmed the rotation was successful in the manufacturing environments as shown in Figure 19. Figure 20 shows the rotation effect on pre-preg panelization.

A second build of coupons was built with and without pre-preg rotation. As seen in Figure

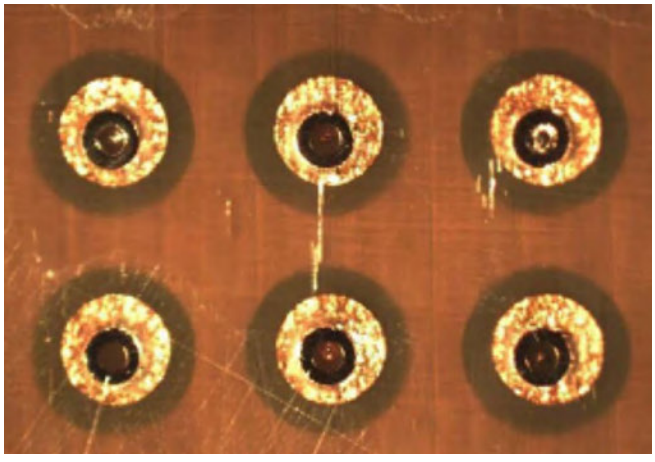

Figure 16: CAF coupon fail site.

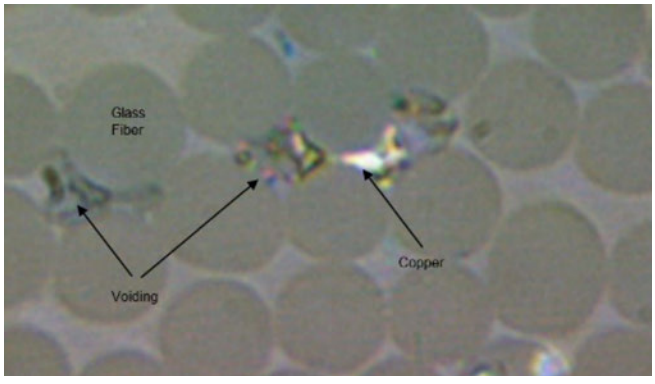

Figure 18: Orthogonal microsection of CAF coupon fail site.

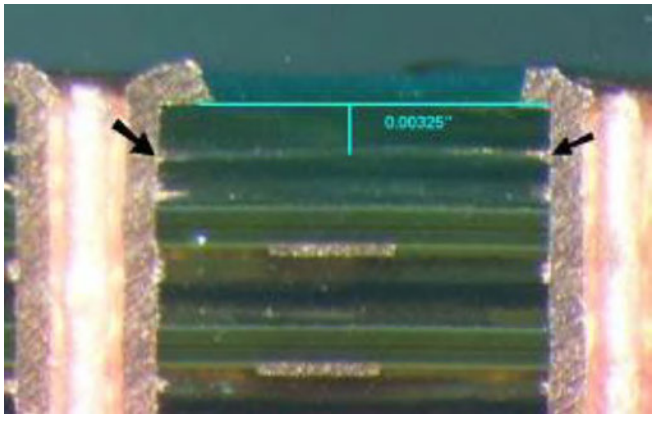

Figure 17: Microsection of CAF coupon fail site.

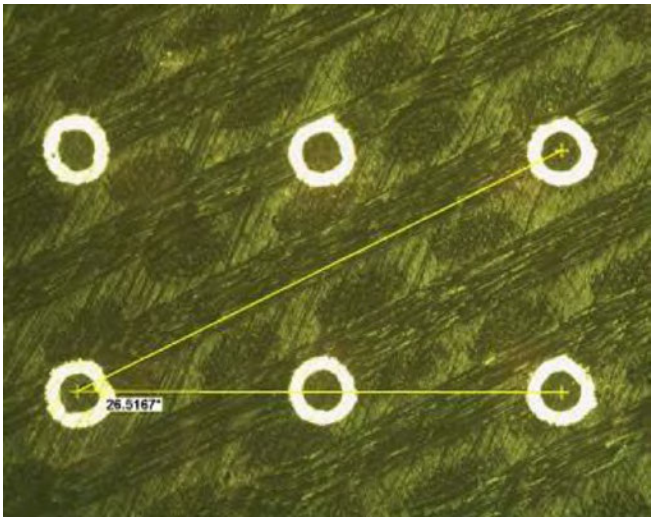

Figure 19: Confirmation of prepreg rotation.

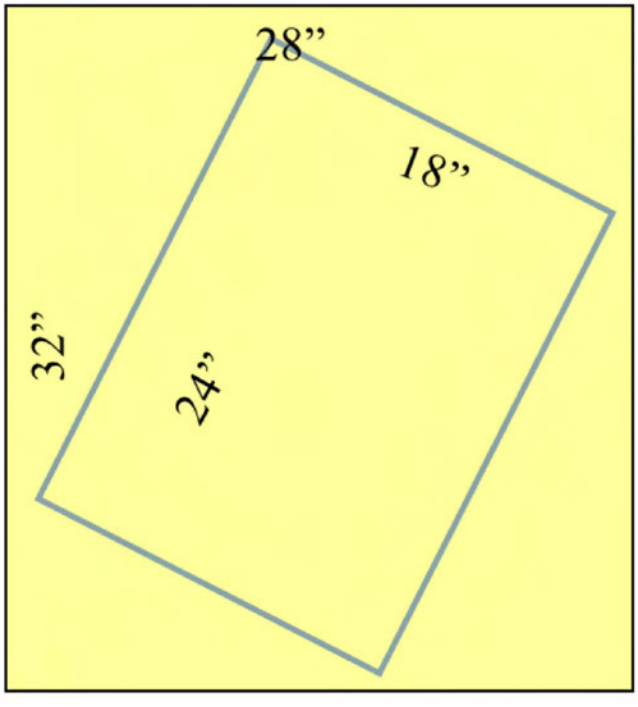

Figure 20: Prepreg panel utilization with rotation.

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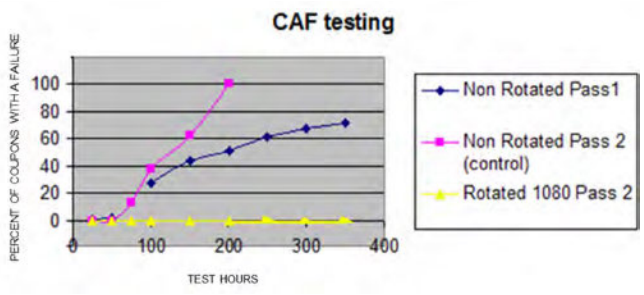

Figure 21: CAF testing results.

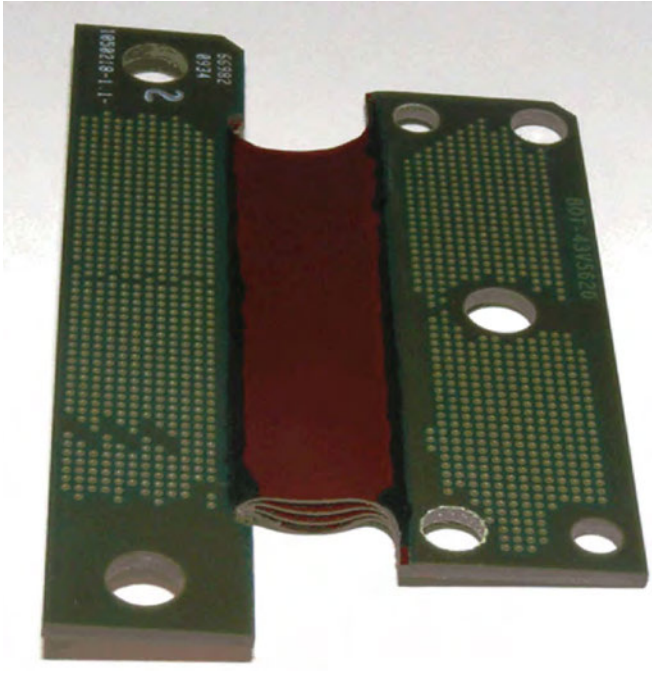

Figure 23: Rigid-flex with backside shown.

21, the non-rotated coupons from pass 1 and 2 performed poorly and the coupons with rotated prepreg had no fails through 350 hours. Additional CAF testing on samples with rotated prepreg and backdrilled vias at the initial and low cost geography manufacturing site had no fails through 500 hours.

Final Implementation

Figures 22 and 23 show the final bookbinder rigid-flex in flat form. The progressive lengths of the bookbinder can be seen. Figure 24 shows the product held in the 90-degree position—as it is positioned in the application. The alignment of the progressive lengths can be seen.

Figure 22: Rigid-flex with LGA contacts shown.

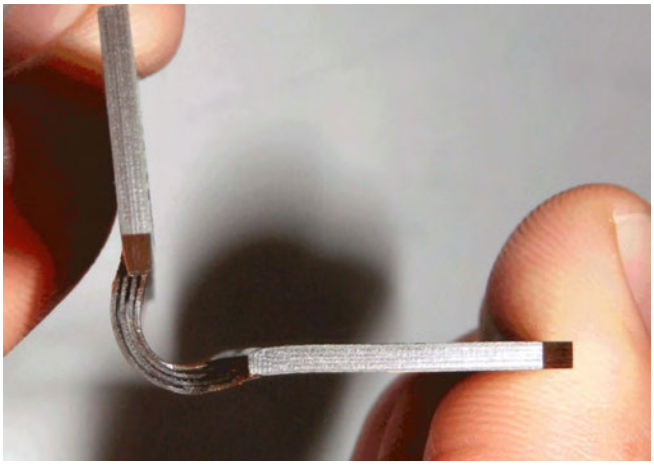

Figure 24: Bookbinder layers in installed position.

Figure 25 shows a 2-blade system with the covers and the scalability card removed. Two rigid-flex can be seen in the bottom right of the picture. Up to four blades could be connected.

Figure 26 shows a close-up view of the interconnect area. The two rigid-flex that can be seen have been electrically and mechanically attached to planar boards 1 and 2 with LGA contacts and mechanical hardware. The flex make 90-degree bends and can float on the two diagonal standoffs on each flex.

Figure 27 shows the LGA housing and LGA contacts on the scalability card. The two diagonal tapered pins provide alignment between scalability card/LGA housing/LGA contacts and each rigid-flex.

Figure 25: Two-blade system.

Figure 26: Two-blade system close-up.

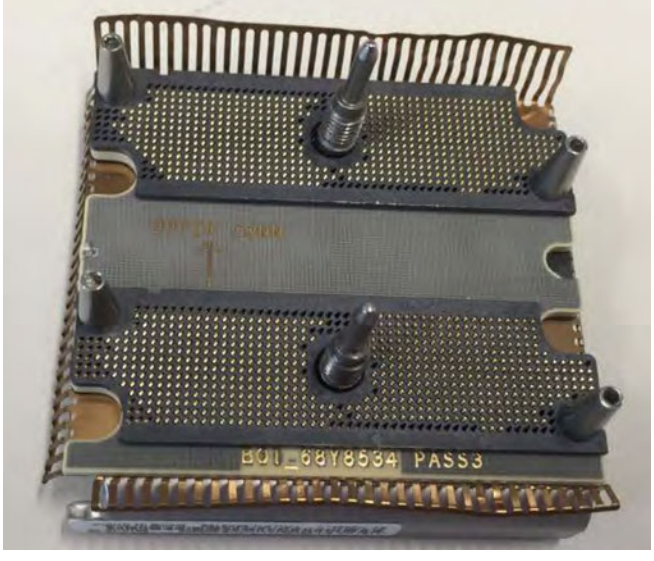

Figure 27: Two-blade scalability card.

Figure 28: Two-blade system with scalability card and hardware installed.

Figure 28 shows the scalability card installed with the mechanical hardware completing the interconnect between the two planar boards.

Conclusions

This rigid-flex design included several key elements, any of which on their own are a reason for special consideration. Together they were a significant challenge. By close collaboration between the flex supplier, material suppliers and end user we successfully implemented an elegant workable solution to a complex problem that addressed all requirements. **PCB**

References

1. Qualification and Performance Specification for Flexible Printed Boards, IPC-6013C, 2009.

2. Qualification and Performance Specification for Rigid Printed Boards, IPC-6012D, 2010.

3. IPC Test Methods Manual, IPC-TM-650, 2007.

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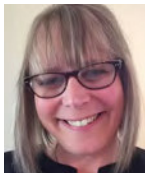

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MilAero007 Highlights

All About Flex: Flex Circuit Specifications for Commercial and Military Applications

Applications across the various markets for printed circuit boards can have significantly different specifications and performance requirements. IPC-6013 is an industry-driven specification that defines the performance requirements and acceptance features for flexible printed circuit boards.

EIPC Reliability Workshop, Tamworth, UK, September 22, 2016

EIPC's reliability workshop, presented in cooperation with Amphenol Invotec, attracted a capacity audience from eight countries—some delegates having travelled from as far away as Russia—to take the opportunity to learn first-hand how to meet OEM, ODM and EMS product quality and safety requirements, and to understand how interconnection stress testing techniques could be applied to determine the reliability of multilayer PCBs.

The Right Approach: FOD and the Aerospace Industry

Unless you are currently building aerospace product to AS9100, you are probably saying, "What the heck is FOD?" What started out as a requirement to prevent damage to aircraft parts such as engines has been flowed down to any component or assembly including PCBs.

John Cardone on Designing Flex for Spacecraft

If you watched footage of the Mars rover driving all over the red planet, you're familiar with some of John Cardone's handiwork. He's been designing rigid, flex, and rigid-flex circuitry for spacecraft since he joined JPL in the early '80s, and he's worked on some of the more ground-breaking flex circuits along the way.

American Standard Circuits Achieves AS9100 Rev C Certification

American Standard Circuit has achieved its AS9100 Rev C certification, the internationally recognized quality management system standard specific to the aerospace, aviation and defense industries. This standard is strongly supported and adhered to by major aerospace OEMs and is being required by vendors within the supply chain on an increasing basis.

Eltek Has Supplied $1.6 Million Orders to a Strategic Customer

Eltek Ltd. announced today that since January 2016 it has supplied approximately US$ 1.6 million of technologically advanced solutions to a strategic customer. The customer selected Eltek because of its capability to produce high-performance and reliable solutions.

Flex Talk: Troubleshooting Flex Circuit Applications for Mil/Aero Projects

I imagine that everyone has been in this position at one time or another: Despite everyone's best attempt at creating the perfect design, PCB fabrication and assembly, something goes wrong and the troubleshooting begins.

American Standard Circuits Achieves AS9100 Rev C Certification

American Standard Circuits has achieved its AS9100 Rev C Certification. AS9100 is the internationally recognized quality management system standard specific to the aerospace, aviation and defense industries.

Colonial Circuits: A Veteran-Owned Small Business

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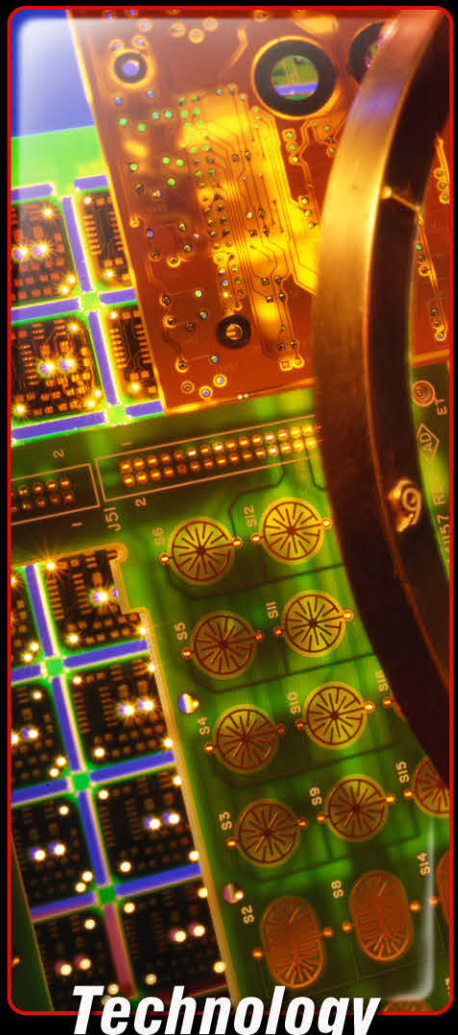
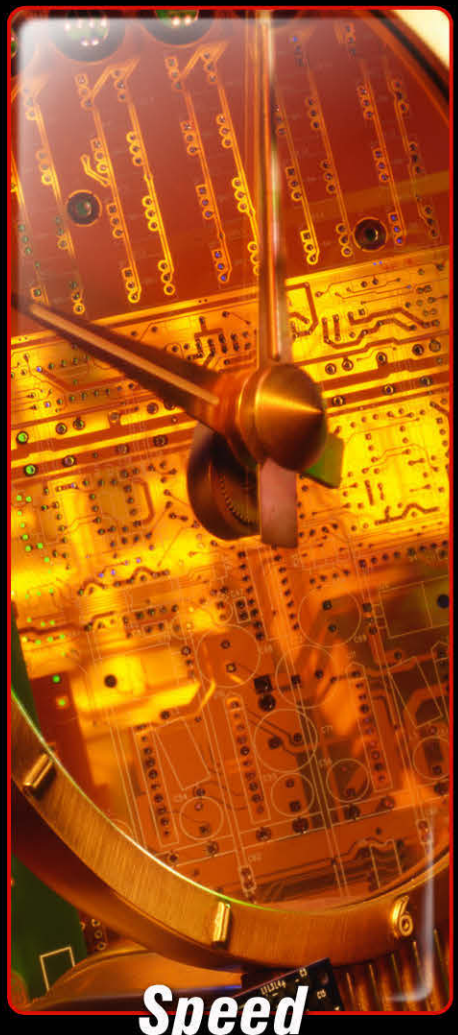
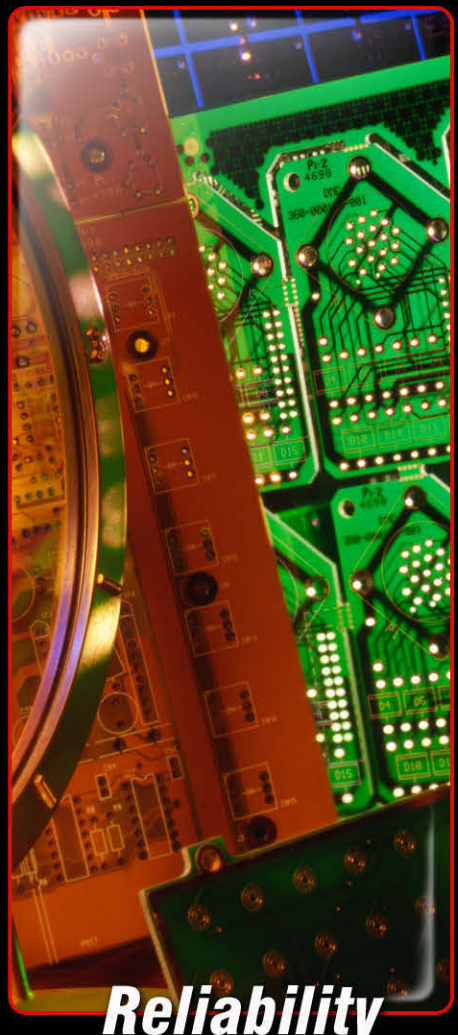


Technology



Speed



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Stepping Up to Laser Processing for Flex, Part 4: Installation, Training and Initial Operation

by Mike Jennings and Patrick Riechel
ESI

Supplementing your production capabilities with flexible circuit laser processing can pay big dividends. It not only enables you to broaden the set of services you can offer your customers, but it also extends your reach into additional markets you might not otherwise be well-equipped to serve. Employing laser technology is one of the best ways to stay current in PCB processing, since it enables you to process more accurate and smaller features than what is possible using mechanical processing.

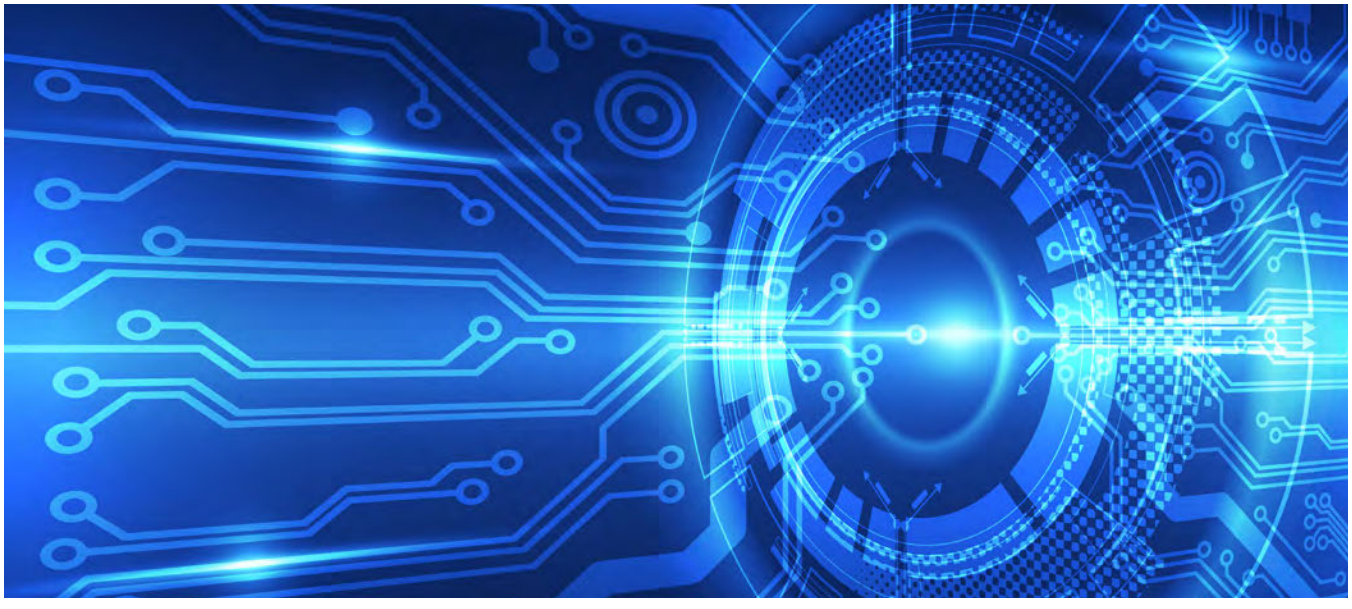
In a previous installment (part 3) of the "Stepping Up to Laser Processing for Flex" series, we discussed the most critical issues related to ensuring that your factory is prepared for implementation of your new laser processing system. With your factory now prepared, let's review the issues associated with getting your new system installed and running properly, so that you can start processing your first runs. This time we'll focus on installation best practices, system verification testing, training and the safe operation of your system.

Getting it There

As with any large piece of manufacturing equipment, just getting it onsite can be the first challenge. Your system supplier should be able to help coordinate transportation of the system to your facility. Working together with your supplier, your shipping/logistics partner and, if necessary, a local rigging company will ensure a smooth delivery and setup process.

The International Commercial Terms (Incoterms) associated with your system purchase will outline the tasks, costs and risks associated with the system's shipment. It's a document that provides details regarding the location to which the system is being delivered and includes the point at which final transportation and any associated insurance become your responsibility.

Due to liability concerns, you will typically need to take responsibility for movement of the system once it reaches your facility. Unless you can provide your own in-house rigging, it is a good practice to stage the equipment at your lo-



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cal rigging company's facility. This is especially beneficial if multiple systems are expected to arrive at different times. This will minimize the production interruptions typically associated with systems being repositioned on the production floor. Such off-site staging is also useful if you do not have an interim storage facility that meets the system storage environmental requirements. For instance, laser systems can become damaged as the result of being exposed to conditions such as high humidity and extreme temperatures or—even worse—being stored outdoors in pouring rain!

Once the system has arrived at your facility—and before moving the uncrated system into position on the production floor—it is wise, and often required as part of the supplier contract, to perform a thorough post-shipment inspection of both the crate and system before taking ownership, noting any damage and comparing the system's condition with the pre-shipment inspection. Since poor handling of the equipment can also result in less-visible system damage to the sensitive optics, the laser, and other precision components, many equipment manufacturers will apply shock and tilt sensors to the shipping crates or the equipment itself in order to document the proper handling of the equipment in transit. If anything looks out of order—whether it be a tripped sensor or obvious physical damage—make sure to get photographic evidence and alert your supplier as soon as possible in order to sort out a recovery plan.

Figure 1: Poor handling during shipment can result in severe equipment damage.

Final system uncrating and unpacking should be done in the presence of your supplier's service team. In addition to inspecting the system for damage after uncrating, you should verify the presence and condition of the sealed environmental barrier bag that was used to prevent the contamination of the system's optics during shipment.

After system uncrating, inspection, and subsequent move to the system's ultimate operating location, system installation/commissioning will typically be performed by your supplier's field service team. This will consist of placing and leveling the system and connecting it to the services that have been prepared for the system's arrival. Electrical power, compressed air and vacuum services should have already been made accessible at the system's ultimate location and those services should be consistent with the system's site requirements.

System and Site Verification Testing

After the system has been connected to the required facility services, your supplier will typically perform a thorough set of compliance, safety and diagnostic tests designed to verify that both the installation site and the system itself meet the agreed-upon requirements.

Site requirement compliance:

These tests will ensure that the installation site complies with the system's requirements as discussed in the previous installment of this series. These verify that environmental factors meet specifications such as temperature and humidity. They will also ensure the availability and quality of services such as vacuum, compressed air, etc.

Safety:

At a minimum, safety tests will ensure that the system's laser beam is safely confined to the pro-

cessing area inside the system, and is not escaping through any gaps in the system's cabinet when the shrouds and doors are closed. They also ensure that safety interlocks are functional and trip at the appropriate time, and that all emergency machine off (EMO) buttons are operational.

Major subsystems:

Verifies the proper functioning of subsystems such as computer, power supplies, sensors, debris removal, etc.

Laser and laser chiller:

Verification of laser and chiller functionality, including laser power levels, chiller temperature stability and chiller coolant levels. This ensures that the laser will continue operating according to its specifications and avoids premature service interventions.

Optics quality and alignment:

Laser spot quality and laser power transmission through the optics path can be affected by optics that may have become contaminated, damaged or misaligned during shipment. Given the importance of laser spot quality and spot size in high-quality via formation, verification of items such as optics alignment, beam diameters and laser spot quality is critical.

Motion/accuracy/kinematics:

Verification of stages, galvanometers, and camera accuracy calibrations as well as motion and control loop functionality ensures that the process features will be placed accurately and formed correctly with precise beam positioning.

Laser power stability and control:

Correctly calibrated and functioning power control ensures the best possible yields, especially for blind vias and other depth-limited processes on sensitive materials. At an absolute minimum, calibration of the system's power measurement sensors against a certified, calibrated external power meter is required. Other tests related to system laser power control and laser power stability further verify how much laser power variability your process engineers will have to build into their process development calculations.

Assuming these tests have been completed and no issues are documented, the system has met the supplier's own system specification criteria. If demonstration applications had been developed by your supplier prior to the system sale, this is often a good time to verify that the applications show similar quality on the system that you are purchasing as compared to those previously seen in the demonstration results. After the completion of these tests, the system will typically be released for your use.

Figure 2: A typical EMO button.

Training and Safe Tool Operation

Now that the system is ready for use, how do you use it? At a minimum, your operators will require training related to basic tool operation. On-site operator training is typically offered by your supplier's service or applications team, complementing a copy of the operator guide. These should cover safe operation of the tool, including laser, electrical, mechanical, chemical safety, functionality and the proper use of safety interlocks and EMOs. This should

Figure 3: Examples of common laser system safety labels.

Figure 4: Example of an LED light tower with operation status (red, yellow, green) and interlock defeat status (white) LEDs.

also involve an explanation of how the system shows that the interlocks are defeated—indicating dangerous Class 4 system status, rather than safe Class 1 operation. Furthermore, system startup and shutdown should be covered, including how to put the laser into standby mode and understanding the time required for the laser to warm up and stabilize after returning from standby. A review of the operator interface—how to log in, how to initialize the system, and process panels, how to start and stop jobs, and other production features—will similarly be covered in a typical training.

Beyond operator training, assuming you will not exclusively use the system for a single application for the life of the tool and have already been given the production process for that application, it is important to train your process engineer or process engineering team on the development of new processes. This is equally important if your team is new to laser processing or if you are switching from one laser supplier or system model to another. Each system will have different operating characteristics and capabilities that impact the process, as well as different software functionality for process development.

There will always be certain guidelines that can be followed for flex laser processing, some of which will be discussed in more detail in the next installment of this series. A typical applications training outline might include the following concepts:

Tool overview:

How does the laser energy get from the laser output to the work piece? How is power controlled? How is the material kept in flat and in place during processing? How does the debris removal mechanism work, how is it used, and what is its importance in consistent processes and optics lifetime?

Creating a laser drill file from a CAD file:

How does one define alignment points, offset, rotation, and scaling methods? How does one set laser focus? How are process parameters and tooling motions (e.g., circles, spirals, punches, routs) added and modified?

Developing processes for blind and through vias, routing, and/or patterning:

What are the available knobs to affect the process, such as tooling motions, laser power, laser repetition rate, process velocity, and laser focus? How does one best combine various tooling motions for any given process? How do blind and through processes differ and what are the associated tradeoffs between throughput and quality/yield? What is fluence and how does it affect material removal? How does one ensure a high yield process with a robust process window?

For both operator and process engineer training, there are many important details to cover. Make sure that the personnel to be trained can fully focus on the training. At a minimum, they should be relieved of other engineering or production responsibilities during the training times and, ideally, distractions such as the use of mobile phones should not be allowed the training room.

Initial Operation

With operators and process engineers fully trained, your team is now equipped to start developing and running production processes. However, it is common for questions to arise as you start operating the tool. Don't hesitate to stay in touch with your supplier. Especially for those new to laser processing, questions are normal! **PCB**

Mike Jennings is director of product marketing with ESI's Industrial Products Division.

Patrick Riechel is product manager for ESI's flexible circuit micromachining tools. To read past columns or to contact them, click here.

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HKPCA's Daniel Chan on China's PCB Manufacturing and Technology Landscape

by Edy Yu
I-CONNECT007

Editor Edy Yu recently spoke with Daniel Chan, executive director of the Hong Kong Printed Circuit Association (HKPCA). Chan possesses more than 25 years of experience in global business management with strong leadership influencing suppliers and internal clients in business strategy and transformation. Prior to HKPCA, Chan had worked in IBM as the Global PCB Commodity Chairman, in the area of integrated supply chain management, quality assurance management, manufacturing and process engineering development and integrated product development. In this interview, Chan discusses the highlights of this year's International Printed Circuit and APEX South China Fair 2016, and he provides his insights on the current PCB technology and manufacturing landscape in China.

Edy Yu: What should we expect this year at the HKPCA & IPC Show?

Daniel Chan: The HKPCA & IPC Show is one of the most influential trade shows in the PCB and electronics assembly markets. It provides the industry with a premium platform for technology exchange as well as leading industry development.

This year's show theme is "Global Wisdom Shaping the Future," and is expected to attract close to 550 exhibitors from 17 countries and regions showcasing their latest innovations in more than 2,500 booths at Halls 1, 2 and 4 of the Shenzhen Convention and Exhibition Center. Our exhibition area now covers more than 50,000 square meters. Of the 550 exhibitors, 100 of them are new to the show.

We are also launching a new Japan/Korea Pavilion this year in Halls 1 and 2. This will group together the leading industry players from Japan and South Korea, bringing innovative equipment and technologies from these two countries to the show. As of September, it had attracted close to 30 exhibitors from Japan and South Korea, including JCU, Tsunoda, Taiyo Ink, Uyemura, Leadtech, Ishihara, NR G&C, MEC, Taesung, and GCE.

This year, the Smart Automation Pavilion will feature enriched content to help the industry progress towards higher productivity and more intelligent production. We are also bringing the Hand-Soldering Competition World Championship to the show, which will be its first time in China. Champions from China, Germany, the United States, South Korea and Japan will compete for the world title. Visitors will be able to observe the highest levels of hand-soldering craftsmanship at the event.

Other concurrent activities include the International Technical Conference, which will feature a variety of topics designed to bring you up to date on the latest technical and market trends in the industry. Meanwhile, the

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Welcome Dinner and golf tournament will provide abundant opportunities to network with peers in a relaxed environment.

***Yu:** What can attendees expect at this show regarding current hot-button issues, such as the environment, smart manufacturing, and automotive electronics?*

Chan: As a leading indicator of industry development, we follow market trends and stay on top of technology breakthroughs and innovations. Green development is still a sustainable topic in the industry and green production has increasingly become a typical configuration for PCB manufacturing. This year, the show's Green Pavilion will continue to provide the industry with a whole host of innovative green energy technology, new materials, and energy-saving production methods, to help enterprises carry out greener production.

To promote Industry 4.0 and Made in China 2025, and to strengthen our understanding of smart production, the Smart Automation Pavilion will be further enhanced this year to offer the latest automation equipment, technologies, and effective solutions that will help the industry move toward intelligent production and reduce labor cost.

The International Technical Conference will be held concurrently at the show, with industry experts sharing their insights on latest issues or solutions. Details will be announced soon.

***Yu:** Does PCB production technology development face any serious challenges today? What technology breakthroughs are you looking forward to seeing?*

Chan: As the value-add of electronic products has increased, circuit board production technology is facing different challenges. From the HDI board point of view, as customer requirements and technology keep improving, manufacturers can now make 3+N+3 HDI boards, and 4+N+4 HDI boards are already on the way. After pressing the PCB more than three times, mostly because of alignment problems, the yield decreases. After multiple pressing, the movement between layers increases, posing a great challenge to the material. On top of this, circuit boards today

Daniel Chan

are more sophisticated and signal transmissions are faster, requiring more accurate routing of boards. High-end boards now use semi-additive methods for production, which poses another challenge for HDI board production. As the circuit boards get smaller and more complicated, width and spacing will become even narrower, from the current 50 microns to 25 microns, and production yield of mobile phone PCBs will face a great challenge.

From the multilayer board point of view, high-frequency boards are facing signal integrity challenges. With the advent of 5G, routers and base stations' transmission speeds are expected to increase; in this case, material requirements and Df/Dk requirements are facing huge challenges. Circuit boards for supercomputers have as many as 40–50 layers. By using sequential lamination method, the alignment and drilling of the PCB and the connection of the inner hole of the HDI board are the technology

bottlenecks in production. Material stability will also face challenges. In addition, as multilayer boards are getting thicker and thicker, and holes getting smaller and smaller, electroplating, filling, and high aspect ratio processes are also facing challenges.

In short, there are all kinds of different aspects of circuit board production technology bottlenecks, and it is difficult to determine which area will make a breakthrough first, but I think material stability, mechanical properties and plating technology need to be further improved.

***Yu:** What can you say about the current domestic PCB landscape, and your business development outlook in 2017?*

Chan: The domestic PCB industry is full of opportunities and challenges. China's electronics design community continues to grow, engaging in product design and the development of standards, such as mobile phones (Huawei), wireless base stations (Huawei, ZTE, Datang), and automotive parts. The development of the design segment is an opportunity. The challenges are coming from two drivers: The first is oversupply, which is causing great competitive pressure. In this case, prices go down and profits drop for domestic manufacturers. It could be a challenge, but it could also be an opportunity, because the cost of domestic manufacturing is relatively low.

Technical requirements are also challenging, because PCBs, especially electronic assembly and applications, get more and more complex. The required value-add and capabilities of PCBs are increasing. For example, mobile phone design is now more complex than ever; 5G technology is moving into the high-frequency domain; and routers and servers are getting even faster. Therefore, as domestic PCB production technology is relatively behind global technology levels, domestic PCB manufacturers need to catch up, narrow the gap, and work with other advanced countries with technology development, to have that innovative ability and meet the global market needs in the future. I am optimistic about the development of the domestic PCB industry, where there is still a huge demand for PCBs. When local manufacturers improve their technology, they will be able to expand their PCB business to the world, and solve technical problems that the domestic electronics industry is facing.

***Yu:** Many PCB manufacturers are now building their own PCB design team, while some are introducing SMT lines into the facility to expand their business. What do you think of this?*

Chan: This is the vertical integration of the whole industry, which goes from PCB production to SMT assembly and PCB design. Many of them are successful, such as Flextronics, Foxconn, Celestica and some other big enterprises. Companies that want to implement vertical integration need to gather their own technical capacity, as the technology in PCB industry is basically different from electronic assembly and electronic product design industries.

In general, PCB production is a mix of chemical, electronic, and physical engineering technology industries. Electronic product design basically belongs to the electronic engineering industry, which includes mechanical engineering, industrial engineering, automation engineering and a small amount of chemical engineering.

Overall, vertical integration is the right direction, which could control the whole chain better, but it is important that sufficient funds, personnel, and technical ability are provided to achieve the goal. Vertical integration also has its weak spot; it could lead to customer distrust, as customers would worry about their intellectual property leaking to the manufacturer's own design center or electronic assembly center. Therefore, PCB manufacturers need to establish independent operations that are separate from their associated PCB design company and electronic assembly company; otherwise, it will have an impact on their PCB sales. So manufacturers should separate the corporate image from the actual operation, which will have a positive effect on vertical integration development.

***Yu:** Thank you for your time.*

Chan: Thank you. **PCB**

HKPCA & IPC Bring Hand-Soldering Competition World Championships to China

by Edy Yu
I-CONNECT007

In an interview with Editor Edy Yu, Helen Guo, member services director at IPC Greater China, discusses IPC's activities and initiatives in China, such as standards development and promotion. She also discusses the upcoming International Printed Circuit and APEX South China Fair 2016, co-organized by HKPCA and IPC this year, which will feature the hand-soldering competition world championship for the first time in China.

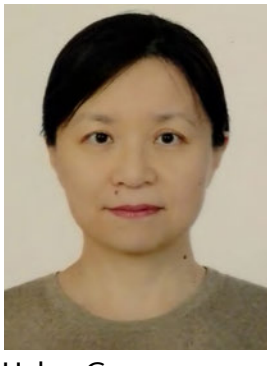
Guo joined IPC last January 1, 2016, to become the Director of IPC Greater China Member Services. She has nearly 30 years of experience in marketing and supply chain management. Prior to IPC, she has worked for AutoClear LLC, Lexmark International Ltd, PerkinElmer China Ltd, EG & G Beijing Representative Office and many other large international multinational companies.

***Edy Yu:** You have been hosting this show in China for many years. What's the purpose, and what has been achieved so far?*

Helen Guo: IPC's mission is to help our members achieve financial success and strengthen their competitive advantages. One of the ways we do this is by co-organizing this show to build a platform for industries to communicate, learn from each other, promote innovation, and facilitate cooperation.

After 15 years, the HKPCA & IPC Show has transcended its regional status and now attracts industry leaders and participants worldwide, becoming one of the most influential trade shows of its kind in the PCB and electronics assembly market. The event offers a premium platform for sourcing and technology exchange.

***Yu:** Smart manufacturing is on everyone's mind. How will they cover this topic?*



Helen Guo

Guo: Industry 4.0 and Made in China 2025 are among the hottest issues in the industry. This year, the Smart Automation Pavilion will return with enriched content, bringing more innovative equipment, technologies and effective solutions that will help the industry move

to more intelligent production and reduce labor cost.

Profit maximization and freeing labor forces for more creative work are driving industry changes right now. Intelligent manufacturing is going well in many industries, including the PCB and EMS sectors.

***Yu:** Please tell us about IPC's specifications promotion and development in China.*

Guo: IPC specifications are evolving, with dozens of appropriate specifications being published each year. In technical, industrial and social development aspects, IPC is working very hard to develop new specifications, including revision updates. We have many of these specifications, such as the 1401 CSR (Corporate Social Responsibility) specification, and the 2581 series specifications (data transmission between automatic manufacturing and cooperation upstream and downstream). In addition, we are developing a press mounting specification in accordance with automotive requirements.

***Yu:** What's new at this year's hand-soldering competition?*

Guo: The hand-soldering competition is one of our hit programs at the show, and it enables visitors to check out the outstanding soldering craftsmanship going on in the industry. This year, we are bringing the Hand Soldering Competition World Championship from the United States. It is the first time for this world championship to be staged in China, with champions from China, Germany, the United States, South Korea and Japan under one roof. We believe the three-day competition will see the highest levels of hand soldering craftsmanship anywhere.

***Yu:** Some PCB manufacturers are starting to develop their own PCB design capacity, while some are expanding their capabilities to SMT. What's your opinion on this?*

Guo: It is normal for a company to expand or narrow their business scales as their advantages and resources change. We are happy to see that PCB makers are putting an effort into designing. Having the ability to design promotes a dynamic industry. IPC has abundant technology and intelligent resources to help companies enter an unfamiliar field and expand quickly.

***Yu:** Thank you for speaking with me today.*

Guo: Thank you. **PCB**

225 Tech Talks–1995 to 2016

by Karl H. Dietz

In August of 1995, the first *Tech Talk* column issued in *CircuiTree Magazine* with the title "Process Latitude." The tag line of "fine lines in high yield" served us well, as it was reasonably broad to encompass many processing and material issues. However, other issues equally important to PCB and substrate manufacture and performance deserved coverage and were addressed over the years.

In April 2011, the last *Tech Talk* article (No. 183) appeared in *CircuiTree Magazine's* last edition. By then, *CircuiTree* founders Barry Matties and Ray Rasmussen had launched PCB007, and they were about to add several online publications, including *The PCB Magazine*. It was at the spring 2011 IPC APEX EXPO where I ran into Ray, who talked me into continuing the *Tech Talk* column in *The PCB Magazine,* as he persuaded several of the other usual suspects to contribute also. Without missing a beat, *Tech Talk* No. 184 then appeared in the May 2011 edition of *The PCB Magazine* and has been a fixture ever since.

Checking back on *Tech Talk* Nos. 100 and 200, which reflected on past and anticipated future changes in electronic packaging, I noted the production shift to Asia, followed by the relocation of the supplier base, and, more recently, the design of electronic devices. New mobile applications forced technology changes and shifted the economic viability of old and new companies. In a basically conservative in-

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dustry that doesn't readily embrace technological change, there were nevertheless innovations in materials and processes: Digital imaging became a reality after overcoming many hurdles. New base materials were introduced to accommodate the needs of lead-free and high-speed signal processing. Coreless structures, parallel processing, and the use of conductive pastes gained acceptance. Technologies crossed the borders between wafer fabrication, wafer-level processing, substrate and PCB fabrication. These trends are likely to continue, but I dare not predict new game-changers.

I am looking forward to following these events in the coming years. My plan is not to write *Tech Talk* columns regularly anymore, as I have done for the past 21 years, but to write occasionally as a guest columnist about topics that capture my attention and that I deem of interest to the readers of *The PCB Magazine*. Many thanks to all of you who have let me know over the years that you enjoyed my column! Feel free to contact me if you have questions that I may be able to help you with! **PCB**

Karl Dietz is President of Karl Dietz Consulting LLC. He is offering consulting services and tutorials in the field of circuit board and substrate fabrication technology. Karl can be reached by e-mail by clicking here, or by phone at (001) 919 870 6230. To view past columns, click here.

Counterintuitive 'Metamaterial' May Enable Heat-resistant Circuit Boards

Almost all solid materials, from rubber and glass to granite and steel, inevitably expand when heated. Only in very rare instances do certain materials buck this thermodynamic trend and shrink with heat. For instance, cold water will contract when heated between 0 and 4 degrees Celsius, before expanding.

Engineers from MIT, the University of Southern California, and elsewhere are now adding to this curious class of heat-shrinking materials. The team, led by Nicholas X. Fang, an associate professor of mechanical engineering at MIT, has manufactured tiny, star-shaped structures out of interconnected beams, or trusses. The structures, each about the size of a sugar cube, quickly shrink when heated to about 540°F (282 C).

Each structure's trusses are made from typical materials that expand with heat. Fang and his colleagues realized that these trusses, when arranged in certain architectures, can pull the structure inward, causing it to shrink like a Hoberman sphere—a collapsible toy ball made from interconnecting lattices and joints.

The researchers consider the structures to be "metamaterials"—composite materials whose configurations exhibit strange, often counterintuitive properties that are not normally found in nature.

In some cases, these structures' resistance to expanding when heated—rather than their shrinking response per se—may be especially useful. Such materials could find applications in computer chips, for example, which can warp and deform when heated for long periods of time.

The researchers have published their results in the journal Physical Review Letters. Fang's co-authors include former MIT postdoc Qi Ge, along with lead author Qiming Wang of the University of Southern California, Jonathan Hopkins of the University of California at Los Angeles, and Julie Jackson and Christopher Spadaccini of Lawrence Livermore National Laboratory (LLNL).

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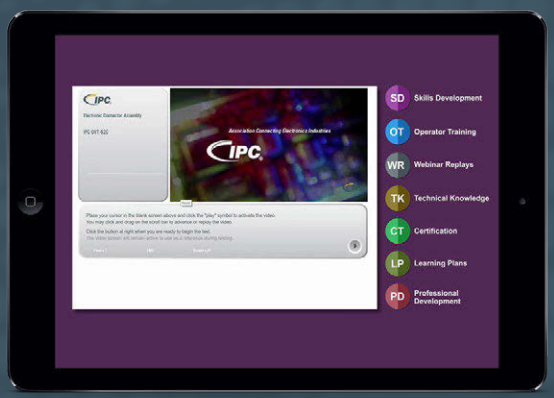

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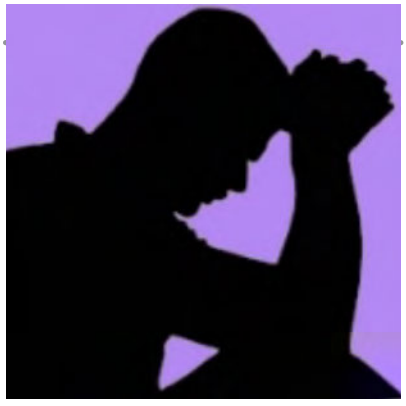


My Graphic Grief: Trade Shows and Events

by Barry Lee Cohen
LAUNCH COMMUNICATIONS

I've had the absolute privilege to organize and direct exhibition activities from Shanghai to Shenzhen, from Munich to Mumbai, from San Diego to San Jose and beyond. No matter the location, I just can't seem to get over my "graphic grief."

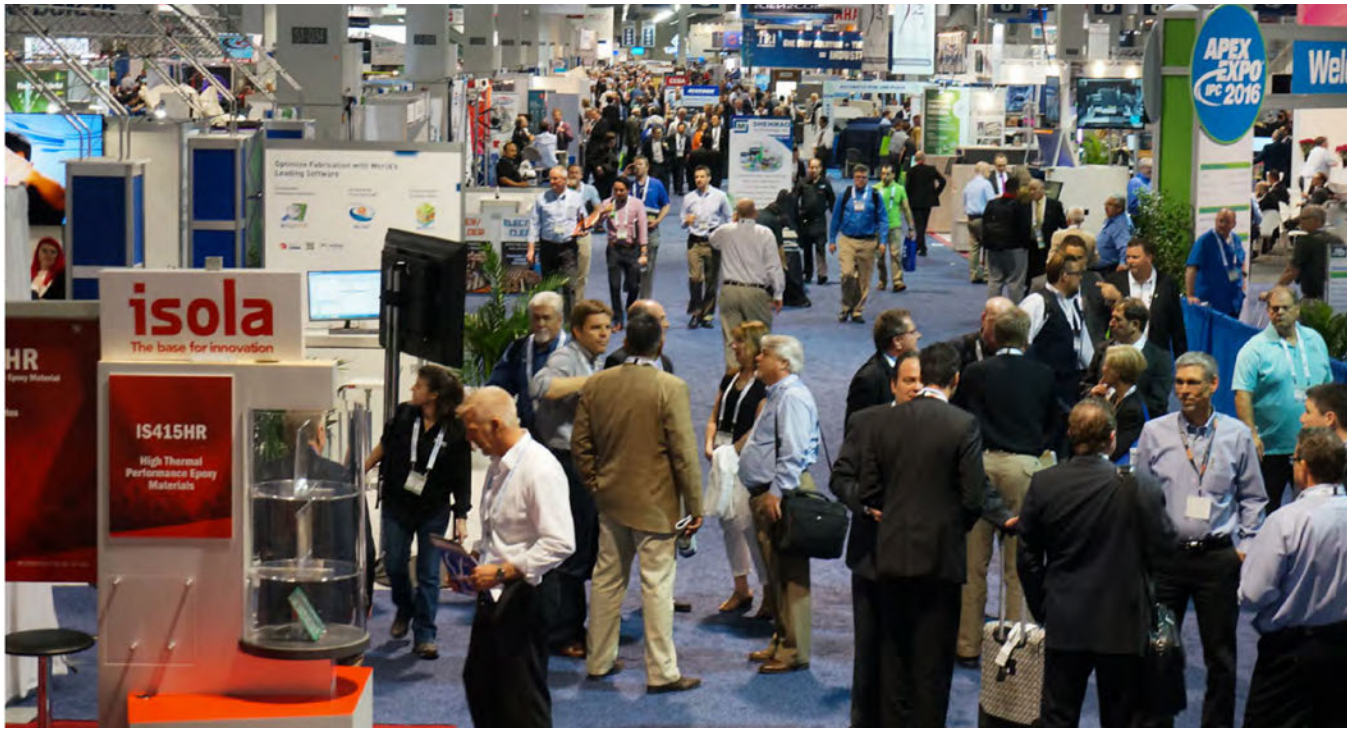
Graphic grief can be debilitating for anyone responsible for managing their company's trade show involvement. At times, many of us have been known to succumb to this scourge by allowing ourselves to produce graphics with headlines that involve a big yawn, teeny tiny text that rambles, and imagery that lacks the creative and instead defaults to generic pictures and cliché slogans that add no compelling or differentiated value. Given the large investment your company makes in booth space and structure, as well as the growing cost of show services and staffing the booth, not taking the time to treat graphic grief would be regrettable.

Don't despair. There is a cure. This month's column is being prescribed to help you grapple with the grief of your graphics, while injecting a few laughs for good measure. Blast-off…

A Trade Show is a Controlled Circus

Decades ago I was walking down the aisle of a major trade exhibition and a realization hit me like a barrage of Jolly Ranchers flying out of exhibitors' candy dishes: A trade show is a controlled circus. With a huge, Jack Nicholson-like crazy man grin on my face, I thought to myself:

Dang it! Each booth is like a cage. Each cage has nicely coiffed guys and gals pawing at the end of their booth carpets, dangling their bright-



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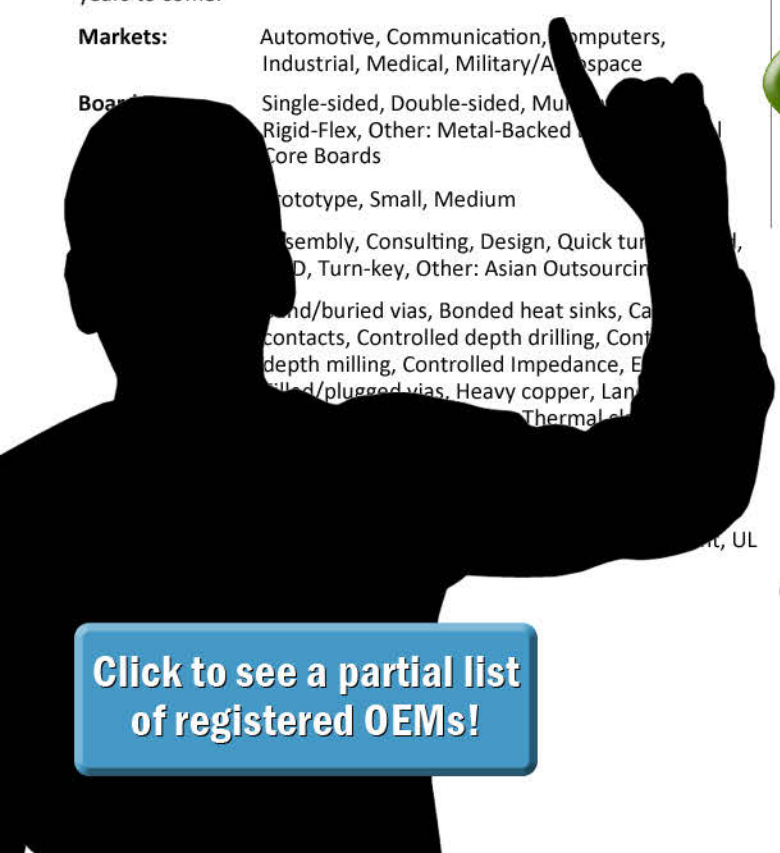

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est smiles and impeccable manners. Each of these well-meaning lions wants to lure me into their lair and devour my intellectual carcass by painfully regurgitating features of their products. These lions eagerly anticipate that I will be swallowed up by their sheer genius of how they decode their graphic mess of messages that are most often being secured in the back of the booth, safe from competitors' shifty eyes. Others will only communicate the secret value of their special sauce in their secluded dens of knowledge (aka, booth conference room).

Fast forward, three decades later.

I attended another trade show for a completely different industry and the same circus runs amok. My advice is the same now as it would have been to the pride if I could only have wiped that dastardly smirk off my face. "Make your message—and your investment—count. Unleash your lions! Collaborate with your guests and stop the graphic grief! Run free, my graphic child. You will not fall prey by clearly and concisely showcasing your knowledge in a compelling, relevant, concise and thought-provoking manner!"

A Graphic is Not a Print Advertisement

• Less is more. Keep your text concise and your overall graphic appeal impactful. A graphic is not a technical paper, but should be employed to elicit questions, discussions, and follow-up that could be technical, market- or sales-related.

• Like a fine wine, let your graphics breathe! There is no sin in purposely allowing some white space to visually showcase relevant imagery and concise text.

• Fonts are your friends when applied wisely. This includes staying true to established and essential corporate identity guidelines. These guidelines should specify the type and size ranges of the font to be used, as well as include an established color palette. The overall tone of the company's communications (both imagery and text) should also be considered as part of the corporate identity that should consistently translate to all media.

• Save the in-depth technical content for your support literature or website. Furthermore, should detailed content be absolutely necessary at the booth, such information should be delineated within the support literature, app or website to help facilitate conversations with highly qualified leads.

Stop the Chest Beating

It amazes me the number of booths that have their key messages hidden amongst the chest beating themes of "leading supplier," "number one widget," "global coverage," and "innovative solutions," to name just a few of the vanilla clichés that get tossed about the main headline of graphics. Now don't get me wrong, a little commercial kudos to your company is all fine and good…and most often expected by the higher-ups. However, did you ever stop to consider:

• Have my potential booth guests read the same thing time after time while grazing at prior cages? Well of course they have!

• Does my chest-beating truly differentiate my product, service or company? Most times the answer is a big NO.

• In the rare cases your self-congratulatory pat is a relevant differentiator, is it the most important statement to be splashed as the main headline? Of course not!

• How does this chest beating add value to your customer's need? It doesn't and in some cases the perceived vanity your graphic inadvertently communicates is scoffed at or worse, opens a Pandora's box discussion as to when your company was considered "number one," in a manner you never intended.

Don't let Customers Coast by Your Booth

• Consider each of your graphics to be a billboard on a congested highway filled with other billboards, traffic signs and various construction detours along the way. At best, you have three seconds to gain the visitors' attention to read the headline. If they find your message to be intriguing, they may read the additional text and related images.

• Don't go cheap. Have professionals design and produce your high quality graphics. It's your company's image hanging on that booth wall or LED screen. How you present your message is a direct reflection of your market leadership, knowledge and commitment to the industries served.

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• Ensure your graphic is two feet off the floor and not competing with potted plants and your nicely polished shoes. The vast majority of your graphic should be eye level, whereas visitors will read your graphics as they do a billboard or magazine which is left to right (excluding parts of Asia) and from top to bottom.

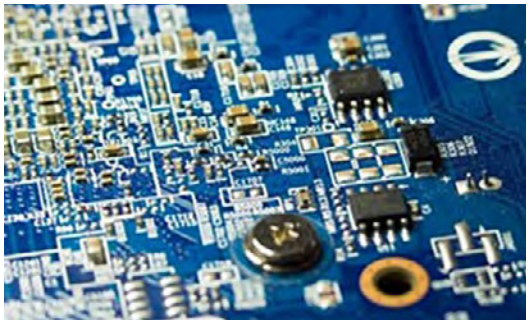
Interactive Modules and Videos

Both can be extremely beneficial, although many times the placement of these tools are not aligned with the key reason you decided to exhibit in the first place. Spending big bucks on a show to introduce your latest new product or service has the potential of being obscured because some blue suit wanted to show the fancy new corporate video or fell in love with a new app that is at best secondary to the actual product or service being introduced. Of course, you want to include such interactive tools, just be careful of making them the focal point of your booth.

Graphic grief is a common, yet curable disease by prescribing to the above recommendations. As always, watch your dosage and repeat for each show. **PCB**

Barry Lee Cohen is president and managing director of Launch Communications. To read past columns or to contact Cohen, click here.

Engineers Design Ultralow Power Transistors that May Function for Years



A new design for transistors which operate on 'scavenged' energy from their environment could form the basis for devices which function for months or years without a battery, and could be used for wearable or implantable electronics.

A newly-developed form of transistor opens a range of new electronic applications including wearable or implantable devices by drastically reducing the amount of power used. Devices based on this type of ultralow power transistor, developed by engineers at the University of Cambridge, could function for months or even years without a battery by 'scavenging' energy from their environment.

Using a similar principle to a computer in sleep mode, the new transistor harnesses a tiny 'leakage' of electrical current, known as a near-off-state current, for its operations. This leak, like water dripping from a faulty tap, is a characteristic of all transistors, but this is the first time that it has been effectively captured and used functionally. The results, reported in the journal Science, open new avenues for system design for the Internet of Things.

The transistors can be produced at low temperatures and printed on almost any material, from glass to polyester. They are based on a unique geometry which uses a 'non-desirable' characteristic, namely the point of contact between the metal and semiconducting components of a transistor, a so-called 'Schottky barrier.'

The new design gets around one of the main issues preventing the development of ultralow power transistors, namely the ability to produce them at very small sizes. As transistors get smaller, their two electrodes start to influence the behaviour of one another, and the voltages spread, meaning that below a certain size, transistors fail to function as desired. By changing the design of the transistors, the Cambridge researchers used the Schottky barriers to keep the electrodes independent from one another.

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TOP TEN

Recent Highlights from PCB007

1 Weiner's World

This month, I was a guest at the High Density Packaging Users Group (HDPUG) meeting in Nashville, Tennessee. The consortium, composed of more than 50 companies (small and large) in the electronics packaging supply chain, conducts projects to solve real world problems or develop data for product parameters, package/component life, and production processing.

2 ECWC14 Seeking Abstracts for 14th Electronic Circuits World Convention

The 14th Electronic Circuits World Convention (ECWC14) will be held in KINTEX, Goyang City, South Korea from April 25–27, 2017 along with the KPCA Show hosted by Korea Printed Circuits Association (KPCA) and the World Electronic Circuits Council (WECC).

3 Volunteers Honored for Contributions to IPC and Electronics Industry

IPC—Association Connecting Electronics Industries presented Committee Leadership, Special Recognition and Distinguished Committee Service Awards on September 26 at IPC's Fall Standards Development Committee Meetings in Rosemont, Illinois.

4 From Automotive to IoT, electronica 2016 has a Supporting Program

From November 8–11, 2016, the international electronics industry will meet in Munich at the world's leading trade fair for electronic components, systems and applications. Besides more than 2,800 international exhibitors, visitors can expect an extensive supporting program with four conferences and five forums.

5 Happy's Essential Skills: Recruiting and Interviewing

Hopefully, your career has progressed to the point that you are empowered to recruit your own team or a key person for your team. There are always technical people looking for better jobs, but many times, the most talented are busy doing their work and not looking for a new opportunity.

6 Institute of Circuit Technology Hayling Island Seminar 2016

In recent years, the Hayling Island Seminar has become established as the most popular date on the Institute of Circuit Technology calendar and, as expected, the 2016 event attracted a large gathering of industry professionals to the south coast of England to share knowledge and experience.

7 One World, One Industry: Voting—A Civic Duty and Industry Opportunity

On Tuesday, November 8, more than 240 million people in the United States will have the opportunity to go to the polls and vote, make their voices heard in government, and influence the direction of public policy for years to come. Much of the world is closely watching with interest in this major U.S. election.

8 Mayim Bialik Chosen as Opening Keynote at IPC APEX EXPO 2017

Actress and neuroscientist Mayim Bialik has been selected through a vote of electronics industry professionals to present the opening keynote at IPC APEX EXPO on Tuesday, February 14, 2017 in San Diego.

9 Happy's Essential Skills: Metrics and Dimensional Analysis

After 20 of my columns, readers probably realize that I am an analytical person. Thus, I dedicate this column to metrics—the method of measuring something. I mentioned the four levels of metrics in my June column "Producibility and Other Figures of Merit." I also introduced the five stages of metrics in the second part of the column "Design for Manufacturing and Assembly, Part 2."

10 A New Facility in India for PCB Fabricator ACI

I-Connect007's Barry Matties met with Raj Dhanani and Bryan Ricke of Advanced Circuitry International to discuss their growing footprint in India, recent investments in their U.S. facility, and the future of the RF and antenna markets.

Events

For IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar of Events, click here.

For the complete PCB007 Calendar of Events, click here.

Electronica
November 8–11, 2016
Munich, Germany

FUTURECAR: New Era of Automotive Electronics Workshop
November 9–10, 2016
Atlanta, Georgia, USA

Printed Electronics USA
November 16–17, 2016
Santa Clara, California, USA

IMPACT Europe 2016
November 29, 2016
Brussels, Belgium

ICT-UK Evening Seminar
December 1, 2016
Harrogate, North Yorkshire, UK

International Printed Circuit & Apex South China Fair (HKPCA)
December 7–9, 2016
Shenzhen, China

DesignCon 2017
January 31–February 2, 2016
Santa Clara, California, USA

MD&M West
February 7–9
Anaheim, California, USA

IPC APEX EXPO 2017 Conference and Exhibition
February 14–15, 2017
San Diego, California, USA

China International PCB & Assembly Show (CPCA)
March 2017
Shanghai, China

Thailand PCB Expo 2017
May 11–13, 2017
Bangkok, Thailand

JPCA Show 2017
June 7–9, 2017
Tokyo, Japan

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Sales and Marketing
Tune your strategies for 2017

JANUARY:
Plating and Surface Finishing
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February:
New Technology:
What's new in equipment, processes, testing and more!

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